ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

الكترونيات رقمية

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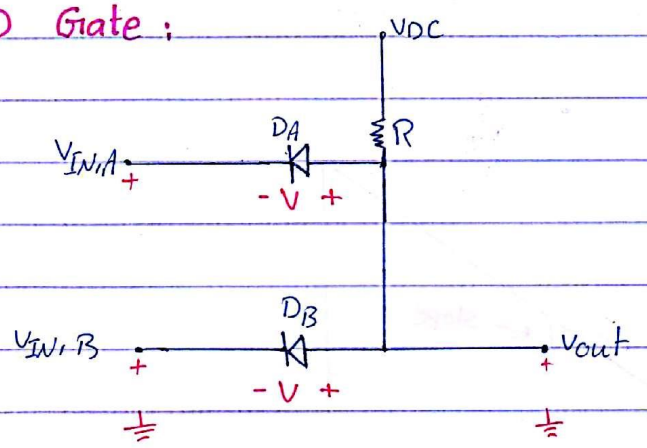
Thursday
22-9-2016

2.5 Diode Resistor Logic (DRL)

. Diode AND Gate :



Case 1: All $V_{IN} > (V_{DC} - V_{D(ON)})$ → V_γ

$-V_{DC} + V + V_{IN} = 0 \rightarrow V = V_{DC} - V_{IN}$

for $V < V_{D(ON)}$ → Diode is off

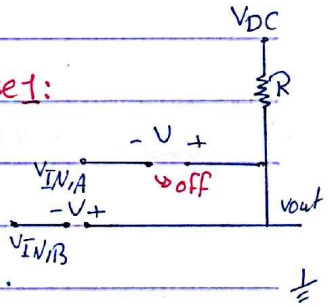
$V_{DC} - V_{IN} < V_{D(ON)}$

$V_{IN} > V_{DC} - V_{D(ON)}$

∴ if both diodes off → $V_{out} = V_{DC}$

∴ if both inputs high → Output is high.

case 1:



Case 2: Any input

$V_{IN} < V_{DC} - V_{D(ON)}$

for $V > V_{D(ON)}$ → Diode is on

$V_{DC} - V_{IN} > V_{D(ON)} \rightarrow V_{IN} < V_{DC} - V_{D(ON)}$

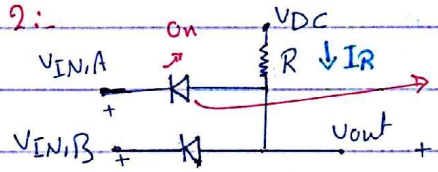
$V_{out} = V_D + V_{IN}$

at $V_{IN} = 0 \rightarrow V_{out} = V_D = 0.7\ V$.

very low input ↵ ↳ for Si Diode

∴ Any low input → low output.

case 2:-



Tip :- Out → AND (3 letters)

بنميز الـ AND بإنه إتجاه الدايودات لبرا السيركت

(Out → AND) ٣ حروف

$$I_R = \frac{V_{DC} - V_{D(ON)} - V_{IN}}{R}$$

$$I_R = \frac{V_{DC} - V_{out}}{R}$$

Truth table

i/p A	i/p B	o/p
L	L	L
H	L	L
L	H	L
H	H	H

- Logic 1 = High
- Logic 0 = Low

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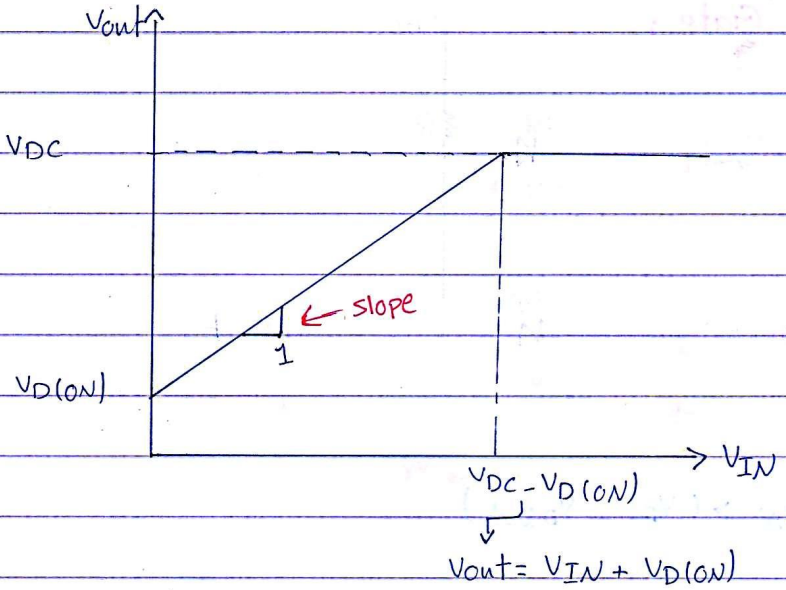
2.5 (DRL)

.VTC (Voltage Transfer characteristic)



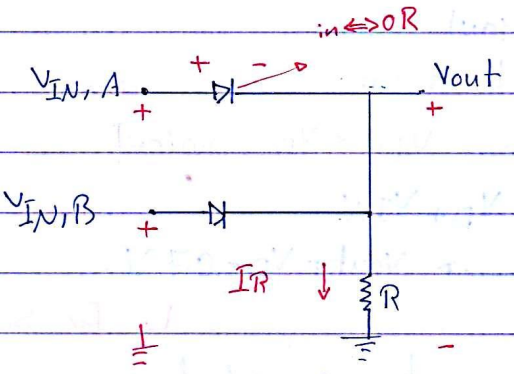
but $V_{out(max)} = V_{DC}$

$\therefore V_{DC} = V_{IN} + V_{D(ON)}$

$V_{IN} = V_{DC} - V_{D(ON)}$

$$\text{Slope} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_{DC} - V_{D(ON)}}{V_{DC} - V_{D(ON)} - 0} = 1 \qquad \therefore \text{slope} = 1.$$

.Diode OR Gate.



A	B	O/P
L	L	L
L	H	H
H	L	H
H	H	H

case 1: Both input voltage $< V_{D(ON)}$

Both input diodes are off

$I_R = 0$

$V_{out} = 0 = V_{OL}$

case 2: Any input voltage $\geq V_{D(ON)}$

Corresponding diode is on.

$V_o = V_{IN} - V_{D(ON)} = V_{OH}$.

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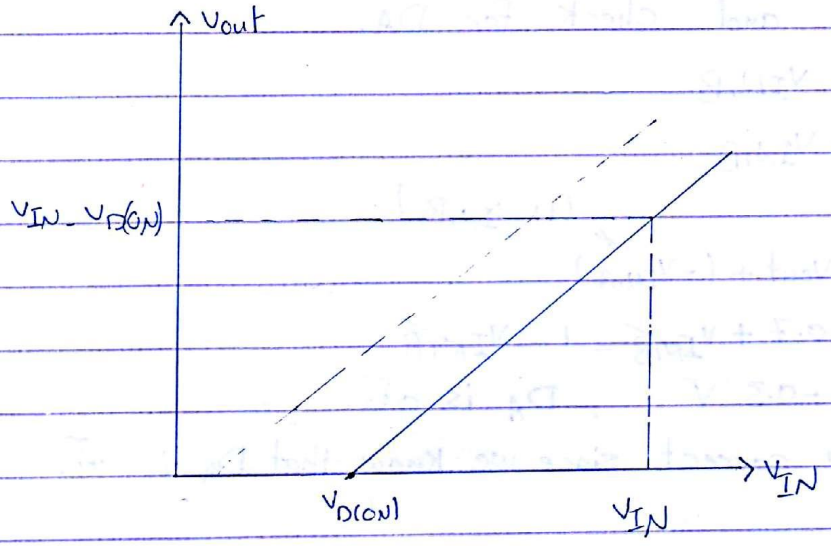
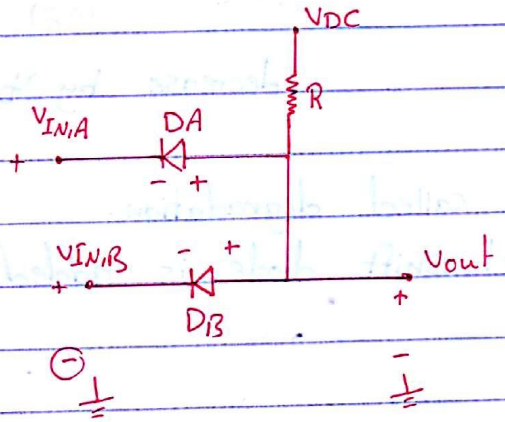
2.5



$$\text{Slope} = \frac{V_{IN} - V_{D(ON)} - 0}{V_{IN} - V_{D(ON)}} = 1.$$

Example 2.3

for AND Gate shown, $V_{IN,A}$ is 1 V above $V_{IN,B}$, show that D_A is cut off ($V_{D(ON)} = 0.7$ V)



Sol: $V_{IN,A} = 1 + V_{IN,B}$ ---- [1]

$V_{IN,B} = V_{out} - V_{DB}$ ---- [2]

$V_{IN,A} = V_{out} - V_{DA}$ ---- [3].

. Assume D_A is on:

From [3] $V_{out} = V_{IN,A} + 0.7$ ---- [4].

[4] in [2] $V_{DB} = V_{IN,A} + 0.7 - V_{IN,B}$ ---- [5].

[1] in [5]. $V_{DB} = 1 + V_{IN,B} + 0.7 - V_{IN,B} = 1.7$ V.

=> inapplicable for diode => assumption incorrect => D_A is off.

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. Now assume D_B on and check for DA.

. From [2] $V_{out} = V_{DB} + V_{IN,B}$

$= 0.7 + V_{IN,B}$

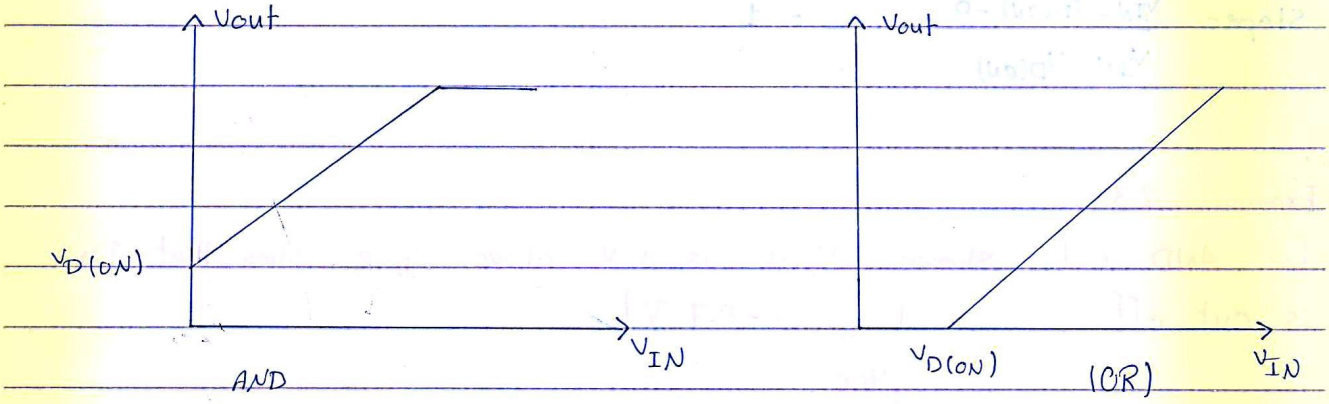
From [3] $V_{DA} = V_{out} + (-V_{IN,A})$ $(1 + V_{IN,B})$

$= 0.7 + V_{IN,B} - 1 - V_{IN,B}$

$= -0.3\ V$, D_A is off.

=> Assumption correct since we know that D_A is off.

2.6 Level shifted Diode Resistor Logic.



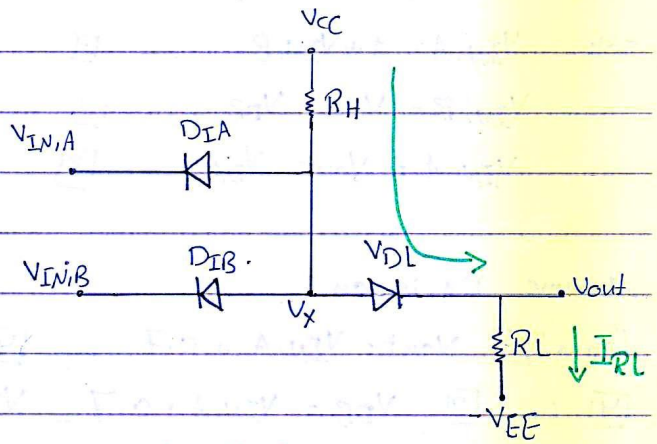
. increase by $V_{D(ON)}$

. decrease by $V_{D(ON)}$

. This increase and decrease is called degradation.

. To remove degradation a level shift diode is added to the AND and OR Gate.

. Level shifted AND Gate.



$V_X = V_D + V_{IN}$

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2.6

Case 1: Any Low input ($V_{IN} < V_X - V_D$)

. Corresponding diode is on.

1.a $V_{IN} > -V_{EE}$

$V_{IN} + V_D > -V_{EE} + V_D$

$V_X > V_D - V_{EE}$

D_L is on.

$-V_{IN} - V_{DI(ON)} + V_{DL(ON)} + V_{out} = 0$

$V_{out} = V_{IN}$.

1.b $V_{IN} < -V_{EE}$

D_L is off

$I_{RL} = 0$

$V_{out} = V_{OL} = -V_{EE}$.

Case 2: both $V_{IN} > V_X - V_D$

∴ both input diodes are off

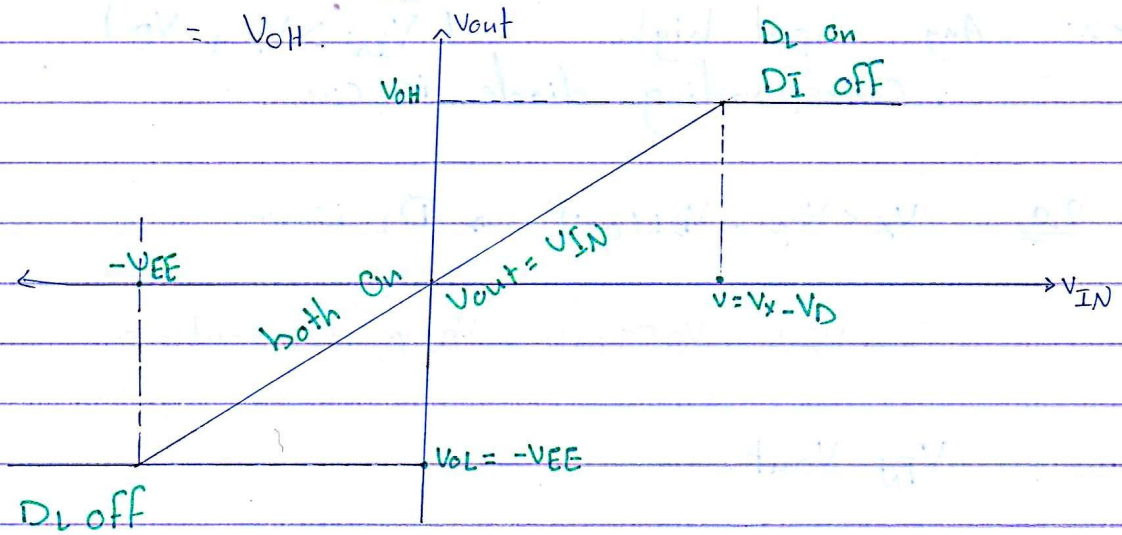
$V_X = V_D + V_{IN}$

$I_D = \frac{V_{CC} + V_{EE} - V_{DL(ON)}}{R_L + R_H}$

$V_{out} = V_{CC} - I_D R_H - V_{DL(ON)}$

$= I_D R_L - V_{EE}$

$= V_{OH}$.



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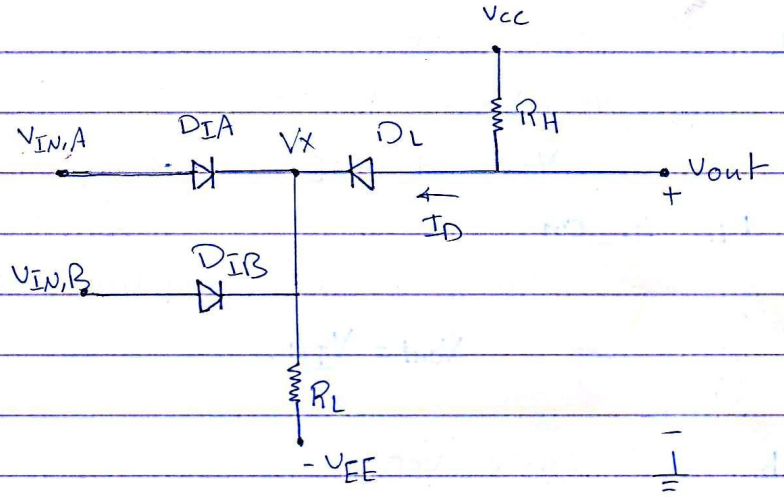
2.6

. Level shifted OR Gate.



Case 1: All inputs Low ($V_{IN} < V_x + V_{D(ON)}$)

D_{IA} , D_{IB} off.

$$I_D = \frac{V_{CC} + V_{EE} - V_{D(ON)}}{R_H + R_L}$$

$$V_{out} = V_{CC} - I_D R_H$$
$$= V_{D(ON)} + I_D R_L - V_{EE}$$
$$= V_{OL}$$

Case 2: Any input high. ($V_{IN} > V_x + V_D$)
. Corresponding diode is on.

2.a $V_x < V_{CC} - V_{DL(ON)} \rightarrow D_L$ is on.

$$-V_{IN} + V_{DF(ON)} - V_{DL(ON)} + V_{out} = 0$$

$V_{IN} = V_{out}$.

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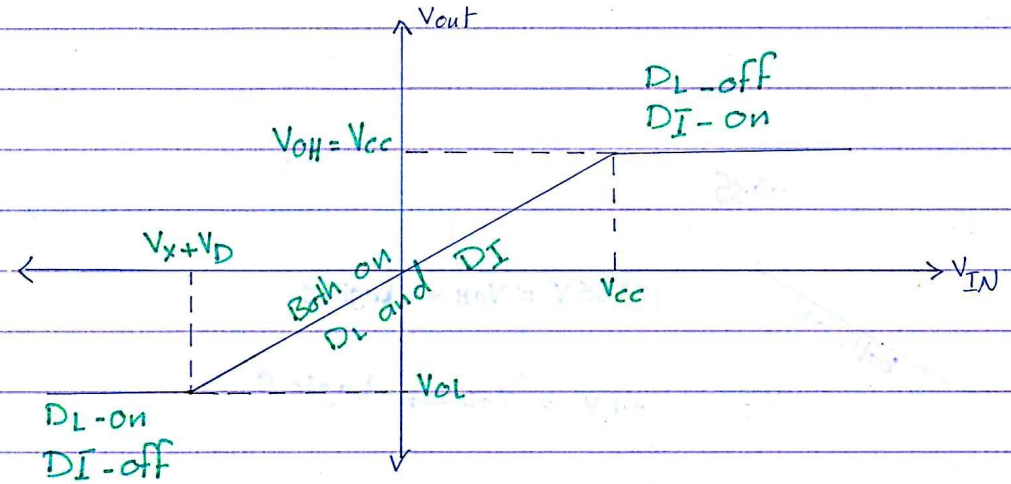
2.6

2.b $V_X > V_{CC} - V_{DC(ON)}$

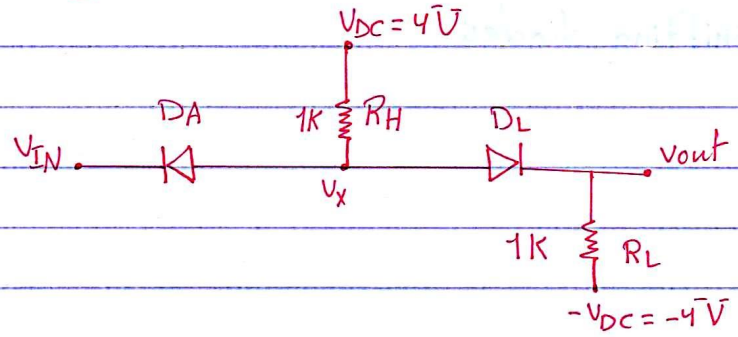
$D_L \rightarrow$ off $\therefore V_{out} = V_H = V_{CC}$



Problem 2.18:-

Draw VTC over an input range of $-V_{DC} \leq V_{IN} \leq V_{DC}$

$V_{DC} = 4\,V$, $V_{D(ON)} = 0.7\,V$



Solution → [1] $V_{IN} < V_X - V_D$, DA is on

1.a $V_X > V_D - 4$, $V_{IN} > -V_{DC} = -4$

D_L is on → $V_{out} = V_{IN}$.

1.b $V_X < V_D - 4$, $V_{IN} < -4$

D_L is off → $V_{out} = -V_{DC} = -4\,V$

[2] $V_{IN} > V_X - V_D$, D_I is off

$$I_D = \frac{4+4-0.7}{2k} = 3.65\ mA$$

$V_{OH} = (3.65 \times 1) - 4 = -0.35\,V$

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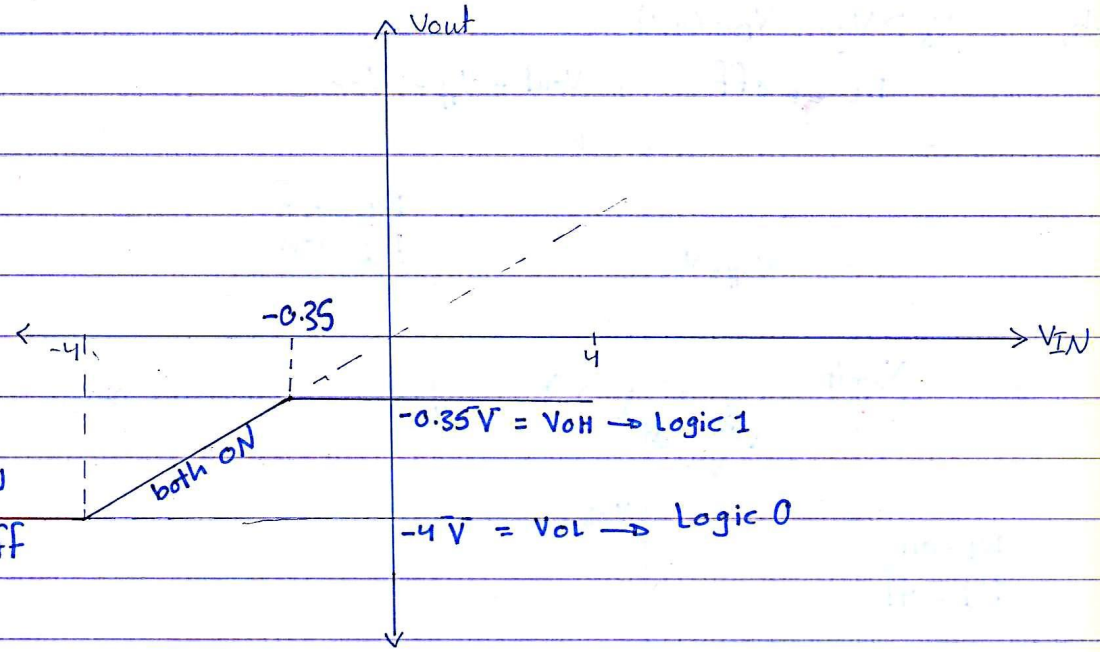
2.6



. Read:

2.7 Clamping Diode for CH7

2.8 Level shifting diodes

Tuesday
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Chapter 4

Introduction to Bipolar Digital Circuits

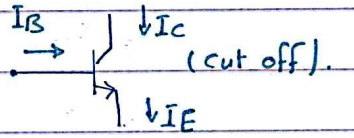
4.1 Analysis of BJT.

1 Cut off.

$I_E = I_B = I_C = 0$

$(B\_C)_J \rightarrow$ Inverse and $(B\_E)_J \rightarrow$ Inverse

↳ Both junctions are reverse biased.



2 Forward Active (FA)

$I_C = \beta I_B$

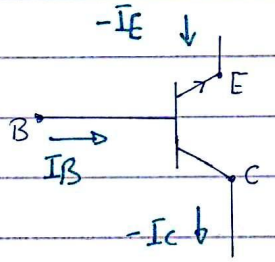
$I_E = I_C + I_B = (\beta+1) I_B$

$(B\_E)_J \rightarrow$ Forward biased.

$(B\_C)_J \rightarrow$ Reverse biased.

$\beta_R << \beta_F$

3 Reverse Active (RA)



$-I_E = \beta_R I_B$

$-I_C = I_B + -I_E$

$-I_C = I_B (1+\beta_R)$

$(B\_C)_J \rightarrow$ Forward biased

$(B\_E)_J \rightarrow$ Reverse biased.

4 Saturation

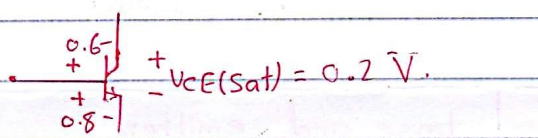
$(B\_C)_J$, and $(B\_E)_J \rightarrow$ Forward

$V_{CE(sat)} = 0.2\ V$

$I_C = \sigma \beta_F I_B$

$0 < \sigma < 1$

$I_E = I_C + I_B$



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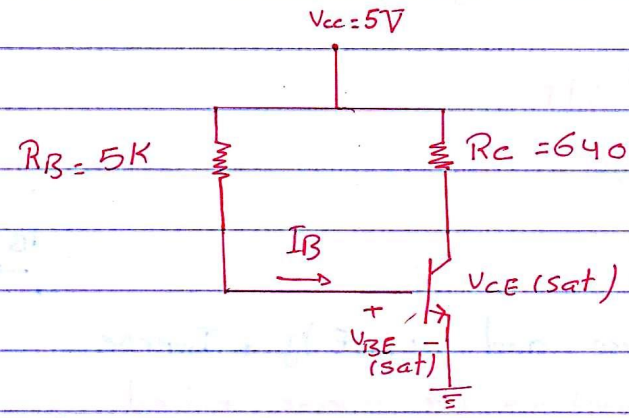
4.1

Example 4.1



$\beta = 65$, Find σ

solution :.

$$I_B = \frac{5-0.8}{5K} = 840\ \mu A.$$

$$I_C = \frac{5-0.2}{640} = 7.5\ mA.$$

$$\sigma = \frac{I_C}{\beta I_B} = 0.137.$$

Standard.

$V_{CE(sat)} = 0.2\ V.$

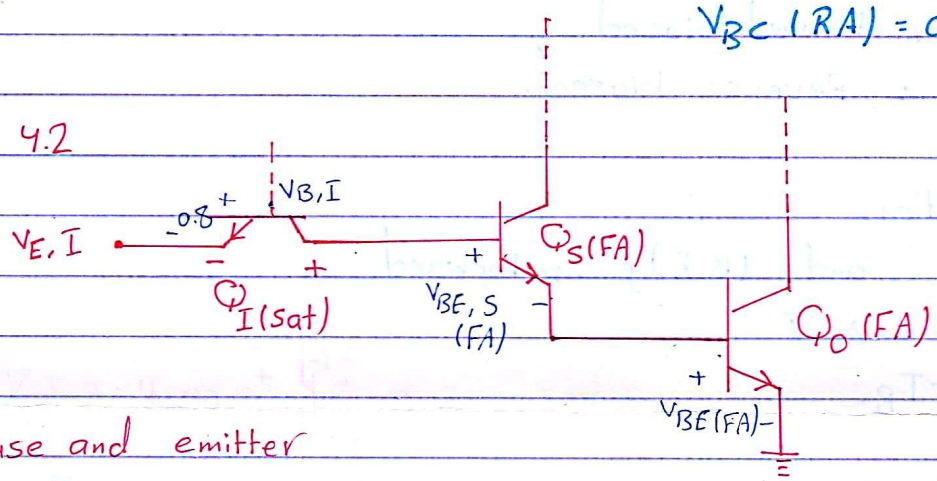
$V_{BE(sat)} = 0.8\ V.$

$V_{BC(sat)} = 0.6\ V$

$V_{BE(FA)} = 0.7\ V$

$V_{BC(RA)} = 0.7\ V.$

Example 4.2



Find base and emitter voltages for each transistor.

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4.1

$V_{E,0} = 0$

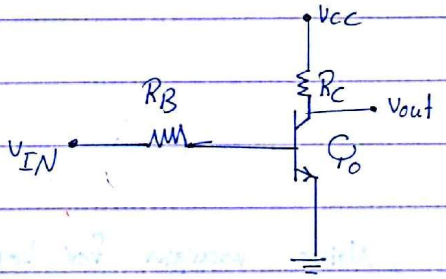
$V_{B,0} = V_{BE,0}(FA) = 0.7\ V.$
$= V_{E,s}$

$V_{B,s} = V_{BE,s} + V_{E,s} = 1.4\ V.$
$V_{E,I} = -V_{CE,I}(sat) + 2V_{BE}(FA)$

$= 1.2\ V$

$V_{B,I} = V_{BE,I}(sat) + V_{E,I} = 0.8 + 1.2 = 2\ V.$

4.2 BJT inverter



. Critical voltages : $V_{OH}, V_{OL}, V_{IH}, V_{IL}$

.

. Volt Low input.

$V_{IN} < V_{BE}(FA) \rightarrow$ BJT is off.

$I_{R_c} = 0$

$V_{out} = V_{OH} = V_{CC}$

. V_{IL} = Input voltage at which Q_0 turns FA.

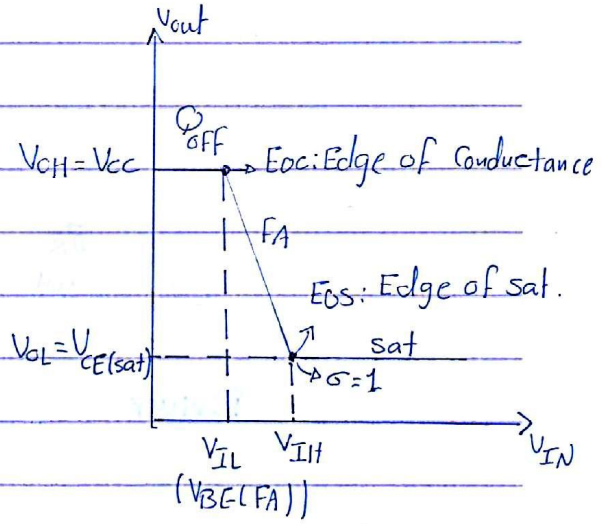
at $V_{IN} = V_{BE}(FA) = V_{IL}$

. As input increases, $I_B \uparrow$, $I_C \uparrow$, $V_{RC} \uparrow$, $V_{out} \downarrow$

(Transmition region)

. V_{OL}: As input increases until Q_0 Saturation.

$V_{out} = V_{OL} = V_{CE}(sat).$



4.2

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- V_{IH} : input at which Q_o saturates.

$$V_{IH} = I_B R_B + V_{BE(sat)}$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$I_B = \frac{I_C}{\beta}, \quad \sigma = 1 \text{ at } E_{OS}$$

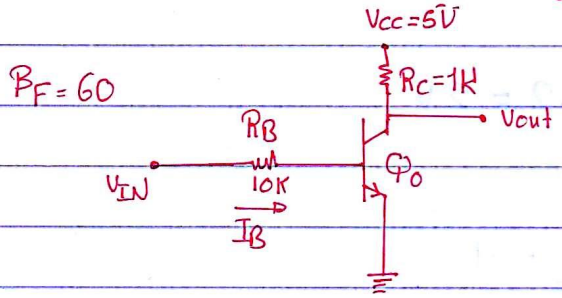
$$\therefore V_{IH} = \frac{V_{CC} - V_{CE(sat)}}{\beta_F} \cdot \frac{R_B}{R_C} + V_{BE(sat)}$$

Example 4.4) Find Noise margins for inverter, $V_{OH} = 5V$

$V_{IL} = 0.7\ V$

$V_{IH} = 1.6\ V$

$V_{OL} = 0.2\ V$



- high noise margin →

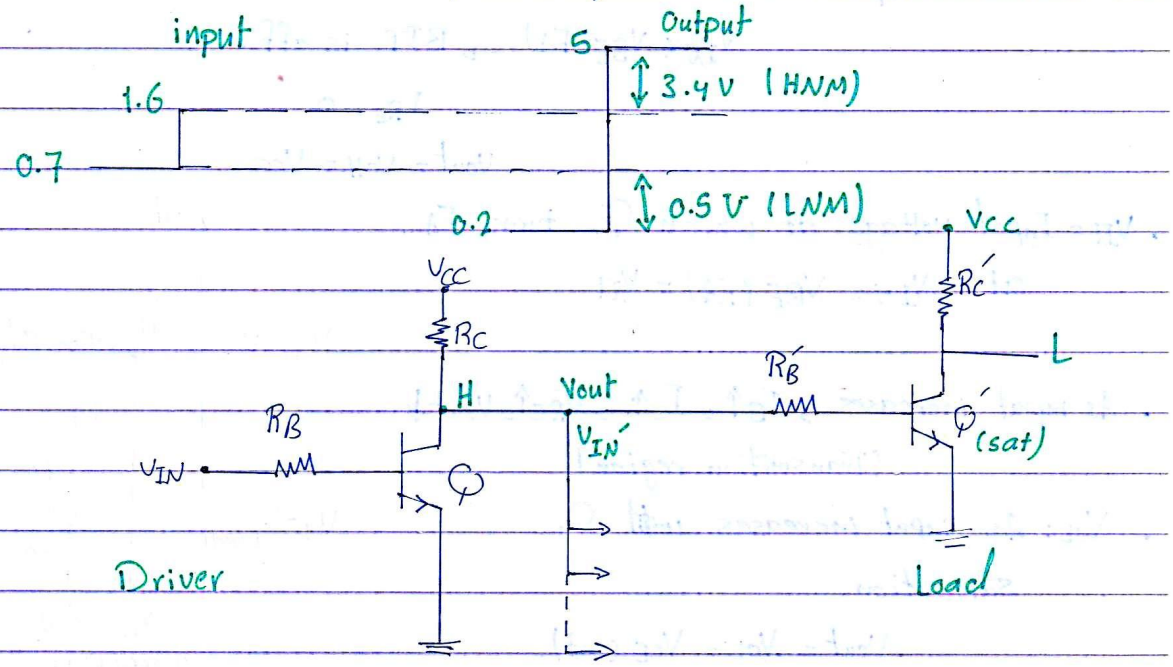
$$V_{HNM} = V_{OH} - V_{IH}$$, Noise margin for logic 1.

- Low noise margin →

$$V_{LNM} = V_{IL} - V_{OL}$$

$\therefore$ HNM = 5 − 1.6 = 3.4 V

LNM = 0.7 − 0.2 = 0.5 V (not practical)



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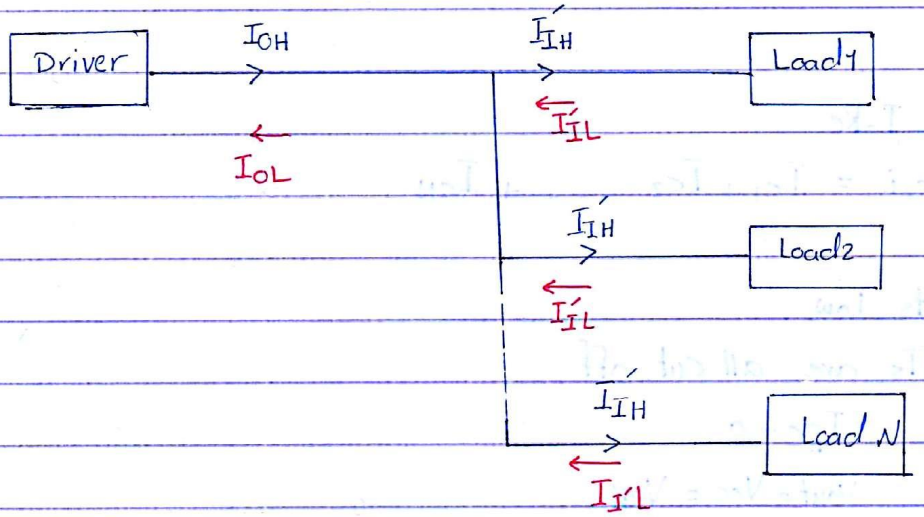
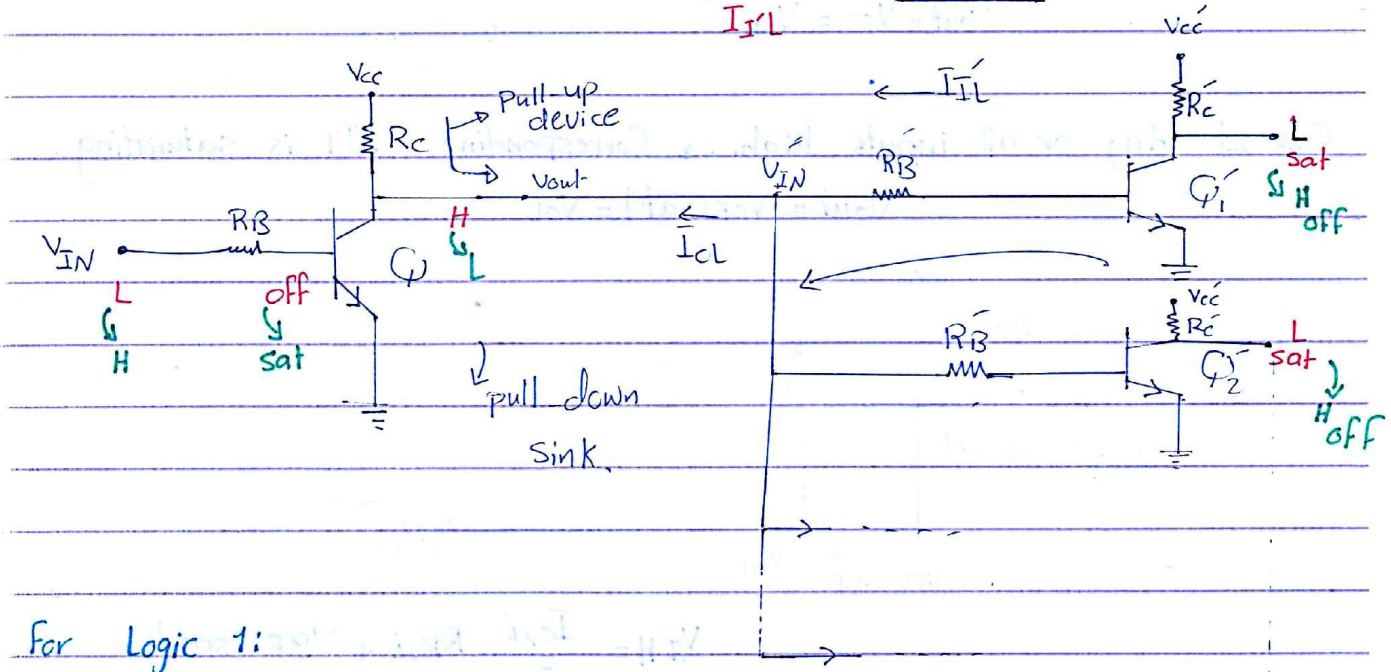
4.3 TTL Circuit.

Fan_out : maximum number of load gates that are allowed at the output of the driver.

Fan_in: is number of inputs allowed at one gate.

$$\text{Fan\_Out} \rightarrow N = \frac{I_o}{I_I'}$$





For Logic 1:

$$N = \frac{I_{OH}}{I_I'H}$$

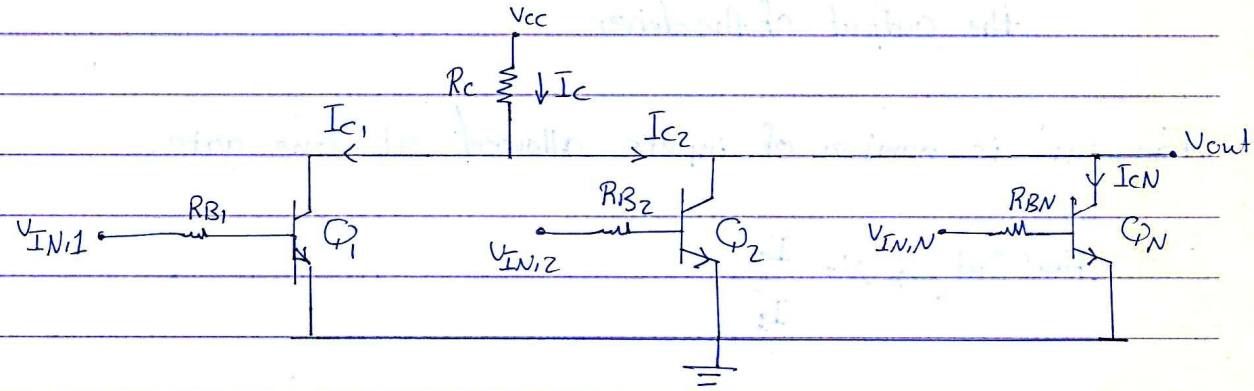
For Logic 0:

$$N = \frac{I_{OL}}{I_I'L}$$

4-10-2016 Tuesday

Chapter 5 Resistor Transistor Logic (RTL)

5.2 Basic RTL NOR Gate.



In general:

$$V_{out} = V_{cc} - I_c R_c$$

$$I_c = \sum_{i=1}^{n} I_{c,i} = I_{c1} + I_{c2} \ldots + I_{cN}$$

Case 1) All inputs low.

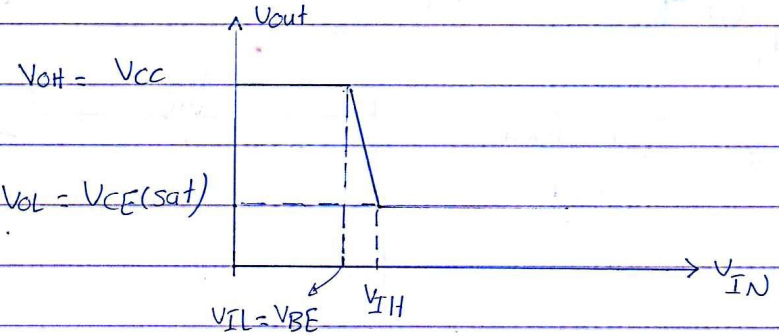
BJTs are all cut-off

$$I_{RC} = 0$$

$$V_{out} = V_{cc} = V_{OH}.$$

Case 2) Any or all inputs high. → Corresponding BJT is saturating.

$$V_{out} = V_{CE(sat)} = V_{OL}$$



$$V_{IH} = \frac{I_{c,i}}{\beta} R_{B,i} + V_{BE(sat)}$$

$$I_{c,i} = \frac{I_{RC}}{\text{number of sat. BJTs}}$$

I_{N1}	I_{N2}	I_{N3}	V_{out}
0	0	0	1
0	0	1	0
0	1	1	0
⋮	⋮	⋮	⋮
1	1	1	0

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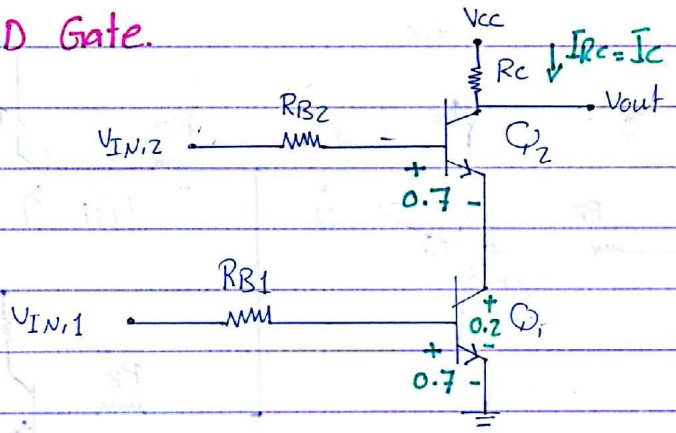
5.3 RTL NAND Gate

. Two inputs NAND Gate.



. for simplicity ignore I_B

$I_{RC} \cong I_{C2} \cong I_{E2} \cong I_{C1} \cong I_{E1}$

$V_{out} = V_{cc} - I_C R_C$

Case 1) Any or all input low

Corresponding BJT is off, and so will be the other one

$I_{RC} = 0 \rightarrow V_{out} = V_{cc} = V_{oH}$.

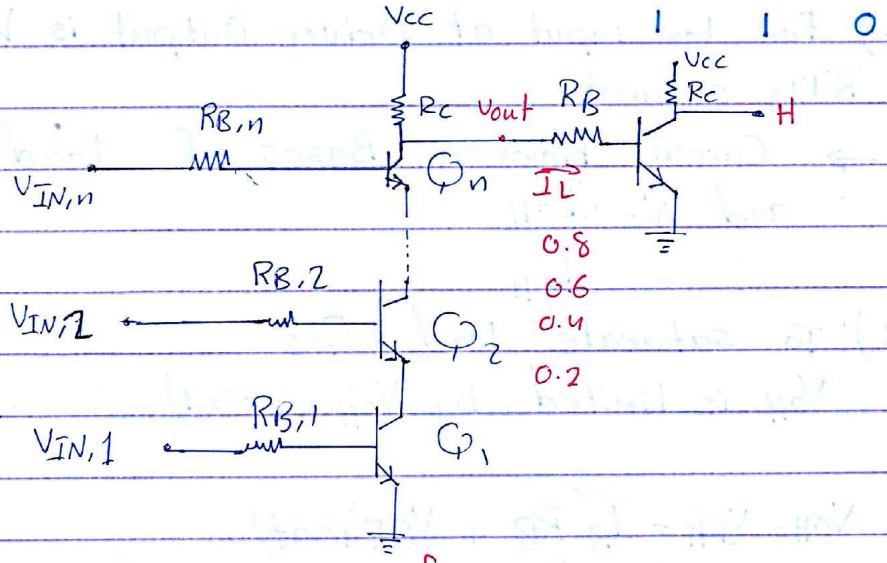
Case 2) All inputs high.

Input high at Q_1 (Q_1 sat) $\rightarrow V_{IL,2} = V_{BE,2(FA)} + V_{CE,1(sat)}$

$\rightarrow$ Both saturating $\rightarrow V_{OL} = 2 V_{CE(sat)}$

IN_1	IN_2	Out
0	0	1
0	1	1
1	0	1
1	1	0

. Multi-inputs RTL



1) All inputs high

$V_{out} = n V_{CE(sat)}$

2) Any input Low

$V_{out} = V_{cc}$

Example 5.1: Find Max-in for RTL NAND if $V_{BE(FA)} = 0.7\,V$, $V_{CE(sat)} = 0.17\,V$

Solution: $n V_{CE(sat)} < V_{BE(FA)}$

$n(0.17) < 0.7$

$n < 4.12$ $\therefore$ 4 inputs are allowed.

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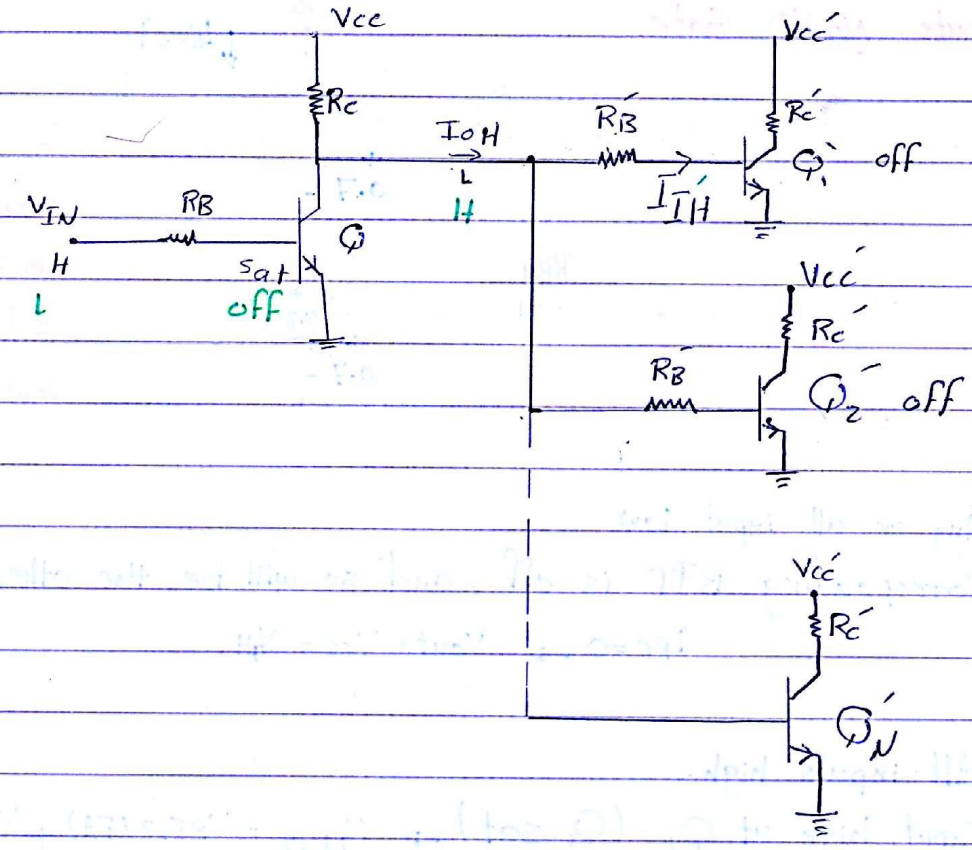
5.4 RTL Fan_Out



$$N = \frac{I_{OH}}{I_{IH}'}$$

1) For high input at Driver, Output is Low →
BJTs of load gates will be off and $I_B = 0$
→ Can't use O/L at Driver to calculate Fan_Out.

2) For low input at Driver Output is high and Load BJTs saturate.
→ Current flows in Bases of load
and $N = \frac{I_{OH}}{I_{IH}}$

3) To saturate load Q's
V_{OH} is limited by V_{IH}' ($\sigma = 1$)

$$V_{OH} = V_{IH}' = I_B' R_B' + V_{BE}'(sat)$$
$$= \frac{I_C'}{\beta} R_B + V_{BE}'(sat)$$
$$= \frac{V_{CC}' - V_{CE}'(sat)}{\beta R_C} R_B' + V_{BE}'(sat)$$

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$$I_{OH} = I_{RC} = \frac{V_{CC} - V_{OH}}{R_C} \quad V_{IH}$$

$$I_{IH} = \frac{V_{IH} - V_{BE(sat)}}{R_B}$$

Example 5.2

$$\rightarrow N = \frac{I_{OH}}{I_{IH}} = \frac{V_{CC} - V_{OH}}{V_{OH} - V_{BE(sat)}} \cdot \frac{10K}{1K}$$

(5, 2.7, 2.7, 0.8)

$$N = 12.1$$

$$\therefore N = 12$$

5.5 RTL power Dissipation

$$P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC}$$

1) $I_{CC(OL)}$ → input high, ○ saturates.

$$I_{CC(OL)} = I_{RC} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

true for Load or no load.

2) $I_{CC(OH)}$ → input Low, ○ off.

high Output:

1) no Load:→

$$I_{CC(OH)} = 0 = I_{RC}$$

2) with load →

$$I_{RC} = I_{CC(OH)} = N I_B$$

$$I_{RC} = N \frac{V_{CC} - I_C R_C - V_{BE(sat)}}{R_B}$$

$$I_{RC} + \frac{I_{RC} R_C N}{R_B} = N \frac{V_{CC} - V_{BE(sat)}}{R_B}$$

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$$I_{RC}\left(1+\frac{R_C}{R_B'}N\right) = N\frac{V_{CC}-V_{BE}(sat)}{R_B'}$$

$$I_{CC(OH)} = I_{RC} = \frac{V_{CC}-V_{BE}(sat)}{R_C + R_B'/N}$$

Example 5.3)

Find $P_{CC(avg)}$: a) no Load
b) with $N=1$.

$V_{CC}=5V$, $R_B=10\,K$, $R_C=1K$, $\beta_F=25$

a) $I_{CC(OL)} = \frac{5-0.2}{1K} = 4.8\,mA$.

$I_{CC(OH)} = 0$

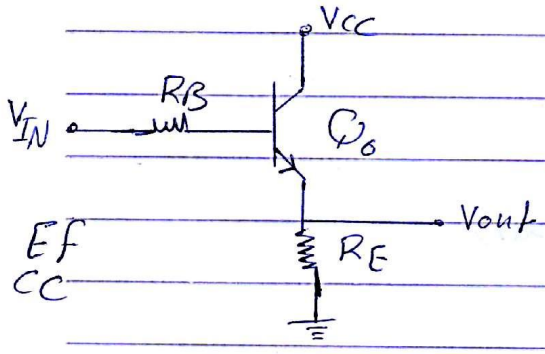
$$P_{CC(avg)} = \frac{0+4.8m}{2} \times 5 = 12\,m\bar{W}$$

b) $I_{CC(OL)} = 4.8\,mA$ (same)

$$I_{CC(OH)} = \frac{5-0.8}{1K+10K} = 382\,\mu A$$

$$P_{CC(avg)} = \frac{4.8m+0.382m}{2} \times 5 = 12.96\,m\bar{W}$$

5.6 Basic RTL Non-Inverter.



$V_{out} = I_E R_E$
$= V_{CC} - V_{CE}$

Case 1) V_{OL}

$V_I < V_{BE(FA)}$

Input low → Q_0 is off $I_B = I_E = I_C = 0$

$V_{out} = V_{OL} = 0$

Case 2) V_{IL}

when $V_{IN} = V_{IL} = V_{BE(FA)}$. (when Q_0 turns initially I_B and I_E are zero and increase when V_{IN} increases

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$V_{out} = I_E R_E$

→ Input increase until Q_0 saturates

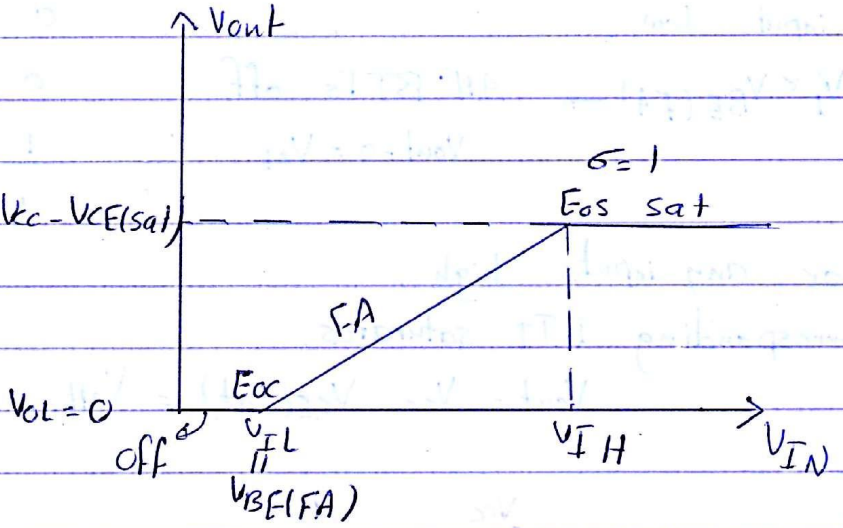
Case 3) $V_{out} = V_{CC} - V_{CE(sat)}$ → V_{OH}

Case 4) V_{IH}

$$V_{IH} = I_{B(Eos)} R_B + V_{BE(sat)} + I_E R_E = I_B R_B + V_{BC(sat)} + V_{CC}$$

, $V_{IH} > V_{CC}$

$$I_B = \frac{I_E}{\beta_{F+1}} \quad , \quad I_E = \frac{V_{CC} - V_{CE(sat)}}{R_E}$$



$$V_{IH} = V_{CC} + V_{BC(sat)} + \frac{V_{CC} - V_{CE(sat)}}{\beta_F + 1} \cdot \frac{R_B}{R_E}$$

Example 5.4) $V_{CC} = 5V$, $R_B = 10\,K$, $R_E = 1K$, $\beta_F = 25$, Find Critical Voltages

Solution: $V_{OL} = 0$

$V_{IL} = 0.7\ V$

$V_{OH} = 5 - 0.2 = 4.8\ V$

$V_{IH} = 5 + 0.6 + \frac{5 - 0.2}{26} \cdot \frac{10k}{1k} = 7.4\ V > V_{CC}$.

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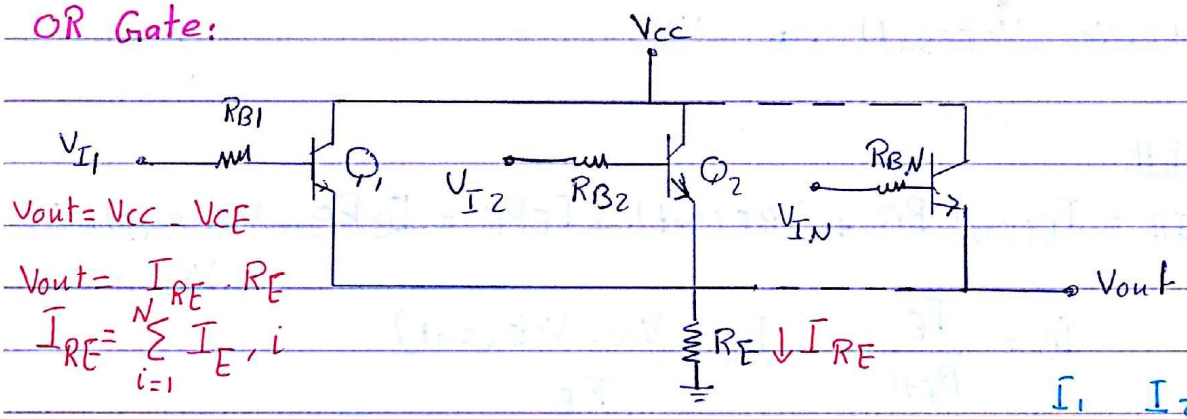
5.7 Basic RTL "OR" and "AND" Gates.

OR Gate:



$V_{out} = V_{CC} - V_{CE}$

$V_{out} = I_{RE} \cdot R_E$

$I_{RE} = \sum_{i=1}^{N} I_{E,i}$

I_1	I_2	Out
0	0	0
0	1	1
1	0	1
1	1	1

Case 1) All inputs Low.

All $V_I < V_{BE(FA)} \rightarrow$ All BJTs off

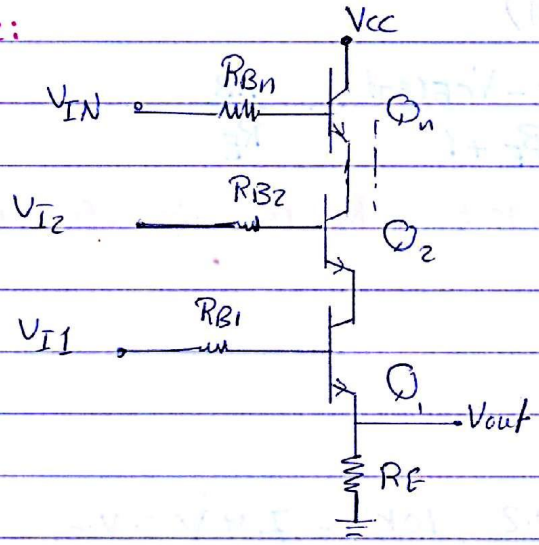
$V_{out} = 0 = V_{OL}$

Case 2) All or any inputs high.

Corresponding BJT saturates.

$V_{out} = V_{CC} - V_{CE(sat)} = V_{OH}$

AND Gate:



I_1	I_2	Out
0	0	0
0	1	0
1	0	0
1	1	1

Case 1) Any input Low

Corresponding BJT is off (so are the rest)

$V_I < V_{IL}$, $I_{RE} = 0$

$V_{out} = V_{OL} = 0$

Case 2) All inputs high.

2.a For a 2-input AND Gate.
Q_1 sat and Q_2 FA.
$V_{out} = V_{OH} = V_{CC} - V_{CE_2}(FA) - V_{CE_1}(sat)$.

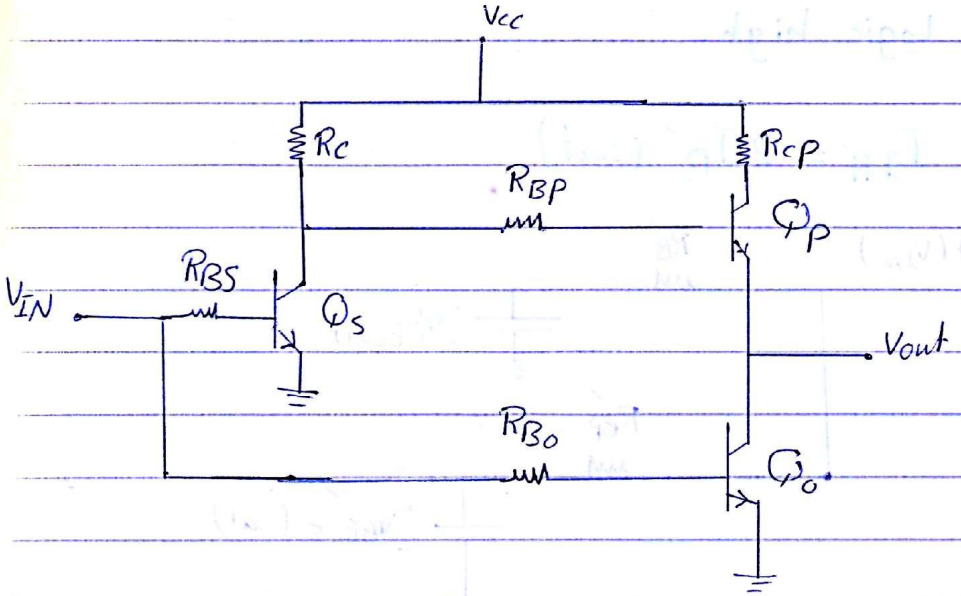
2.b if Both BJTs saturate
$V_{OH} = V_{CC} - 2V_{CE\ sat}$.

. For a n-input AND Gate.
$V_{OH} = V_{CC} - n V_{CE(sat)}$

. For Fan in
$V_{OH} \geq V_{IH}$

→ From Load eq.
$V_{CC} - n V_{CE(sat)} \geq V_{IH}$

5.8 RTL with active pull up.



. provides additional sourcing current.
. $R_{cp} < R_c$. $R_{cp} \approx 0.1 R_c$
→ higher fan-out.

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- Q_o is an inverter that sinks current for low output.
- $R_{BS} = R_{Bo} = R_B$
  They are equal for Q_s and Q_o to run simultaneously

Case 1) For high input
Q_s and Q_o saturates:

$$-V_{CE,s(sat)} + I_{BP} R_{BP} + V_{BE,p(sat)} + V_{CE,o(sat)} = 0$$

$$V_{BE,p(sat)} = -I_{BP} R_{BP}$$

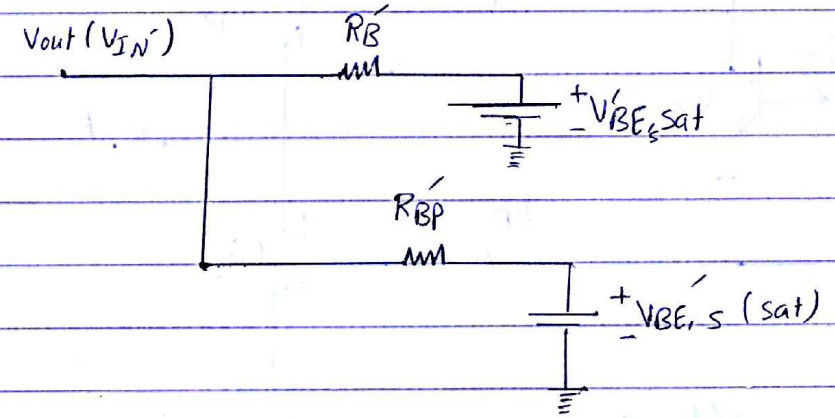
$$I_{BP} = \frac{-V_{BE}}{R_{BP}} \rightarrow Q_p \text{ off.}$$

$$V_{out} = V_{CE,o(sat)} = \text{Logic 0.}$$

Case 2) For low input
Q_s and Q_o are off.
Q_p is saturating.

$$V_{out} = V_{cc} - I_{Rcp} R_{cp} - V_{CE,p(sat)}$$
$$= \text{Logic high.}$$

- $N = \frac{I_{OH}}{I_{IH}'} \rightarrow I_{IH}' = 2 I_B'(sat)$.



RTL Fan_Out

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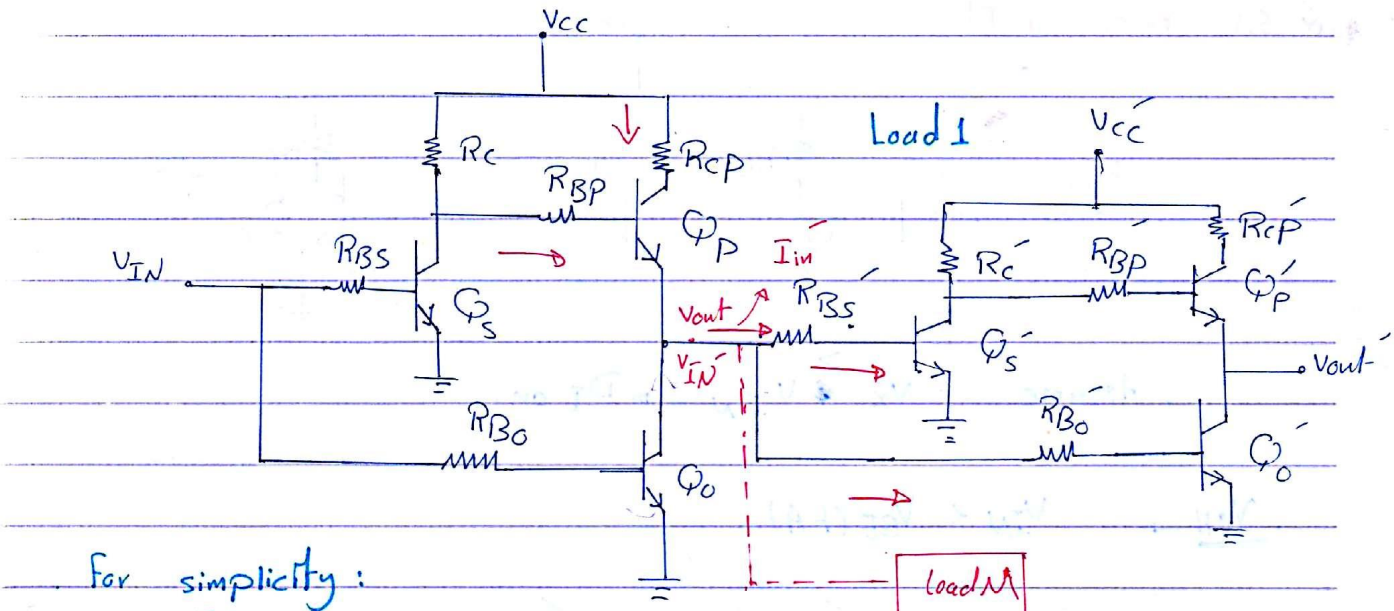

For simplicity:

$I_E \approx I_{RcP}$

$I_{OH} = N I_{I'H}$.

$= N 2 I_B'$

$N = \dfrac{I_{OH}}{2 I_B'}$ → $I_{cp} \simeq I_{E,P}$

$I_{OH} = \dfrac{V_{cc} - V_{cEp(sat)} - V_{OH}}{R_{cp}}$

$I_B' = \dfrac{V_{OH} - V_{BE'(sat)}}{R_B'}$

at $\sigma = 1$

$V_{OH} = V_{IH}' = I_B' R_B' + V_{BE}$

$= \dfrac{V_{cc}' - V_{cE,s(sat)}}{R_c' \beta} R_B' + V_{BE'(sat)}$

$N = \dfrac{V_{cc} - V_{CE(sat)} - V_{OH}}{V_{OH} - V_{BE'(sat)}} \cdot \dfrac{R_B'}{2 R_{cp}}$, $R_{cp} \approx 0.1 R_c$.

$R_{cp} < R_c$

→ N for RTL with active pull up is higher than N with passive pull_up. (Example 5.5, N=12)

Chapter 6

Tuesday
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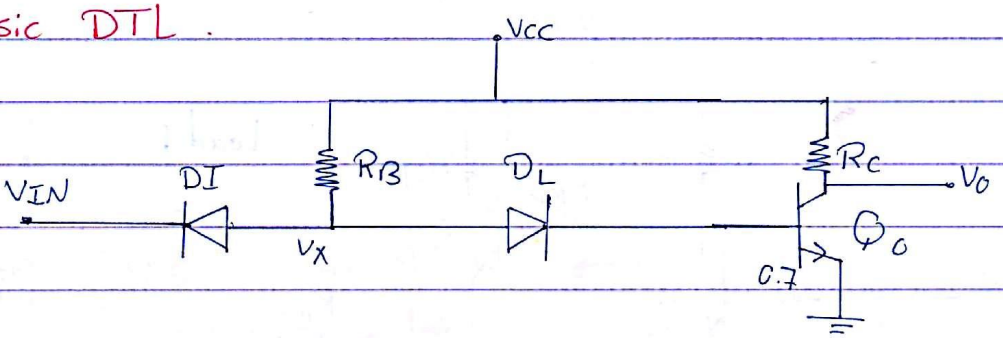
6.1 Basic DTL



. Assume $V_X > V_{IN}$ → D_I on.

. V_{OH} → $V_{IN} < V_{BE(FA)}$

$V_X = V_I + V_{D(ON)} < V_{DL(ON)} + V_{BE,Q}$

$V_{IN} < V_{BE(FA)}$

↳ Q_0 and D_L is off.

$I_{RC} = 0$, $V_{out} = V_{OH} = V_{CC}$.

. V_{IL} : when Q_0 turns on FA.

$V_X = V_{IN} + V_{DI(ON)} = V_{DL(ON)} + V_{BE(FA)}$

$V_{IN} = V_{BE(FA)} = V_{IL}$.

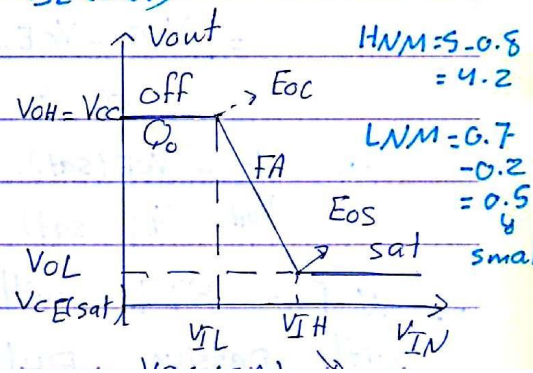
→ As input increases, at some point Q_0 saturates.

. $V_{OL} = V_{CE(sat)}$.

. V_{IH} (when Q_0 saturates)

$V_X = V_{IN} + V_{DI(ON)} = V_{DL(ON)} + V_{BE(sat)}$

$V_{IN} = V_{BE(sat)}$.



HNM = 5 - 0.8 = 4.2

LNM = 0.7 - 0.2 = 0.5 V

small

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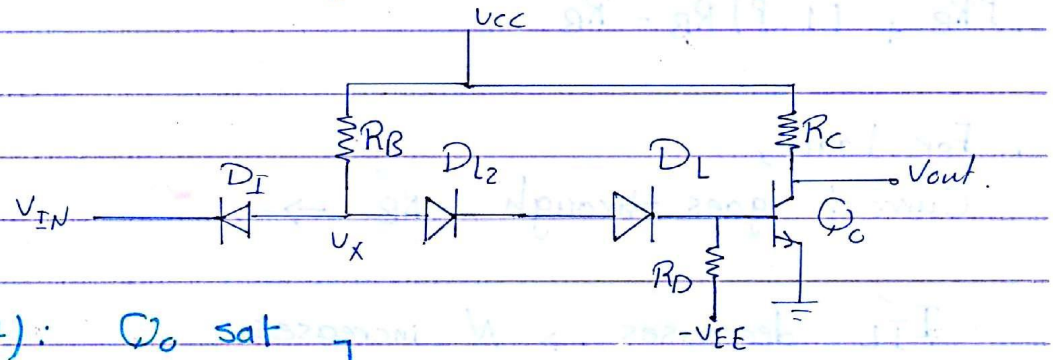
. when $V_x < V_{IN}$ → D_I is off
but V_{CC} provides current directly to Q_o and Q_o saturating.

. R_B is chosen such that Q_o is saturating when
$V_x = V_{BE(sat)} + V_{D(ON)}$

6.2 Modefied DTL

. Additional Level shifting Diode.



$V_{OL} = V_{CE(sat)}$: Q_o sat
$V_{OH} = V_{CC}$ Q_o off
} Same as Basic DTL.

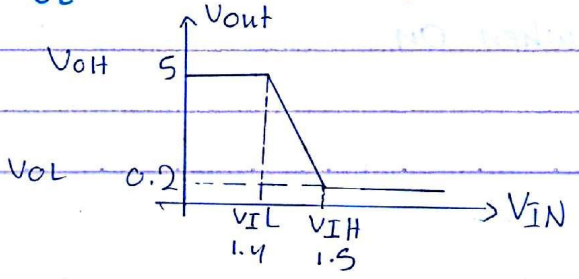
V_{IL}: $V_x = V_{IN} + V_{DI(ON)} = V_{DL} + V_{DL2} + V_{BE}$

$V_{IN} = V_{DL2} + V_{BE(FA)} = V_{IL}$.

V_{IH}: $V_x = V_{IN} + V_{DI(ON)} = V_{DL2} + V_{DL} + V_{BE(sat)}$

$V_{IN} = V_{BE(sat)} + V_{DL(ON)}$

. LNM improves due to the addition of DL_2
. HNM still good.
. RD and -VEE are used as a discharge path for Q_o.



HNM = 3.5 V good
LNM = 1.2 V good.

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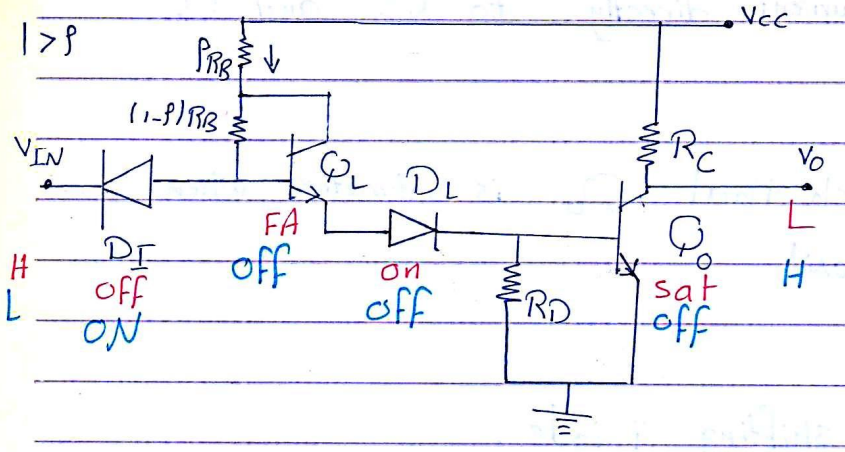
6.3 Transistor Modified DTL



$\beta R_B + (1-\beta) R_B = R_B$

- For Load,
  Current goes through R_B ⇒

  I_{IL} decreases → N increases.

- For Driver,
  Considered Resistance that $I_{E,C}$ passes through is βR_B → $I_{E,L}$ increases
  → $I_{o,L}$ increases.
  → N increases.

- Due to voltage drop on $(1-\beta) R_B$,

  $V_{C,L} > V_{B,L}$

  $V_{BC,L}$ (-Ve)

→ (B-C)J is reverse biased.
→ Q_L is FA when on.

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Example 6.1) Find VTC (no Load)

Sol. → $V_{OH} = V_{CC} = 5\,V$

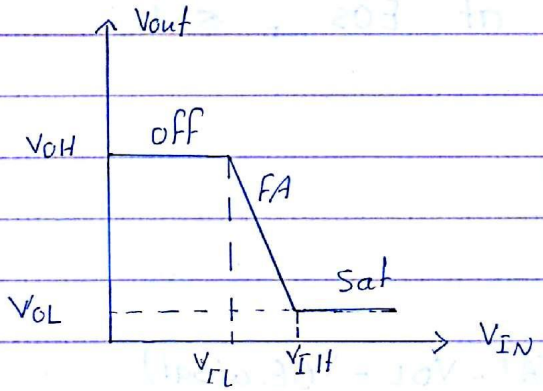
$V_{OL} = V_{CE(sat)} = 0.2\,V$.

↳ V_{IL} (when Q_o turns FA).

$V_{IL} = 2V_{BE(FA)} = 1.4\,V$

↳ V_{IH} (when Q_o saturates).

$V_{IH} = V_{BE,L(FA)} + V_{BE,O(sat)} = 1.5\,V$.



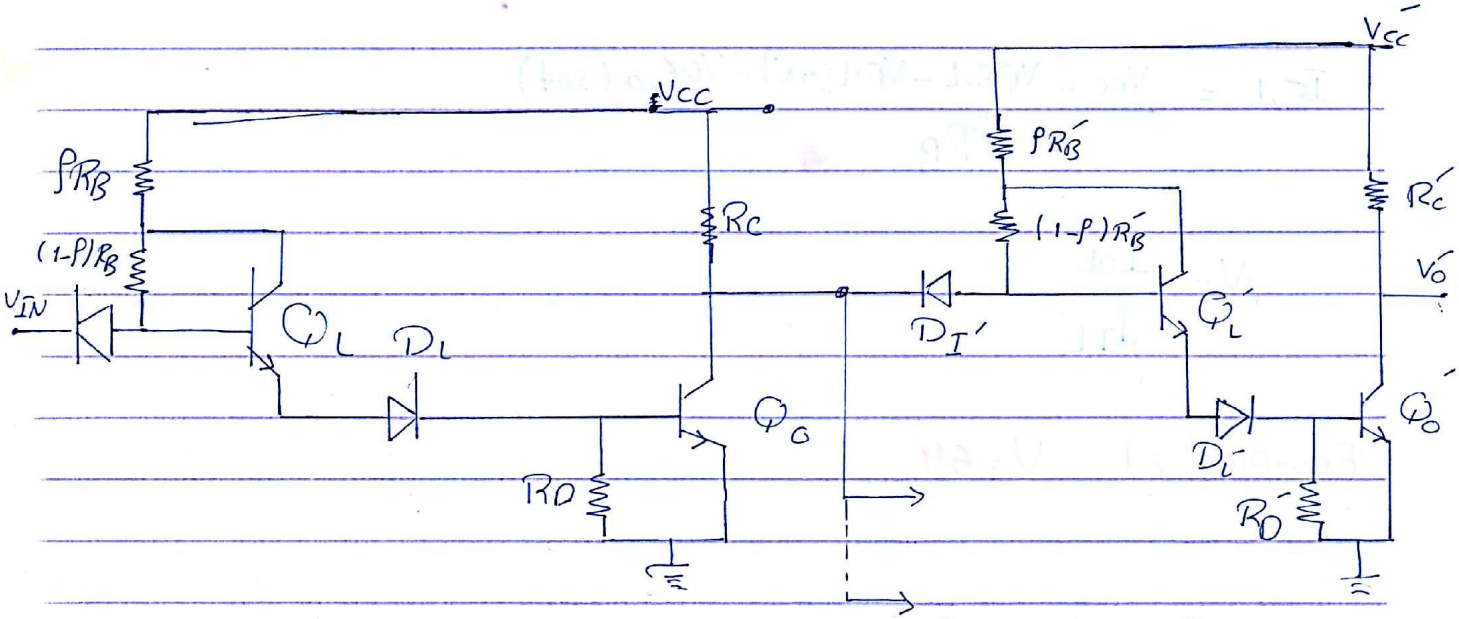
6.4 DTL NAND

. Adding more inputs at more DI's, this cct used as a NAND gate.

⇒

I_{N1}	I_{N2}	V_o
L	L	H
L	H	H
H	L	H
H	H	L

6.5 DTL FAN_Out.



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$$I_{IL}' = \frac{V_{CC} - V_{DI} - V_{CE,0(sat)}}{R_B'}$$

$$I_{OL} = I_{C,0} - I_{RC}$$

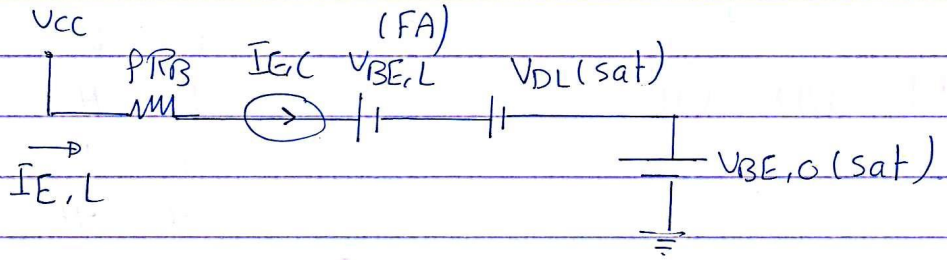
$$I_{RC} = \frac{V_{CC} - V_{CE,0(sat)}}{R_C}$$

$I_{C,0} = \sigma \beta_F I_{B,0}$ at EOS $\rightarrow \sigma = 1$

$I_{B,0} = I_{E,L} - I_{RD}$

$$I_{RD} = \frac{V_{BE(sat)}}{R_D}$$

$$I_{E,L} = \frac{V_{CC} - V_{BE,L(FA)} - V_{DL} - V_{BE,0(sat)}}{\rho R_B + \cancel{\frac{(1-\rho) R_B}{\beta+1}}} \quad \text{ignored}$$



$$I_{E,L} = \frac{V_{CC} - V_{BE,L} - V_{DL(ON)} - V_{BE,0(sat)}}{\rho R_B}$$

$$N = \frac{I_{OL}}{I_{IL}'}$$

Example 6.2) $N = 54$

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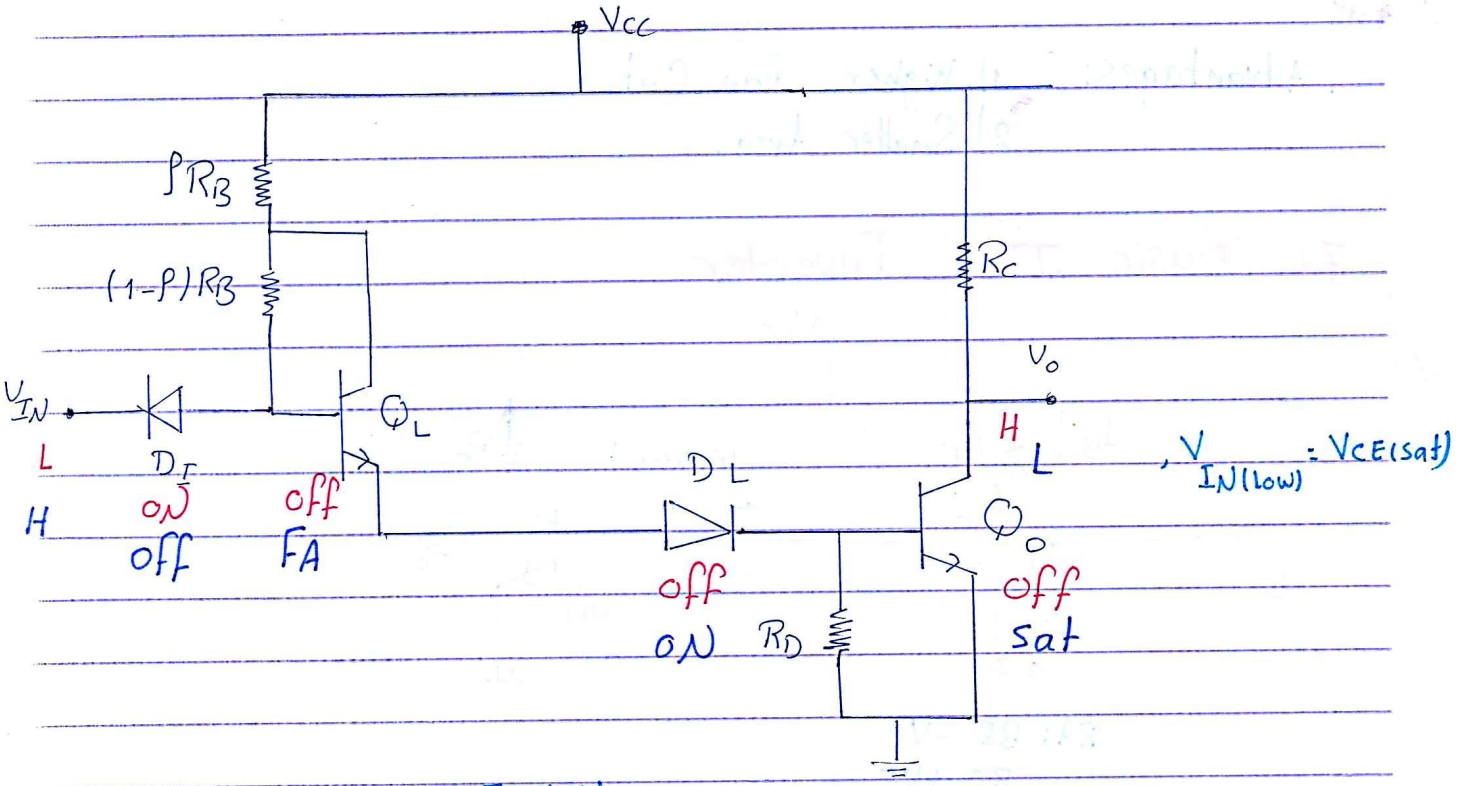
6.6 DTL Powe Dissipation.



$$P_{cc(avg)} = \frac{I_{cc(OH)} + I_{cc(OL)}}{2}$$

1) $I_{cc(OH)}$ → from earlier stage

$I_{RC(OH)} = 0$

$$I_{RB(OH)} = \frac{V_{cc} - V_{DI(ON)} - V_{CE(sat)}}{R_B}$$

$I_{cc(OH)} = I_{RB}$

2) $I_{cc(OL)}$ →

$$I_{RC(ON)} = \frac{V_{cc} - V_{CE,Q(sat)}}{R_C}, \quad I_{\rho RB\,(OL)} = \frac{V_{cc} - V_{BE,L(FA)} - V_{OL} - V_{BE,}}{\rho R_B}$$

$I_{cc(OL)} = I_{RC(OL)} + I_{\rho RB\,(OL)}$

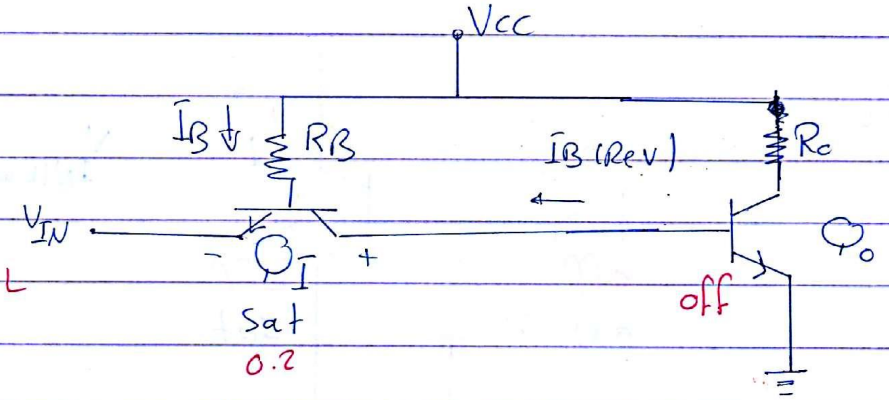
Example 6.3: $P_{cc(avg)} = 8.73\ mW$

Sunday 16.10.2016

Chapter 7 „Transistor Transistor Logic" TTL

Advantages: 1) higher Fan_Out
2) Smaller Area.

7.1 Basic TTL Inverter.



RA: BE -Ve
BC +Ve

$I_B \gg I_{C,I}$

Q_I: unconventional transistor

$V_B > V_E$

$$I_B = \frac{V_{cc} - V_{BE} - V_{IN(low)}}{R_B}$$

Q_1 operates in an unconventional way:
At low inputs, $(B-E)_J$ is forward biased, $I_{B,I}$ enters Q_1 and I_{E_1} exists E_1 to low input.
This transistor action forces $I_{C,I}$ into collector.
But $I_{C,I}$ is limited by reverse Leakage base current of Q_o which is off.

→ Q_I saturates.

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V_{OH} Low input.

$$I_{B,I} = \frac{V_{CC} - V_{BE,I(sat)} - V_{IN}}{R_B} \text{ , in mA.}$$

Q_o is off

$V_{B,O} = V_{CE,I(sat)} + V_{IN(ON)} < V_{BE,O(FA)}$

$I_{RC} = 0$

$V_{out} = V_{OH} = V_{CC}$

V_{IL} → $-V_{IL} - V_{CE,I(sat)} + V_{BE,O(FA)} = 0$

$V_{IL} = V_{BE,O(FA)} - V_{CE,I(sat)}$

$= 0.5$ V.

As V_{IN} increases, $V_{RC}\uparrow$, $V_{out}\downarrow$

untill Q_o saturates at:

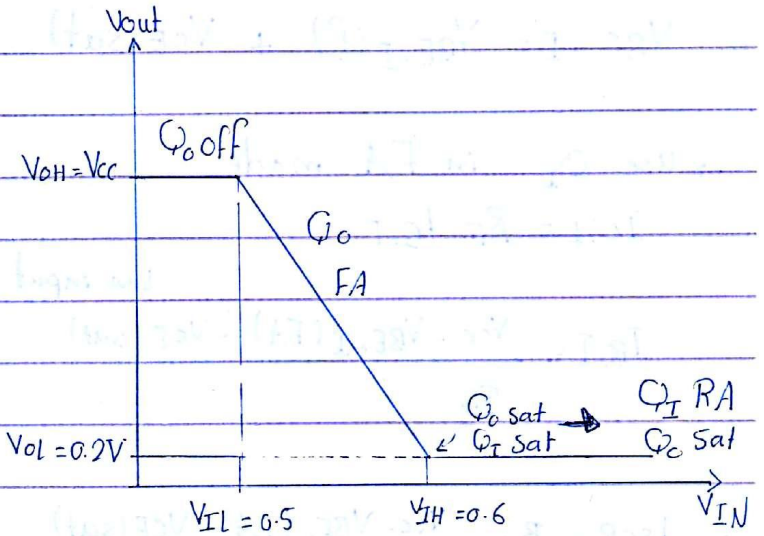
$V_{IH} = V_{BE,O(sat)} - V_{CE,I(sat)} = 0.6$ V

$V_{OL} = V_{CE,O(sat)} = 0.2$ V

As input increases such that:

$V_{E,I} > V_{BE,I}$, $(B.E)_J$ reverse biased.

and $(B.C)_J$ is forward, Large Current is supplied through $(B.C)_J$ to Q_o.



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- Q_o is still saturating
  Q_I is in RA.

$V_{BC,I} = V_{cc} - \underbrace{I_B R_B - V_{BE,o}(sat)}$ → less than V_{cc}

$V_{BC,I}$ → +Ve
→ Q_I RA

SCR

7.2 Comparison of stored Charge Removal between DTL and TTL

Q_o Sat → off
O/P L → H
IN H → L

- Current stored in Base of Q_o untill discharge through Q_I and Low input.

$I_{c,I} = I_{SCR}$
Input Low → (BE).I (+Ve).

- $V_{B,I} = V_{BE,I}(?) + V_{IN}(low)$ ~~$V_{E,,I}$~~

- $V_{c,I} = V_{BE,o}(sat)$
- $V_{BC,I} = V_{BE,I}(?) + V_{CE}(sat) - V_{BE,o}(sat) = 0.6$

→ Use Q_I in FA mode.

$I_{c,I} = \beta_F I_{B,I}$

Low input

$I_{B,I} = \dfrac{V_{cc} - V_{BE,I}(FA) - V_{CE}(sat)}{R_B}$

→ $I_{SCR} = \beta_F \dfrac{V_{cc} - V_{BE,}(FA) - V_{CE}(sat)}{R_B}$

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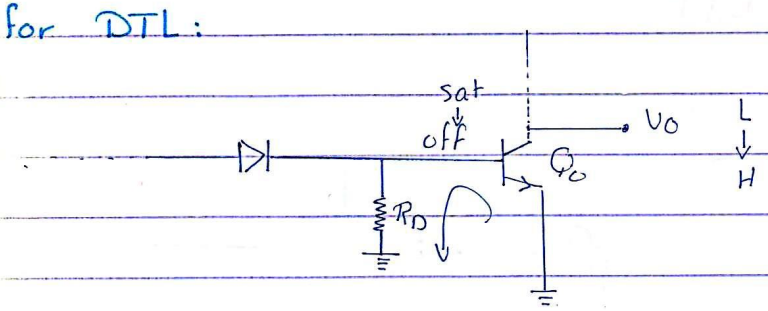
for DTL:



$$I_{RD} = I_{SCR} = \frac{V_{BE,O}(sat)}{R_D}$$

$I_{SCR}(TTL) \gg I_{SCR}(DTL)$

→ TTL removes stored charge faster than DTL.

→ DTL has higher Delay.

Example 7.1:

Find factor of improvement for SCR, between DTL and TTL

DTL: $R_D = 5K$

TTL: $R_B = 2K$

$V_{CC} = 5V$, $\beta_F = 50$

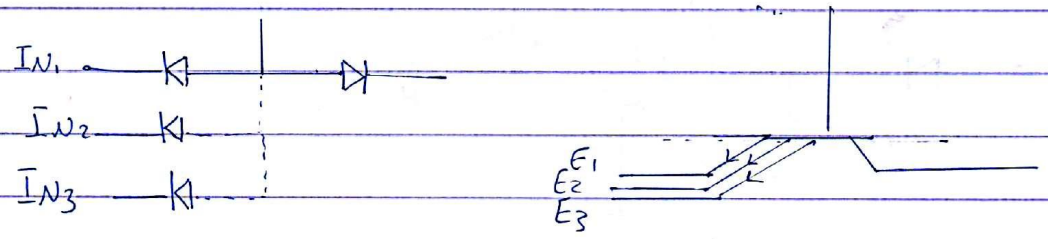
$$I_{C,I}(TTL) = 50 \quad \frac{5-0.7-0.2}{2K} = 102.5 \text{ mA}.$$

$$I_{RD} = \frac{0.8}{5K} = 0.160 \text{ mA}$$

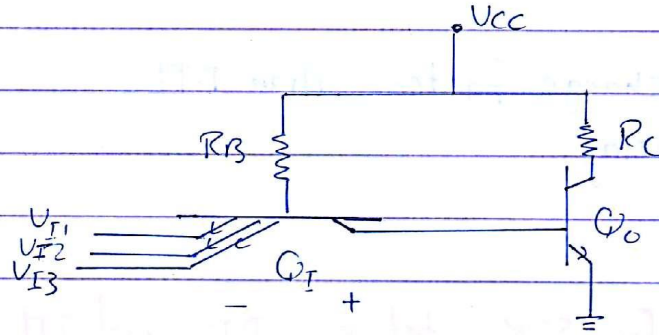
$$\frac{102.5}{0.16} = 640.6$$

Tuesday
18.10.2016

7.3 Basic TTL NAND Gate with Multiple Emitter BJT

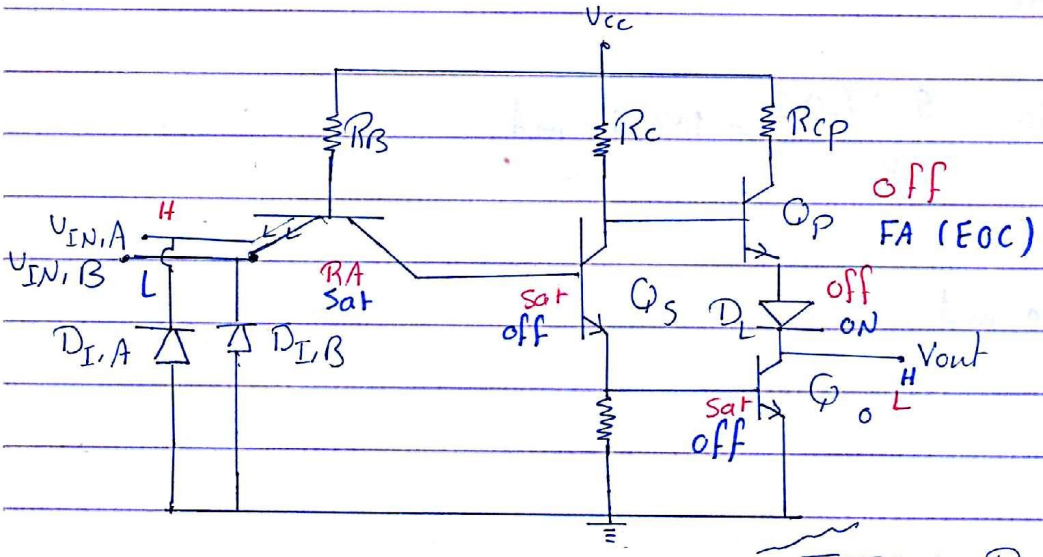


- Any input low, Q_I sat, Q_o off output H, $V_{OH} = V_{CC}$
- All inputs high, Q_I RA, Q_o sat output L, $V_{OL} = V_{CE(sat)}$



Pull-up / Pull-down

7.4 Standard TTL NAND Gate with TOTEM Pole output



TOTEM Pole

Q_S: for logic inversion.

Q_P, Q_o, DL : TOTEM pole

R_{DI} Discharge path for Q_o

D_{IA}, D_{IB}: Clamping diodes that clamp input at $-V_\gamma$, in case input goes below $-V_\gamma$ (for protection)

CH 7

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$V_{B,P} = V_{CE,S}(sat) + V_{BE,O}(sat)$

$V_{E,P} = V_{DL} + V_{CE,O}(sat)$

$V_{BE,P} = V_B - V_E = 0.1\ V < V_{BE}(FA)$

$\therefore Q_O$ is off.

7.5 Standard VTC for TTL with TOTEM Pole.

V_{OH} $V_{IN} < V_{BE}(FA) - V_{CE}(sat)$

Q_I sat $V_E < V_B$

$$I_{B,I} = \frac{V_{CC} - V_{BE,I}(sat) - \cancel{V_{IN}(ON)}\ V_{CE}(sat)}{R_B}$$

Large $\gg I_{C,I} = -I_{B,S}$ (leakage)

Q_S, Q_O off, Q_P and DL on.

$V_{OH} = V_{CC} - V_{BE,P}(FA) - V_{DL}(ON)$, Ignore $I_{B,P}(FA)$

$= 3.6\ V$.

. V_{IL} (when Q_S turns FA) at $V_{IL} = V_{BE,S}(FA) - V_{CE,I}(sat)$

$= 0.5\ V$

. As input increases $I_{B,S}\uparrow$, $I_{C,S}\uparrow$, $I_{RC}\uparrow$, $V_{out}\downarrow$

. Input increases until Q_O turns FA at V_{IB}.

. V_{IB} = Input break voltage.

. $V_{IB} = -V_{CE,I}(sat) + V_{BE,S}(FA) + V_{BE,O}(FA) = 1.2\ V$.

. V_{OB} : output voltage at break point Q_O still at (EOC)

$V_{OB} = V_{CC} - I_{RC}R_C - V_{BE,P}(FA) - V_{DL}(ON)$

Tuesday
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CH7

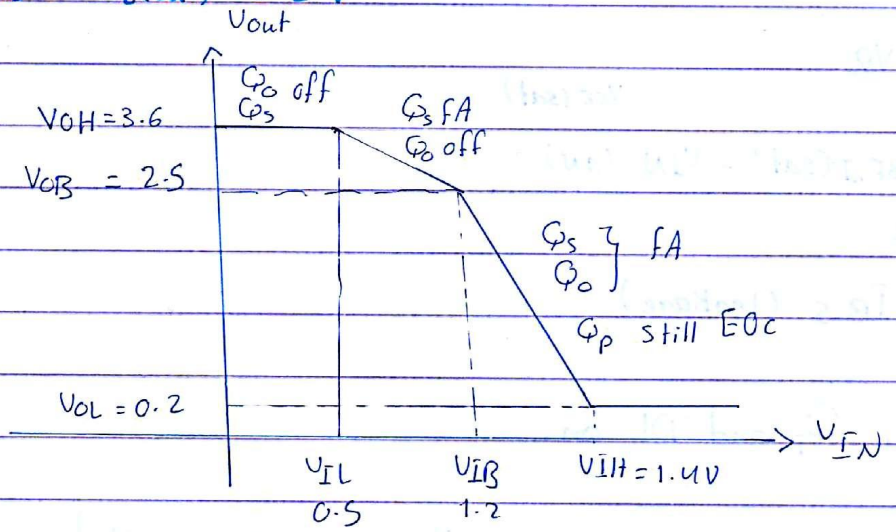
- Ignore $I_{B(FA)}$ for Q_p and Q_s

- $I_{RC} \approx I_{C,S} \approx I_{E,S} \approx I_{RD} = \frac{V_{BE,O(FA)}}{R_D}$

- $V_{OB} = V_{CC} - \left(\frac{R_C}{R_D} + 1\right) V_{BE(FA)} - V_{DL(ON)}$

- $V_{IH} = -V_{CE(sat)} + 2V_{BE(sat)} = 1.4\ V$
  $\quad\ \ {}_{'I}$

$V_{OL} = V_{CE(sat)} = 0.2\ V$



7.6 TTL Fan-out

$$N = \frac{I_{OL}}{I_I'}, \quad I_I'{}_L = \frac{V_{CC}' - V_{BE,I(sat)} - V_{CE(sat)}}{R_B'}$$

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Sunday

CH7 : 7.7 Power Dissipation

. $I_{CC(OH)} \rightarrow$

$$I_{RB(OH)} = \frac{V_{CC} - V_{BE,I(sat)} - V_{CE(sat)}}{R_B}$$

$I_{RC(OH)} = I_{B,P(FA)} \rightarrow$ ignore.

$I_{RCP(OH)} \rightarrow$ Small (ignore).

$I_{CC(OH)} = I_{RB(OH)}$.

. $I_{CC(OL)} \rightarrow$

$$I_{RB(OL)} = \frac{V_{CC} - V_{BC,I(RA)} - 2V_{BE(sat)}}{R_B}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE,S(sat)} - V_{BE,O(sat)}}{R_C}$$, $I_{RCP(OL)} = 0 \rightarrow Q_P$ is off.

$$I_{CC(OL)} = I_{RB(OL)} + I_{RC(OL)}$$

. $$P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} \cdot V_{CC}$$

. Example 7.4: $P_{CC(avg)} = 10.4\ mW$

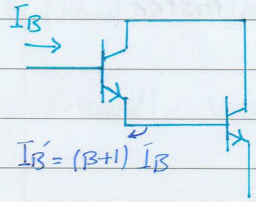
CH7: 7.9 Low Power TTL

. For lower power $\rightarrow$ lower currents are needed, (Higher resistor values)
. But a disadvantage is due to less current $\rightarrow$ we have less fan_out.

. Example 7.5: $P_{CC(avg)} = 919\ \mu W \approx 1\ mW$

CH7: 7.10 High Speed TTL (HTTL)

. Resistor values are decreased to increase current.
$\rightarrow$ Higher speed , $\rightarrow$ Higher fan_out
. Q_P is replaced by a Darlington pair $\rightarrow$ which provides higher current.



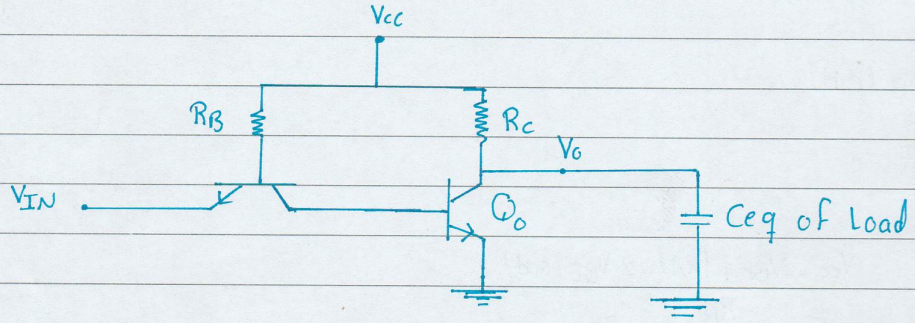
. $I_O = (\beta+1)^2 I_B \approx \beta^2 I_B$

27-10-2016 Thursday

CH7: Back to 7.4 Comparison of load capacitance charging

Basic TTL	VS	TOTEM Pole TTL
passive pull_up		active pull_up
$I_{passive}$		I_{active}
$I_{ch,passive}$		$I_{ch,active}$

1) Basic TTL:

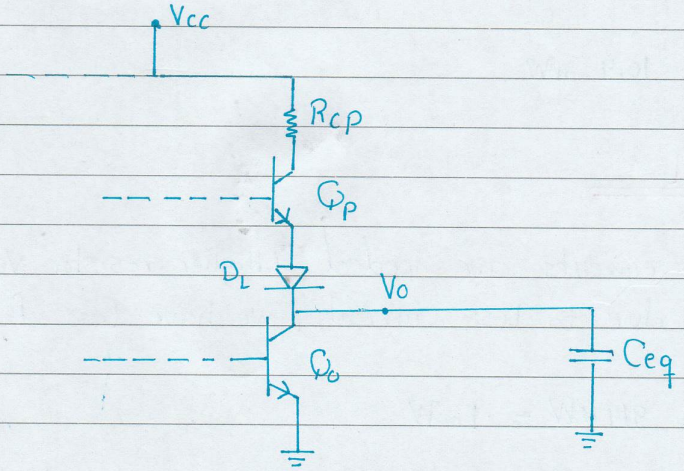


Q_o: sat → off , V_o: L → H↑

$I_{passive} = R_c . C_{eq}$

$I_{passive} = \frac{V_{cc} - V_{CE(sat)}}{R_c}$ (initially)

2) TOTEM Pole TTL:



Q_o : sat → off , V_o: L → H

$I_{active} = R_{cp} . C_{eq}$

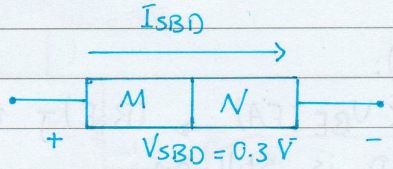
$I_{active} = \frac{V_{cc} - V_{CE,p(FA)} - V_{D(ON)} - V_{CE(sat)}}{R_{cp}}$

- $R_{cp} \approx 0.1 R_c$ → $I_{active} < I_{passive}$ ∴ Active is faster
  $I_{active} > I_{passive}$ ∴ Active is faster

27-10-2016
Thursday

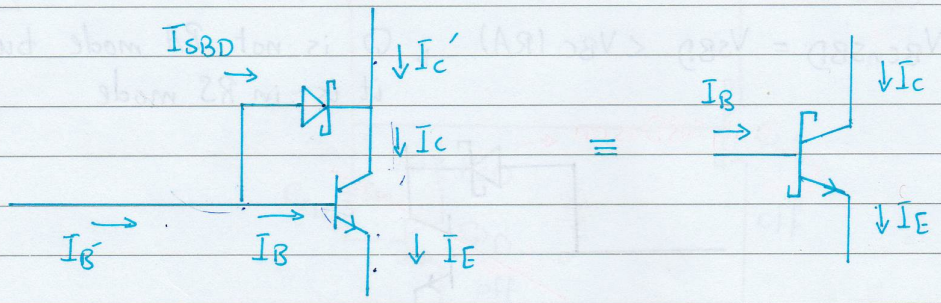
CHAPTER 8: Shottky Transistor Logic (STTL)

. Shottky Diode :



SBD: Shottky Barrier Diode

. Symbol:



in Hard EOS mode

$I_C = \beta I_B = I_C' + I_{SBD}$, $I_C' = I_C - I_{SBD}$

. Shottky Clamped BJT:

→ Regular BJT : $V_{BC}(sat) = V_{BE}(sat) - V_{CE}(sat) = 0.8 - 0.2 = 0.6\ V$

→ To avoid saturation, a SBD is connected between base and collector.

→ When BJT tends to saturate (I_B' increases such that BJT is about sat), SBD turns on at (0.3 V) and $V_{BC} < V_{BC}(sat)$, also current is directed through SBD. This will prevent BJT from saturating, and transistor is said to operate in the [Hard mode]. (Some books Called it EOS).

. Operation modes for Q_{SBD}:

1) Cut_off: I_B' current is not enough to turn on SBD and the BJT.
. $I_B = I_E = I_C = 0$, $I_{SBD} = 0$, Q_{SBD} is cut_off.

2) FA: I_B' increases, such that $V_B > V_E$ but $V_B < V_C$
. Q_{SBD} operates in FA mode $V_{BE}(FA) = 0.7\ V$

3) Hard mode: SBD is on, $V_{SBD} < V_{BC}(sat)$, BE → +Ve ; Q_{SBD} in Hard mode.
. $I_C(Hard) = \beta_F I_B$, $I_C'(Hard) = I_C - I_{SBD}$

$V_{CE}(Hard) = V_{BE}(Hard) - V_{SBD} = 0.8 - 0.3 = 0.5\ V$.

CH8: 8.2 Shottky Clamped BJTs

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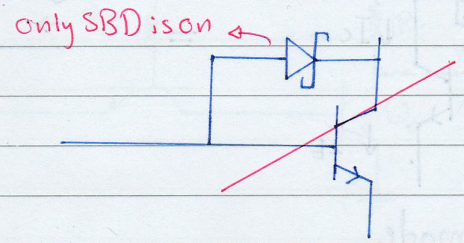
4) Reverse Shottky (RS):

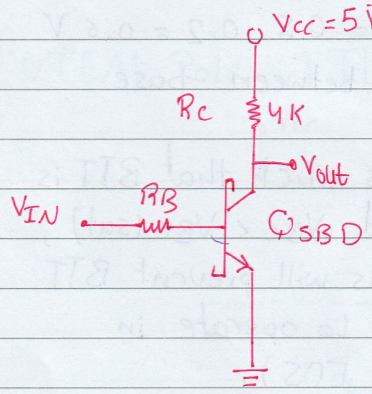
. $V_B < V_E$, $V_{BE} < V_{BE(FA)}$ → (B-E)J Reverse biased.
but $V_B > V_C$, V_{SBD} is still on.
and since BJT's $V_{BC} > V_{SBD}$, as in only SBD is on
$I_B' = I_{SBD} = -I_C'$

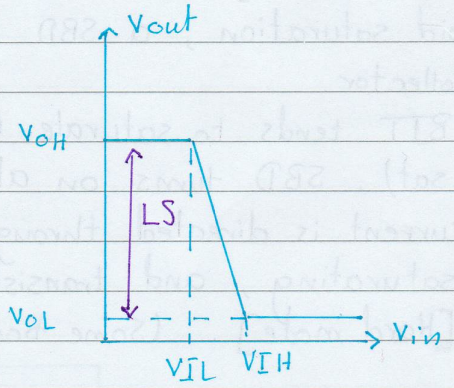
. $V_{BC,SBD} = V_{SBD} < V_{BC(RA)}$ → Q is not RA mode but it is in RS mode



Example 8.1: find VTC and LS (Logic swing).

$LS = V_{OH} - V_{OL}$





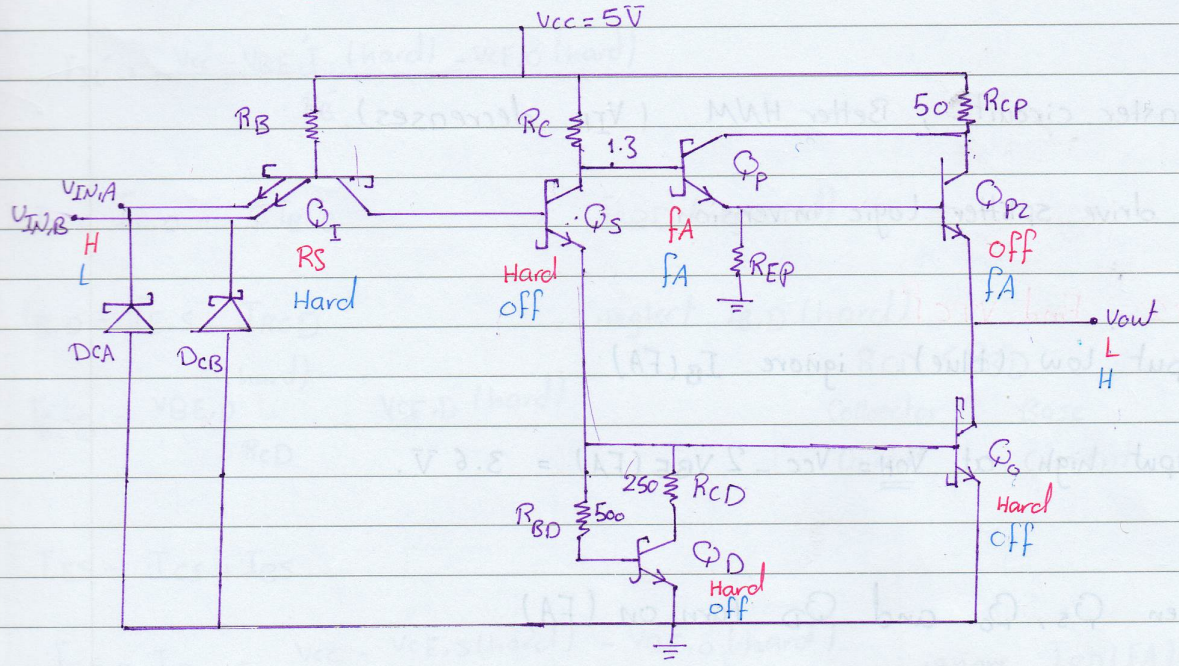
. Q_{SBD} off when input low → Currents = 0
$V_{OH} = V_{CC} = 5\ V$

. When input high such that Q_{SBD} operates in it's hard mode.
$V_{OL} = V_{CE(Hard)} = 0.5\ V$
$LS = 5 - 0.5 = 4.5\ V$
. $V_{IL} = V_{BE(FA)} = 0.7\ V$
. $V_{IH} = I_B R_B + V_{BE(hard)}$, $I_B = \frac{I_C}{\beta_F}$

$I_C = \frac{V_{CC} - V_{CE(hard)}}{R_C}$

30-10-2016
Sunday

CH8: 8.3 schottky Clamped TTL (STTL)



. Assuming Q_P saturates (or hard)

$$V_{BE,P_2}(\hat{P}) + V_{CE,P(sat)} = V_{CE,P_2}$$

$$V_{BE} + V_{CE(sat)} > V_{CE(sat)}$$

$V_{CE,P_2} > V_{CE(sat)} \rightarrow Q_{P_2}$ doesn't saturate
$\rightarrow$ No Q_{SBD} is needed

. Darlington pair, Q_P and Q_{P_2} $\rightarrow$ high speed
$\rightarrow$ high Sourcing current.

. R_{EP}: used as a discharge path for Q_{P_2}

. Delay time drops from 10 nS in TTL to 2nS in STTL.

. Q_D, R_{BD}, R_{CD} $\rightarrow$ squaring network.

. Q_D and Q_0 are designed to operate simultaneously.

. Q_D, R_{BD}, R_{CD} active discharge path for Q_0 and path to ground for Q_S.
. Q_S only operates when Q_D is on, which is only when Q_0 is on.
. Removal of break point.
. Less transmition width.

CH8: 8.3 Shcottky clamped TTL (STTL)

30-10-2016
Sunday

→ Faster circuit , Better H/M (V_{IH} decreases).

Q_S: drive splitter Logic inversion.

Example 8.2: Find VTC?

- input low (blue). ignore I_B(FA)

- Output high at $V_{OH} = V_{CC} - 2V_{BE}(FA) = 3.6\ V$.

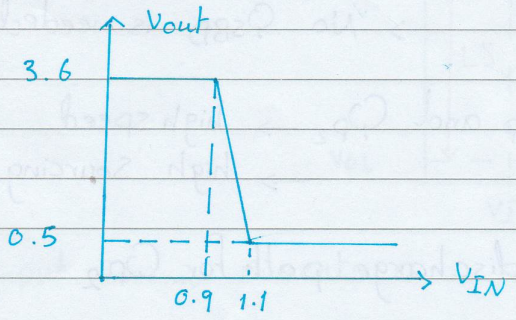
- When Q_S, Q_o and Q_D turn on (FA)

$V_{IL} = -V_{CE,I}(hard) + 2V_{BE}(FA) = 0.9\ V$

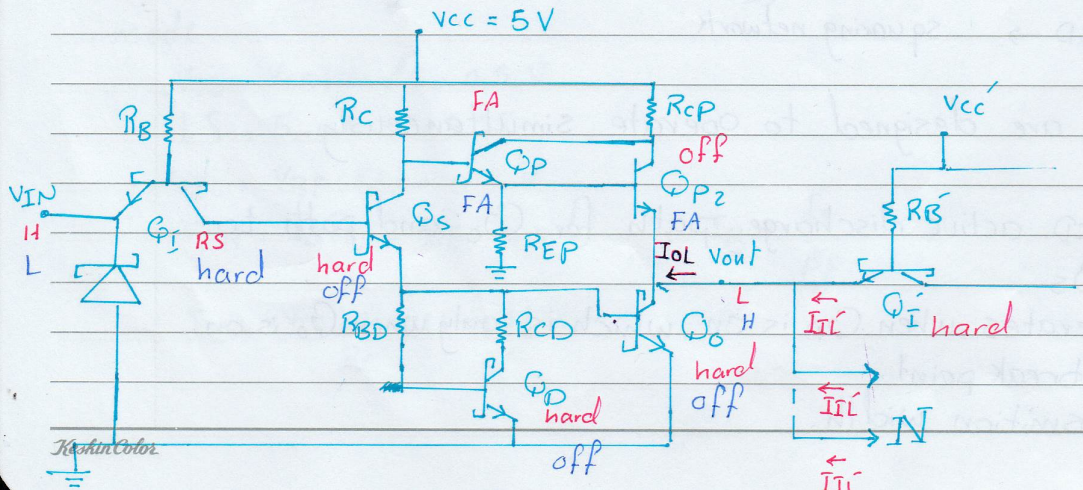
- When Q_S, Q_o and Q_D turn hard

$V_{IH} = -V_{CE,I}(hard) + 2V_{BE}(hard) = 1.1\ V$.

- $V_{OL} = V_{CE,o}(hard) = 0.5\ V$.



CH8: 8.4 STTL Fan_out



1-11-2016
Tuesday

CH8: 8.4 STTL Fan-Out

$$I_{IL}' = \frac{V_{CC} - V_{BE,I}\ (hard) - V_{CE,O}\ (hard)}{R_B}$$

$I_{OL} = I_{C,O} = \beta I_{B,O}$, I_{SBD} (neglected)

$I_{B,O} = I_{E,S} - I_{RCD}$, neglect $I_{B,D}$ (hard)

$$I_{RCD} = \frac{V_{BE,O\ (hard)} - V_{CE,D\ (hard)}}{R_{CD}}$$

$R_{CD} < R_{BD}$

Collector Current Base Current

$I_{ES} = I_{CS} + I_{BS}$

$$I_{CS} = I_{RC} = \frac{V_{CC} - V_{CE,S(hard)} - V_{BE,O\ (hard)}}{R_C}$$, ignore $I_{BP(FA)}$

$$I_{BS} = I_{RB} = \frac{V_{CC} - V_{BC(RS)} - 2V_{BE\ (hard)}}{R_B}$$

$V_{BC(RS)} = V_{SBD} = 0.3\,V$, $N = \frac{I_{OL}}{I_{IL}'}$

Section example: 8.3 $N = 149$

CH8: 8.5 Power Dissipation

- $I_{CC(OL)} \Rightarrow$

$$I_{REP(OL)} = I_{REP} = \frac{V_{CE,S} + V_{BE,O} - V_{BE,P}}{R_{EP}}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE,S(hard)} - V_{BE,O\ (hard)}}{R_C}$$

$$I_{RB(OL)} = \frac{V_{CC} - V_{SBD} - 2V_{BE(hard)}}{R_B}$$

$I_{CC(OL)} = I_{REP} + I_{RC} + I_{RB}$

- $I_{CC(OH)} \Rightarrow$

$I_{REP(OH)} = \frac{V_{CC} - V_{BE,O}}{R_{EP}}$, ignore $I_{BP(FA)} = I_{RC(OH)} \approx 0$, low input.

$$I_{RB(OH)} = \frac{V_{CC} - V_{BE,I\ (hard)} - V_{CE\ (hard)}}{R_B}$$

CH8: 8.5 Power Dissipation

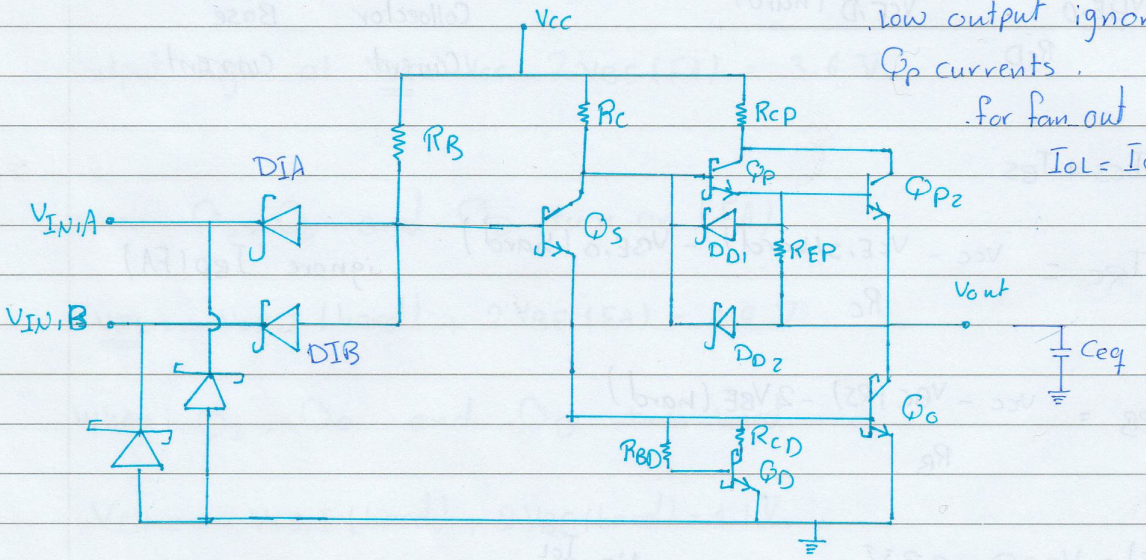
1-11-2016 Tuesday

$I_{CC(OH)} = I_{RCD} + I_{RB(OH)}$

$P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} \cdot V_{CC}$

Example 8.4 = 20.05 mW

CH8: 8.6 Low Power STTL (LSTTL)

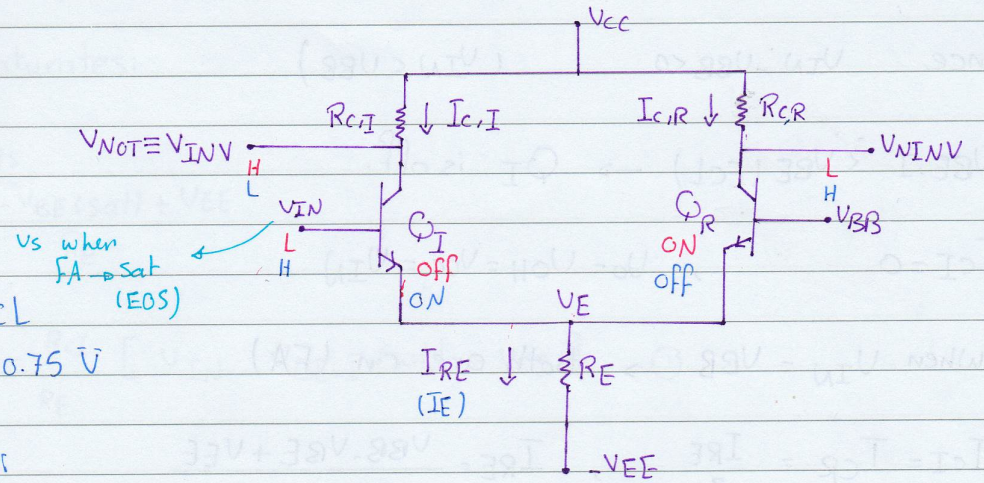


low output ignore Qp currents. for fan out $I_{OL} = I_{C,O}$

QI replaced by DI, no need since Qs does not saturate.

3-11-2016
Thursday

CHAPTER 11: Basic Emitter Coupled logic ECL



. for FA = ECL

. $V_{BE(ECL)} = 0.75\ V$

. In general:

$Q_{ICN} \rightarrow V_E = V_{IN} - V_{BE,I}$

$Q_{RCN} \rightarrow V_E = V_{BB} - V_{BE,R}$, $I_{RE} = \dfrac{V_E + V_{EE}}{R_E}$

$V_{INV} = V_{CC} - I_{c,I} R_{cI}$, $V_{NINV} = V_{CC} - I_{c,R} R_{cR}$

. $V_{IN} < V_{BB}$ such that Q_I off, Q_R on.

V_{NOT} is high $\rightarrow I_{c,I} = 0$

V_{NINV} is low $V_{NINV} = V_{CC} - \cancel{I_{cR}}^{I_E} R_{cR}$

. If $V_{IN} > V_{BB}$, such that Q_I is on, Q_R is off.

. $V_{INV} = V_{CC} - \cancel{I_{cI}}^{I_{RE}} R_{cI}$, Logic Low

. $V_{NINV} = V_{CC}$, Logic high , $I_{cR} = 0$

. CH 11: 11.2 ECL Current switch VTC.

. FA base current will be ignored

. $V_{OH} \rightarrow$

$V_{IN} < V_{BB}$, and V_{BB} is high enough to turn Q_R to FA Region.

$V_E = V_{BB} - V_{BE,R}$ (ECL)

$V_{BE,I} = V_{IN} - V_E = \underbrace{V_{IN} - V_{BB}}_{-Ve} + V_{BE,R}$ (ECL)

CH11: 11.2 ECL (current switch ECL)

3-11-2016 Thursday

. Since $V_{IN} - V_{BB} < 0$ $(V_{IN} < V_{BB})$

$V_{BE,I} < V_{BE(ECL)} \rightarrow Q_I$ is off.

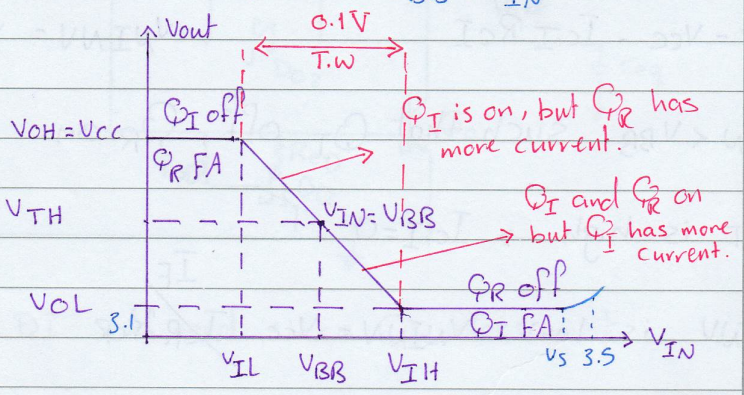
$I_{CI} = 0$, $V_o = V_{OH} = V_{CC} = V_{IN}$

. When $V_{IN} = V_{BB} \rightarrow$ both are on (FA)

. $I_{CI} = I_{CR} = \frac{I_{RE}}{2}$, $I_{RE} = \frac{V_{BB} - V_{BE} + V_{EE}}{R_E}$

. $V_{INV} = V_{NINV} = V_{CC} - \frac{I_{RE}}{2} \cdot R_{CI}$

. for certain values of R_{CI} and $R_{CR} \rightarrow V_{out} = V_{BB} = V_{IN}$.



. V_{IL} and V_{IH}:-
Transition width between OH and OL is equal to 0.1 V. ($T_W = 0.1$ V)

V_{INV} $(V_{IN} > V_S)$
$V_{IN} - V_{BC(sat)} = 3.5 - 0.6$
$= 2.9$ V

. $V_{IL} = V_{BB} - 0.05$, $V_{IH} = V_{BB} + 0.05$

. when $V_{IL} < V_{IN} < V_{BB} \rightarrow Q_R$ is more on than Q_I
. when $V_{BB} < V_{IN} < V_{IH} \rightarrow Q_I$ is more on than Q_R.

. $V_{OL} \rightarrow V_{IN} > V_{BB}$ at $V_{IN} \gtrsim V_{BB} + 0.05 \rightarrow Q_I$ is on.

. $V_E = V_{IN} - V_{BE,I(ECL)}$

. $V_{BE,R} = V_{BB} - V_E = V_{BB} - V_{IN} + V_{BE,I(ECL)} = \cancel{V_{BB}} - \cancel{V_{BB}} - 0.05 + V_{BE(ECL)}$
$= V_{BE} - 0.05 < V_{BE(ECL)}$
$\therefore Q_R$ is off.

$I_{CR} = 0$, $I_{CI} = I_{RE}$
$V_{INV} = V_{OL} = V_{CC} - I_{RE} R_{CI}$, $I_{RE} = \frac{V_{IN} - V_{BE,I(ECL)} + V_{EE}}{R_E}$

$\therefore V_{OL} = V_{CC} - (V_{IN} - V_{BE,I} + V_{EE}) \frac{R_{CI}}{R_E}$

6-11-2016 Sunday

CH 11: 11.2 ECL (current switch ECL)

- When Q_I saturates:

$V_{IN} = V_S$

$$I_{C,I} = \frac{V_S - V_{BE}(sat) + V_{EE}}{R_E}$$

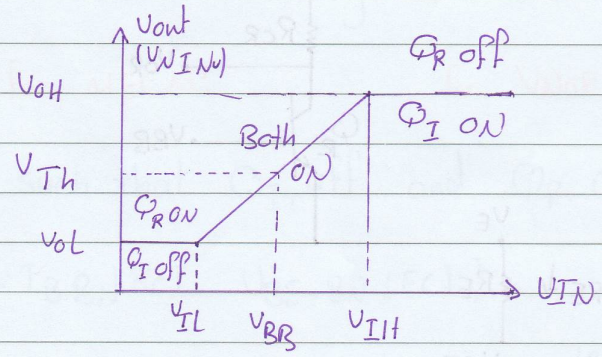
$$V_{INV} = V_{CC} - \frac{R_{CI}}{R_E}\left[V_{IN} - V_{BE,I}(sat) + V_{EE}\right] \quad \cdots (1)$$

$$V_{INV} = V_S - V_{BC}(sat) \quad \cdots (2)$$

Solve for V_{INV} and V_S

$$V_S = \frac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E}\left[V_{BE}(sat) - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$$

for V_{NINV}:



V_{BB} → Constant ; Q_R does not saturate

Example 11.1: $V_{BB} = 2.6\ V$, $R_{CI}, R_{CR}, R_E = 1k$

$V_{CC} = 5V$, $V_{EE} = GND$

$V_{BC}(sat) = 0.6$, $V_{BE}(ECL) = 0.75\ V$

$V_{OH} = 5\ V$

$V_{IL} = 2.6 - 0.05 = 2.55\ V$

$V_{IH} = 2.6 + 0.05 = 2.65\ V$

$$V_{OL} = V_{CC} - \frac{R_{CI}}{R_E}\left(\underbrace{V_{IN}}_{2.65} - V_{BE} + V_{EE}\right) = 3.1\ V$$

$$V_S = \frac{5 + 0.6 + \frac{1k}{1k}\left[0.8 - 0\right]}{1 + \frac{1k}{1k}} = 3.2\ V, \quad V_{INV}(V_S) = 3.2 - 0.6 = 2.6\ V$$

6-11-2016
Sunday

CH11: 11.2 ECL (current switch)

. Advantages of ECL current switch:

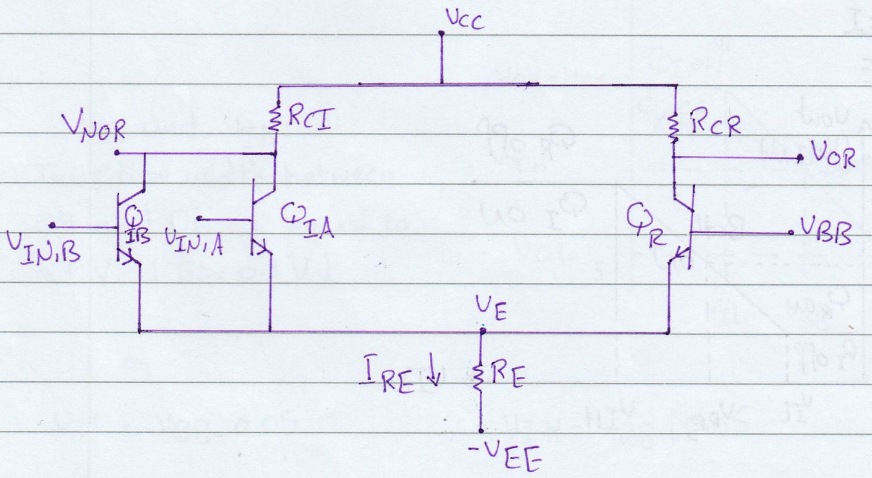
1) low sensitivity to noise, due to the cct's nature as a differential cct, if an external signal interferes, it will be cancelled out.

2) Current drawn from power supply is stable during switching.

3) Two complementary outputs: V_{INV}, V_{NINV}.

4) Outputs are referenced to V_{cc} which can be replaced with GND for more stability.

CH11: 11.4 Basic ECL NOR/OR Gate.



. if Any input is high:

Corresponding input Q is on, Q_R is off, current flows in R_{CI}, V_{NOR} is low, V_{OR} is high.

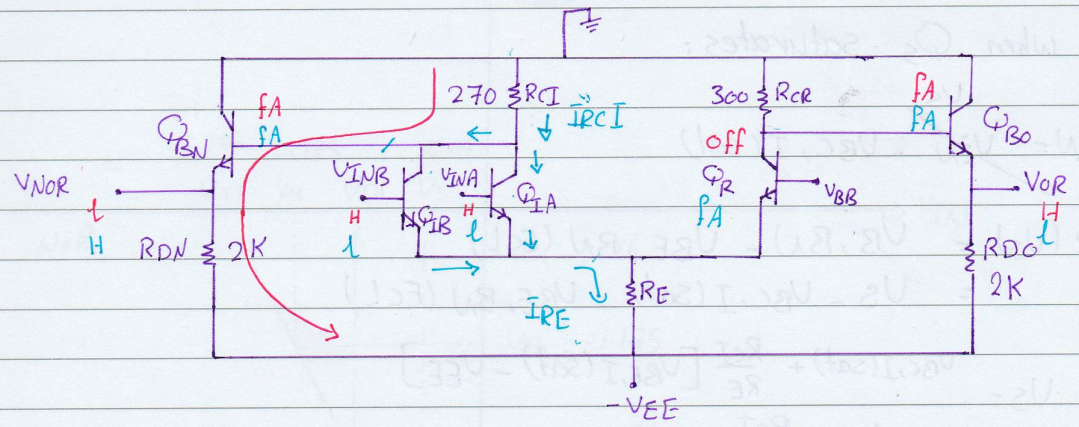
. if All inputs low:

Q_{IA}, Q_{IB} off, Q_R ON → V_{NOR} High, V_{OR} low

A	B	V_{NOR}	V_{OR}
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

CH 11: 11.5 MECL NOR/OR Gate with output buffers

8-11-2016 Tuesday



Advantages: 1) high current (higher fan-out)
2) high switching capabilities → does not saturate.
3) level shifting of output by V_{BE}.

Disadvantages: 1) high current produces high power dissipation
2) Also high current produce large spike due to fast switching.

CH 11: 11.6 VTC for MECM: . for V_{NOR}

. V_{OH}: low input such that Q_I, off and Q_R, ON.

$$V_{NOR} = V_{OH} = 0 - I_{B,BN} R_{CI} - V_{BE,BN(ECL)}$$

To find $I_{B,BN}$:

$$-0 + I_{B,BN} R_{CI} + V_{BE,BN(ECL)} + I_{E,BN(ECL)} R_N - V_{EE} = 0$$

$$I_{E,BN} = I_{B,BN}(\beta+1)$$

$$I_{B,BN} = \frac{V_{EE} - V_{BE(ECL)}}{R_{CI} + (1+\beta_f) R_N}$$

. V_{IL} and V_{IH}: Same as current switch

$$V_{IL} = V_{BB} - 0.05 \quad , \quad V_{IH} = V_{BB} + 0.05$$

. V_{OL}: Q_{IS}, ON and Q_R, off: ignore $I_{B,BN(FA)}$

$$\therefore I_{RCI} = \sum I_{CI} = I_{RE}$$

where $I_{RE} = \dfrac{V_{IN} - V_{BE,I(ECL)} + V_{EE}}{R_E}$

$$V_{NOR} = V_{OL} = -I_{RCI} \cdot R_{CI} - V_{BE,BN(ECL)}$$

CH11: 11.6 VTC for MECL

8-11-2016 Tuesday

. V_S when Q_S saturates:

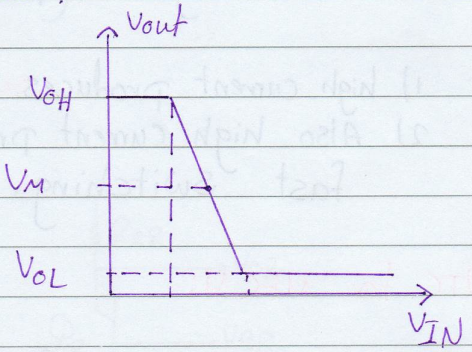
$$V_{B,BN} = V_{IN} - V_{BC,I(sat)}$$

$$V_{NOR}(V_S) = V_{B,BN} - V_{BE,BN}(ECL)$$
$$= V_S - V_{BC,I(sat)} - V_{BE,BN}(ECL)$$

where $$V_S = \frac{V_{BC,I(sat)} + \frac{R_{CI}}{R_E}[V_{BE,I(sat)} - V_{EE}]}{1 + \frac{R_{CI}}{R_E}}$$

. Noise sensitivity: quantity effects of input variations on output.

$$NSH = V_{OH} - V_M$$
$$NSL = V_M - V_{OL}$$



. Noise immunity = $\frac{\text{Sensitivity}}{\text{logic swing}}$

$$N_{IH} = \frac{NSH}{LS}, \quad N_{IL} = \frac{NSL}{LS}, \quad \text{where } LS = V_{OH} - V_{OL}$$

Example 11.2: Find LS, noise margins and noise immunity.

$V_{BB} = -1.175\ V = V_M$
$V_{OH} = -0.76\ V$, $V_{IL} = -1.225\ V$
$V_{IH} = -1.125\ V$, $V_{OL} = -1.55\ V$
$V_S = -0.29\ V$
$LS = -0.76 - (-1.55) = 0.79\ V$
$HNM = -0.76 - (-1.125) = 0.365\ V$
$LNM = -1.225 - (-1.55) = 0.325\ V$

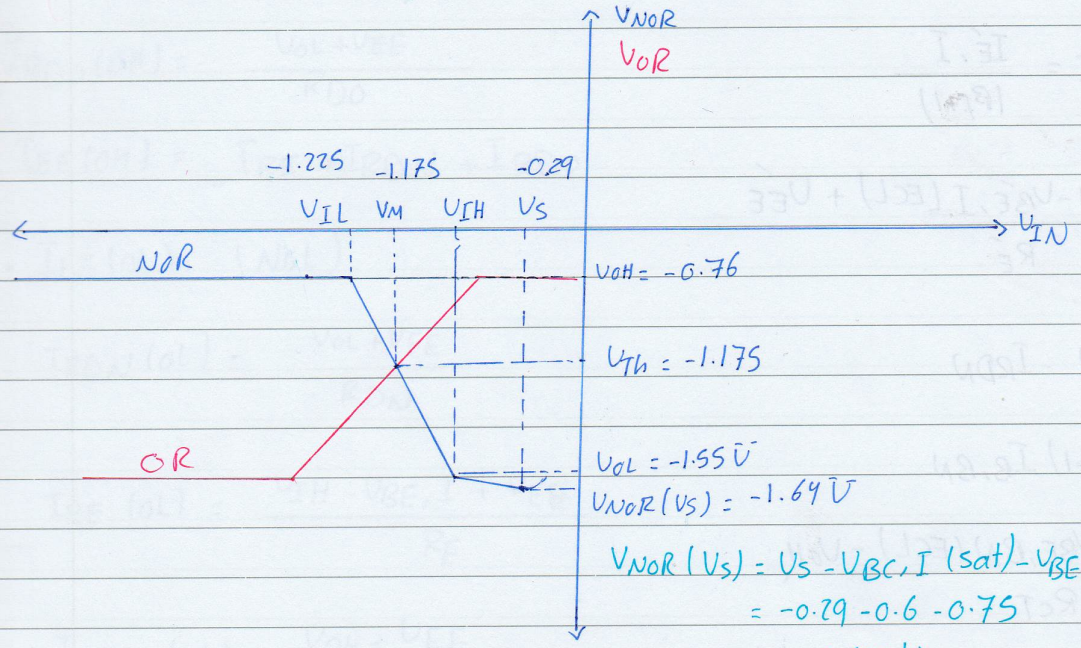
. Noise margins are low, but not a problem since logic swing is small.

$$NIH = \frac{-0.76 - (-1.175)}{0.79} = 0.53\ V$$

$$NIL = \frac{-1.175 - (-1.55)}{0.79} = 0.475\ V$$

10-11-2016 Thursday

CH11: 11.6 VTC for MECL



$$V_{NOR}(V_S) = V_S - V_{BC,I}(sat) - V_{BE,BN}(ECL)$$
$$= -0.29 - 0.6 - 0.75$$
$$= -1.64\ V$$

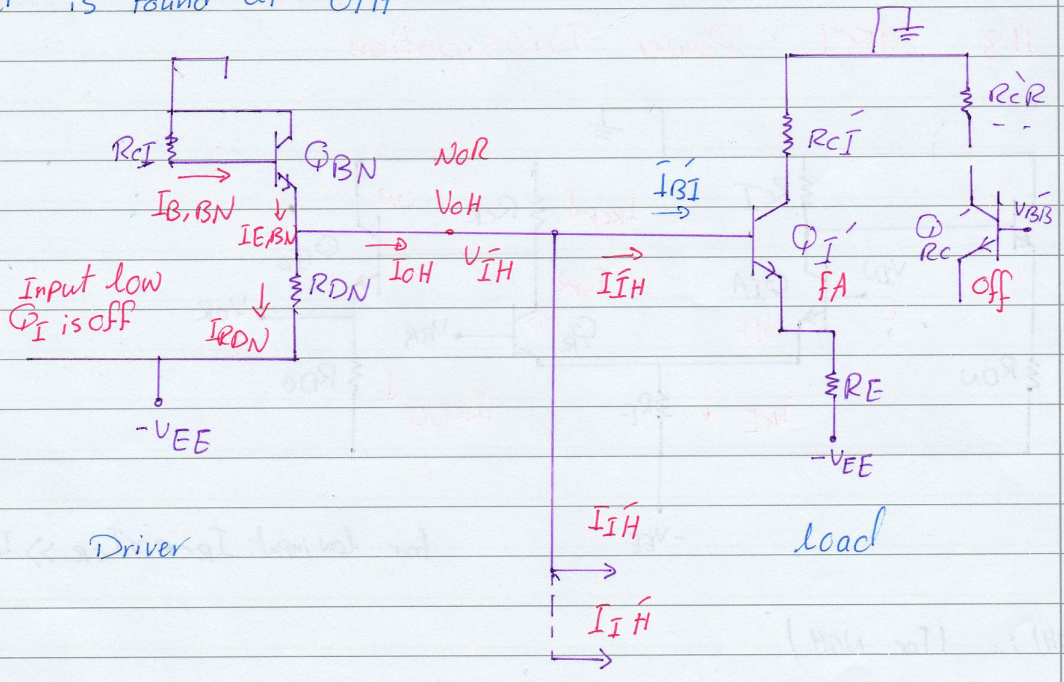
CH11: 11.7 MECL I Fan_out

Output at NOR Driver, input at Q_I'.

if input is low, Q_I' is off and $I_I' = 0$

↳ Fan_out can't be found at O/L.

↳ Fan_out is found at O/H



$$N = \frac{I_{OH}}{I_{IH}'}$$

CH11: 11.7 MECL Fan Out

10-11-2016 Thursday

$$I_{IH} = I_{B'} , I = \frac{I_{E'} , I}{(\beta_F + 1)}$$

$$I_{E'} , I = \frac{V_{OH} - V_{BE'} , I (ECL) + V_{EE}}{R_{E'}}$$

$$I_{OH} = I_{E} , _{BN} - I_{RDN}$$

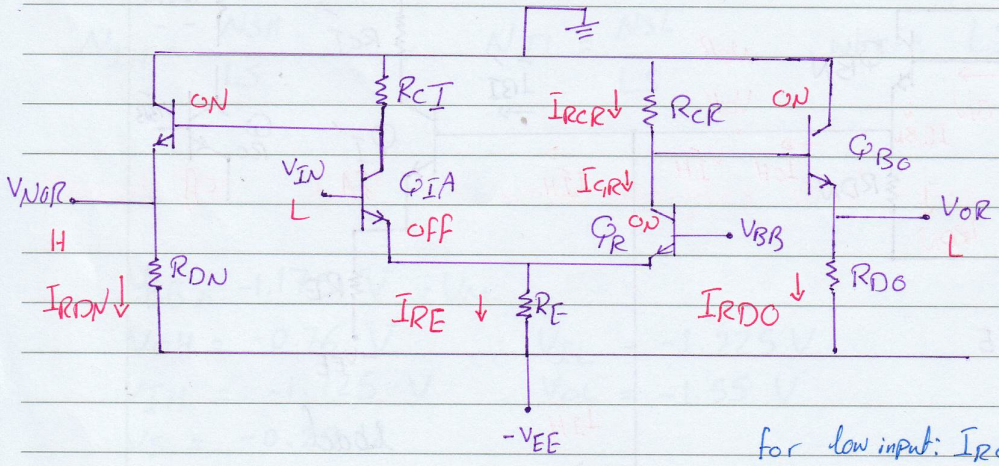
$$I_{E,BN} = (\beta_F + 1) I_{B,BN}$$

$$I_{B,BN} = \frac{0 - V_{BE,BN} (ECL) - V_{OH}}{R_{CI}}$$

$$I_{RDN} = \frac{V_{OH} + V_{EE}}{R_{DN}}$$

- unlike TTL, where the driver output sinks the load current and thus doesn't affect the output's voltage, the ECL's load drags current from the ECL's driver, which decreases the O/p's voltage as load gates increase

CH11: 11.8 MECL Power Dissipation



for low input: $I_{RCR} \simeq I_{CR} \gg I_{B,BO}$

$I_{EE(OH)}$: (for NOH)

$$I_{RE(OH)} = \frac{V_{BB} - V_{BE,R} + V_{EE}}{}$$

$$I_{RDN(OH)} = \frac{V_{OH} + V_{EE}}{R_{DN}}$$

CH11: 11.8 MECL Powe Dissipation

13-11-2016 Sunday

$$I_{RDO(OH)} = \frac{V_{OL} + V_{EE}}{R_{DO}}$$

$$I_{EE(OH)} = I_{RE} + I_{RDN} + I_{RDO}$$

- $I_{EE(OL)}$: (NOL)

$$I_{RDN(OL)} = \frac{V_{OL} + V_{EE}}{R_{DN}}$$

$$I_{RE(OL)} = \frac{V_{IH} - V_{BE,I} + V_{EE}}{R_E}$$

$$I_{RDO(OL)} = \frac{V_{OH} + V_{EE}}{R_{DO}}$$

$$I_{EE(OL)} = \Sigma I$$

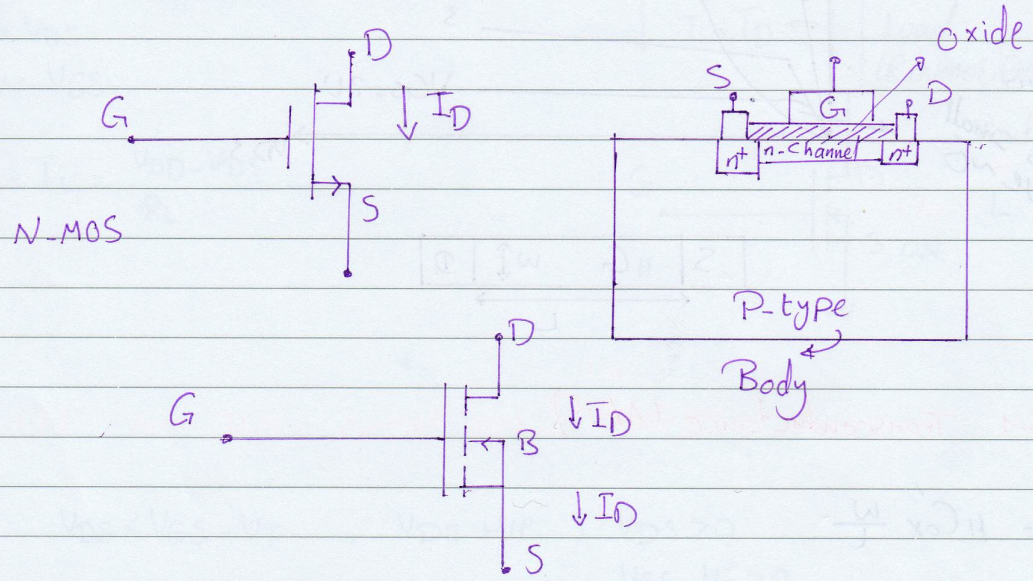
- $$P_{EE} = V_{EE} \frac{I_{EE(OH)} + I_{EE(OL)}}{2}$$

CHAPTER 16 METAL oxide semi-conductor FETs

15-11-2016 Tuesday

CH16: 16.3 MOSFET modes of operation.

. N-channel MOSFET.



. Threshold voltage (VT)

→ $V_{GS} > V_{TN}$ for an electrical channel to be induced between Drain and Source.

. Enchancment V_{TN} , +Ve
. depletion V_{TN} , -Ve

1) Cut off $V_{GS} < V_{TN}$, $I_D = 0$ → MOSFET is off.

2) Linear Mode $V_{GS} \geq V_{TN}$, $V_{DS} < V_{DS(sat)}$

$V_{DS} < V_{GS} - V_{TN}$

$$I_D(Lin) = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

k → Transconductance parameter

3) Saturation Mode

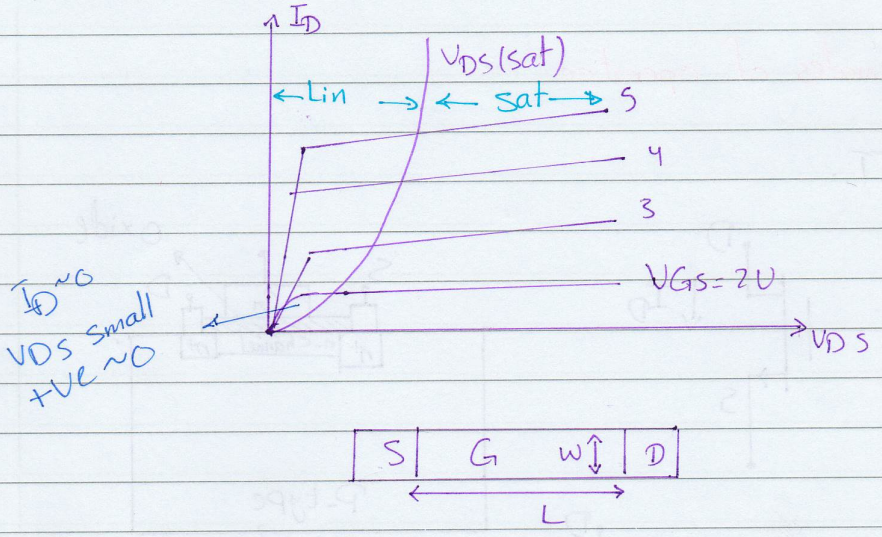
$V_{GS} \geq V_{TN}$

$V_{DS} \geq V_{DS(sat)}$ → $V_{DS} \geq V_{GS} - V_{TN}$

$$I_{DS(sat)} = \frac{k}{2}(V_{GS} - V_T)^2$$

15-11-2016
Tuesday

CH16: 16.3 MOSFET Modes of operation.



CH16: 16.4 Transconductance (A/V^2)

$$K_n = \mu C_{ox}' \frac{W}{L}$$

μ: mobility for electrons

C_{ox}: Capacitance for oxide

$$C_{ox}' = \frac{\varepsilon_{ox} \rightarrow \text{permettivity}}{t_{ox} \rightarrow \text{thickness}} \quad \Big| \text{ oxide}$$

CH16.6: P-Channel MOSFET.

V_{TP}: Enchancement -Ve
Depletion +Ve

1) Cut-off: $V_{G,P} \leq -V_{TP}$

$$I_D = 0$$

2) Linear $V_{SG,P} \geq -V_{TP}$

$V_{SD,P} < V_{SG} + V_{TP}$

$$I_{D,P}(Lin) = k_P \left[(V_{SG,P} + V_{TP}) V_{SD,P} - \frac{V_{SD,P}^2}{2} \right]$$

$\frac{V_{SD,P}^2}{2} \rightarrow V_{SD,P}(sat)$

3) Saturation: $V_{SG,P} \geq V_{T,P}$, $V_{SD,P} \geq (V_{SG,P} + V_{TP})$

$$I_{D,P}(sat) = \frac{k_P}{2} (V_{SG,P} + V_{TP})^2$$

15-11-2016
Tuesday

CHAPTER 17 Introduction to MOS Digital ccts

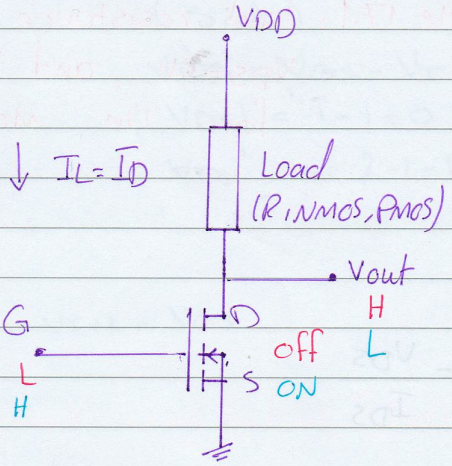
CH 17: 17.1 General NMOS Inverter

for Linear:-

$V_o = V_{DS}$

$V_{IN} = V_{GS}$

$$I_D = I_L = \frac{V_{DD} - V_{DS}}{R_L}$$



CH 17 : 17.2 Zero Drain current active (Lin) MOSFET

- $V_{DS} < V_{GS} - V_T$, V_{DS} +ve , $V_{DS} > 0$

  $V_{GS} - V_T > 0$

  $V_{GS} > V_T \rightarrow$ Active

  ($V_{DS} < V_{DS(sat)}$)

* Prove analytically :-

$$I_{D(Lin)} = K\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$V_{DS} = 0 \rightarrow I_D = 0$

$V_{DS} = 2(V_{GS} - V_{TN})$ X NOT Applicable because V_{DS} can't be higher than $V_{DS(sat)}$

- For high V_{GS}, Low V_{DS} and proper load, NMOS is used as a pull down cct.

CH17: 17.2 Zero Drain current active MOSFET

17-11-2016
Thursday

Example 17.1: find resistance of D-S channel (R_{DS}) if $V_{DS}=3V$, and $V_{DS}=0$, $V_T=1V$, $K=40\ \mu A/V^2$ for Lin Mode.

$$R_{DS}=\frac{V_{DS}}{I_{DS}}$$

$$I_D(lin)=K\left[(V_{GS}-V_{TN})V_{DS}-\frac{V_{DS}^2}{2}\right]$$

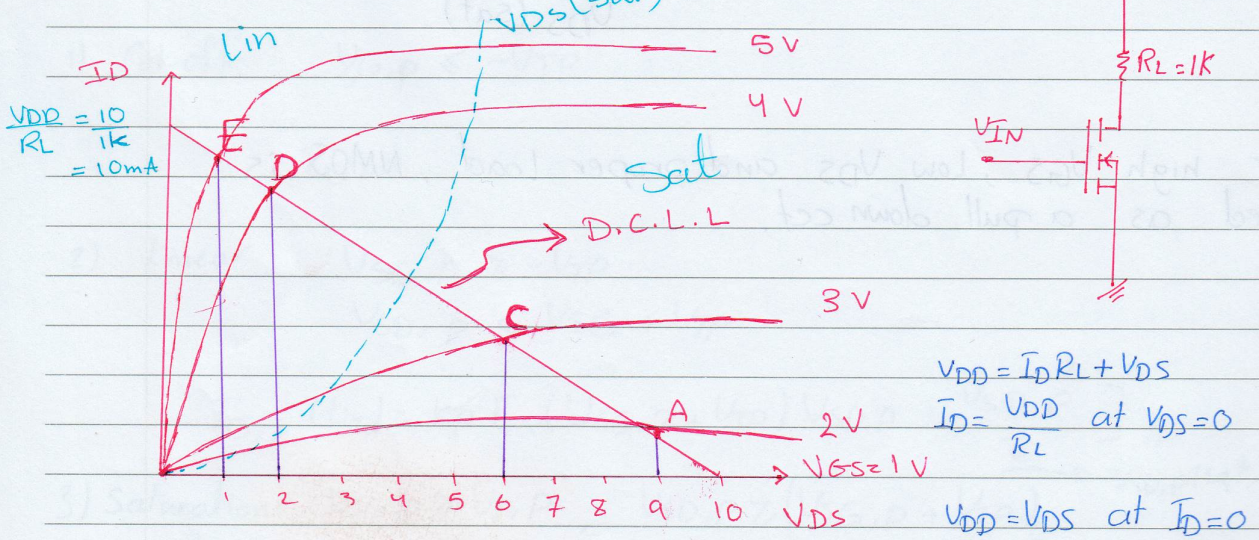
$$R_{DS}=\frac{dV_{DS}}{dI_{DS}}\ ,\quad \frac{dI_{DS}}{dV_{DS}}=K(V_{GS}-V_{TN}-V_{DS})$$

$$R_{DS}=\frac{1}{K(V_{GS}-V_{TN}-V_{DS})}=\frac{1}{40\mu(5-1-3)}=25\ K\Omega$$

$$R_{DS}\Big|_{V_{DS}=0}=6.25\ K\Omega$$

- As V_{DS} decreases, R_{DS} decreased, conductivity increased, which is useful for NMOS as a pull down device.

Example17.2: Draw VTC for the given I-V MOSFET curve $V_{DD}=10V$, $R_L=1K$.



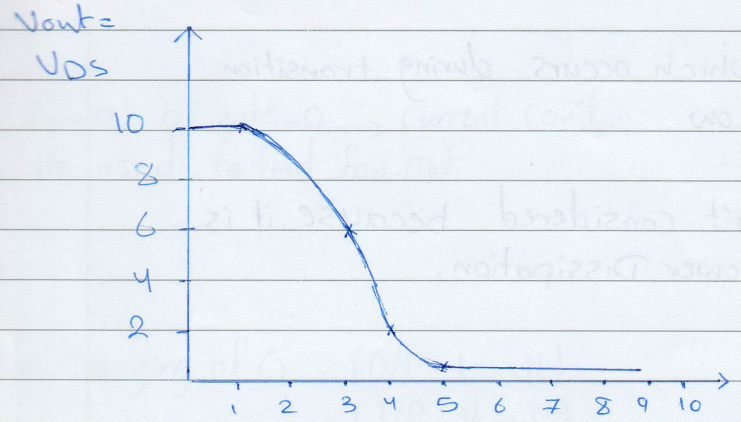
$V_{DD}=I_DR_L+V_{DS}$

$I_D=\frac{V_{DD}}{R_L}$ at $V_{DS}=0$

$V_{DD}=V_{DS}$ at $I_D=0$

17-11-2016
Thursday

CH17 : 17.2 Zero_Drain current active MOSFET



(sat)

$V_{DS} = V_{GS} - V_T$

$V_{DS1} = 1-1 = 0$

$V_{DS_2^1} = 2-1 = 1$

. Prove that V_{DS} equals the values in graph using $I_D(Lin)$, $I_D(sat)$

* for A,B,C use $I_{D(sat)} = \frac{K}{2}[V_{GS} - V_T]^2$

$$V_{DS} = V_{DD} - I_D R_L$$

* for D,E use $I_D(Lin) = K\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$

$V_{DS} = V_{DD} - I_D R_L$
↳ solve for I_D and V_{DS}

Example 17.4: Partial differential of an NMOS I_D Expression.

$$I_D(Lin) = K\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$d\underset{V_{out}}{I_D}(\underset{V_{in}}{V_{GS}}, V_{DS}) = \frac{\partial I_{DS}}{\partial V_{GS}} dV_{GS} + \frac{\partial I_D}{\partial V_{DS}} dV_{DS}$$

$\frac{\partial I_{DS}}{\partial V_{GS}} \rightarrow dV_{IN}$; $\frac{\partial I_D}{\partial V_{DS}} \rightarrow dV_{out}$

$$\frac{\partial I_D}{\partial V_{GS}} = KV_{DS} \quad , \quad \frac{\partial I_D}{\partial V_{DS}} = K(V_{GS} - V_T - V_{DS})$$

$$dI_D = KV_{DS}\,dV_{GS} + K(V_{GS} - V_T - V_{DS})\,dV_{DS}$$

CH17:

~~Example~~ 17.6 : Power Dissipation

* Static power Dissipation

$$P_{DD\,(static)\,(avg)} = \frac{I_{DD(OH)} + I_{DD(OL)}}{2} V_{DD}$$

CH17: 17.6 Power Dissipation

17-11-2016
Thursday

* Dynamic power Dissipation, which occurs during transition between O/p high and O/p Low

* for BJT this power wasn't considered because it is small compared to static power Dissipation.

$$P_{D,dyn} = C_L \, V \, V_{DD}^2$$

C_L: Capacitance of load "f"

V: switching frequency "Hz"

Example 17.5: $V_{DD} = 5V$, $V = 0.5MHZ$, $C_L = 10pF$

$I_{DD(OH)} = 5\mu A$, $I_{DD(OL)} = \#\ 100\ \mu A$

find total P_{DD}?

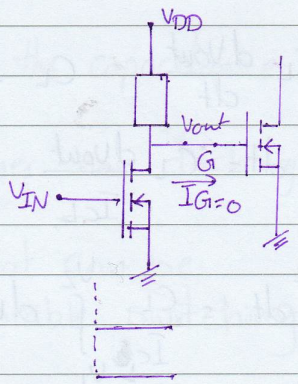
$$P_{DD,st} = \frac{100\mu + 5\mu}{2} \times 5 = 262\ \mu W$$

$$P_{DD,dy} = 10p \times 0.5M \times 25 = 125\ \mu W$$

$$P_{tot} = 262 + 125 = 387\ \mu W$$

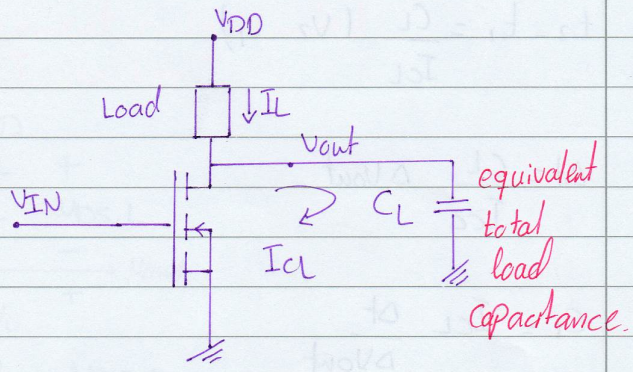
20-11-2016
Sunday

CH17: 17.7 Fan_Out.



. Current at gate = 0 → current can't be used to find fan_out

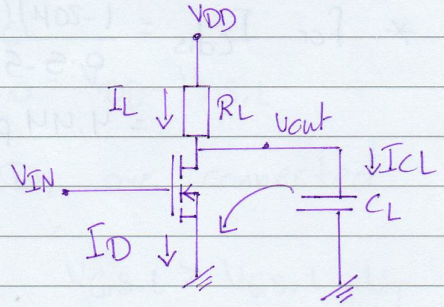
1) Charging of C_L (O/P L → H)
(I/P H → L)



NMOS is off and 100% of I_L charges load capacitance.

$$I_L = I_{CL} = \frac{C\,dV_{CL}}{dt} = \frac{C\,dV_{out}}{dt}$$

2) Discharging (O/P H → L)
(I/P L → H)



$$I_{CL} = I_L - I_D \quad , \; I_D > I_L$$
$$= -C_L \frac{dV_{out}}{dt}$$

. Fan_Out depends on load capacitance which affect propagation delay.

. Time required for switching between high and low depends on C_L

Example 17.6: find C_L, $I_{CRG} = 50\,\mu A$, $I_{Dis} = -20\,\mu A$
$\Delta t = 1\,\mu S$, $V_{OL} = 0.5\,V$, $V_{OH} = 5\,V$

CH17: 17.7 Fan-Out

20-11-2016
Sunday

$$I_{CL} = C_L \frac{dV_{out}}{dt} = C_L \frac{\Delta V_{out}}{\Delta t}$$

or $dt = C_L \frac{dV_{out}}{I_{CL}}$, I_{CL} varies between charging and dis., Assume Const. for simplicity

$$\int_{t_1}^{t_2} dt = \frac{C_L}{I_{CL}} \int_{V_1}^{V_2} dV_{out}$$

$$t_2 - t_1 = \frac{C_L}{I_{CL}} (V_2 - V_1)$$

$$\Delta t = \frac{C_L}{I_{CC}} \Delta V_{out}$$

$$C_L = I_{CL} \frac{\Delta t}{\Delta V_{out}}$$

* for $I_{CRG} = 50\,\mu A$

$$C_L = \frac{50(1\mu)}{5-0.5} = 11.1\,pF$$

* for $I_{Cdis} = \frac{(-20\mu)(1\mu)}{0.5-5}$

$$= 4.44\,pF$$

- If we choose $C_L = 11.1\,pF$

$$\Delta t|_{ch} = \frac{C_L}{I_{CL}} \Delta V_{out} = 1\,\mu s$$

$$\Delta t|_{dis} = \frac{11.1}{-20}(-4.5) = 2.5\,\mu s > 1\,\mu s$$

↳ we can't use $C_L = 11.1\,pF$ since discharging needs time higher than $\Delta t = 1\,\mu s$

↳ Try $4.44\,pF$: $\Delta t|_{ch} = \frac{4.44p(4.5)}{50\mu} < 1\,\mu s$

$$\Delta t|_{dis} = \frac{4.44p(-4.5)}{-20p} = 1\,\mu s \quad \therefore \text{Choose } C_L = 4.44\,pF$$

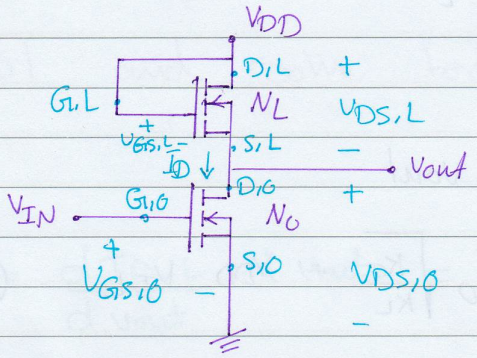
22-11-2016 Tuesday

* High to Low transmition Limits the value of the capacitance.

* Obvious, Since charging current is higher than discharging.

fan_Out:- The Max Load capacitance that can be driven and Maintain an acceptable switching time.

CHAPTER 19: Saturated Enchancement_only Loaded NMOS_Inverter



$V_{IN} = V_{GS,O}$

$V_{out} = V_{DS,O} = V_{DD} - V_{DS,L}$

* GL and D_L are connected $V_{GS,L} = V_{DS,L}$

$V_{GS,L} > V_{GS,L} - V_T$

$V_{DS,L} > V_{GS,L} - V$ → N_L is saturating.

$V_{DS,L(sat)}$

CH19: 19.1-19.3 VTC of E_Only NMOS Inverter

$V_{IN} = V_{GS,O} < V_{T,O}$, NMOS → cut_off

$I_{D,O}(off) = 0 = I_{D,L}(sat) = \frac{K_L}{2}(V_{GS} - V_{T,L})^2$

$V_{GS,L} = V_{T,L} = V_{DS,L}$

$V_{out} = V_{DD} - V_{DS,L} = V_{DD} - V_{T,L} = V_{OH}$

22-11-2016
Tuesday

- V_I :

$$V_{IN} = V_{GS,0} = V_{T,0} = V_{I,L}$$

↳ low

- when $V_{IN} = V_{GS,0} > V_{T,0}$ → both transistors are in sat. region
Find V_{out} as function of V_{IN}, $I_{D,L}(sat) = I_{D,0}(sat)$.

$$I_{D,L}(sat) = I_{D,0}(sat)$$

$$\frac{K_L}{2}(V_{GS,L} - V_{T,L})^2 = \frac{K_0}{2}(V_{GS,0} - V_{T,0})^2$$

$$V_{GS,0} = V_{IN}$$

$$V_{GS,L} = V_{DS,L} = V_{DD} - V_{out}$$

$$V_{out} = -\sqrt{\frac{K_0}{K_L}}\, V_{in} + V_{T,0}\sqrt{\frac{K_0}{K_L}} + V_{DD} - V_{T,L} \quad \cdots (1)$$

* The larger $\sqrt{\frac{K_0}{K_L}}$ → the steeper the transition.

* Middle pt V_M :
when $V_{IN} = V_{out} = V_M$ → both sat

in eq(1) substitute for V_{IN} and V_{out} with V_M.

$$V_M = \frac{\left(V_{DD} - V_{T,L} + V_{T,0}\frac{\sqrt{K_0}}{\sqrt{K_L}}\right)}{1 + \sqrt{\frac{K_0}{K_L}}}$$

- V_{IH} at $\frac{dV_{out}}{dV_{in}} = -1$

$N_0 \rightarrow$ Lin , $N_L \rightarrow$ sat

$$I_{D,0}(Lin) = K_0\left[(V_{GS} - V_{T,0})V_{DS,0} - \frac{V_{DS,0}^2}{2}\right]$$

$$V_{GS,0} = V_{IN} \quad , \quad V_{DS,0} = V_{out}$$

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$$I_{D,0}(lin) = K_0 \left[(V_{IN} - V_{T,0}) V_{out} - \frac{V_{out}^2}{2} \right] \quad \ldots (2)$$

$$I_{D,L}(sat) = \frac{K_0}{2} \left[V_{DD} - V_{out} - V_{T,L} \right]^2 \quad \ldots (3)$$

$$d I_{D,L} = \frac{d I_{D,L}}{d V_{out}} d V_{out} \quad \ldots (4) \; (6)$$

$$d I_{D,0} = \frac{d I_{D,0}}{d V_{IN}} d V_{IN} + \frac{d I_{D0}}{d V_{out}} d V_{out} \quad \ldots (5)$$

Set [5] = [6] and solve for $\frac{d V_{out}}{d V_{in}}$

$$\frac{d I_{D0}}{d V_{IN}} d V_{IN} = \frac{d I_{D,L}}{d V_{out}} d V_{out} - \frac{d I_{D,0}}{d V_{out}} d V_{out}$$

$$\frac{d V_{out}}{d V_{in}} = \frac{d I_{D,0}}{d V_{IN}} \Big/ \left[\frac{d I_{D,L}}{d V_{out}} - \frac{d I_{D,0}}{d V_{out}} \right]$$

After deriving $\rightarrow = -1$

$$V_{out}(V_{IH}) = \frac{K_0 (V_{IH} - V_{T,0}) + K_L (V_{DD} - V_{TL})}{2K_0 + K_L}$$

* for another relation between V_{IH} and $V_0(V_{IH})$

Set $I_{D,L}(sat) = I_{D,0}(Lin)$
and solve For V_{IH} also Substitude for $V_0(V_{IH})$ from eq (6)

$$V_{IH} < V_{T,0} + \frac{2(V_{DD} - V_{T,L})}{\sqrt{\frac{3K_0}{K_L}} + 1}$$

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- V_{OL}, N_L (sat), N_0 (lin)

$I_{D,L}$ (sat) = $I_{D,0}$ (lin)

$V_{GS,0} = V_{IN} = V_{OH} = V_{DD} - V_{TL}$

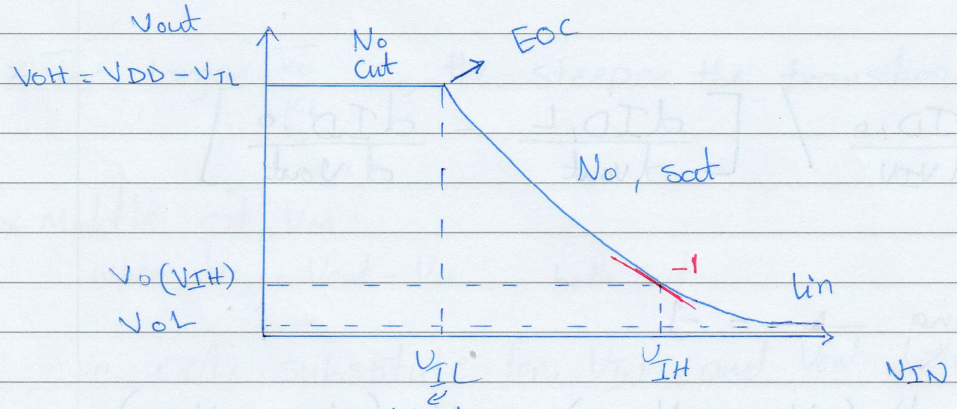
$V_{DS,0} = V_{OL}$

$V_{GS,L} = V_{DD} - V_{OL}$

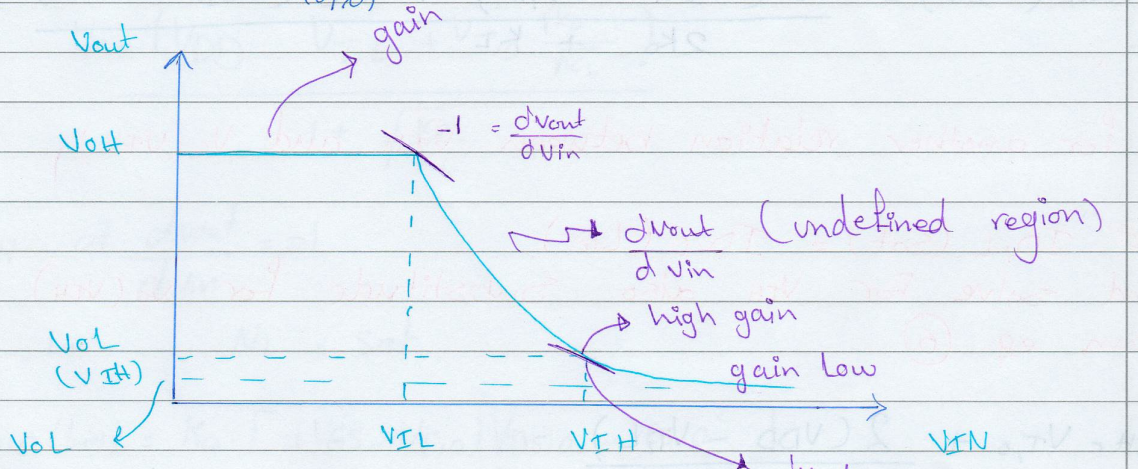
$$\Rightarrow V_{OL} = \frac{K_L (V_{DD} - V_{TL})^2}{2K_L (V_{DD} - V_{TL}) + 2K_0 (V_{DD} - V_{T,L} - V_{T,0})}$$

- $LNM = V_{IL} - V_0(IH)$
- $HNM = V_{OH} - V_{IH}$

$V_0(V_{IL})$



$(V_{T,0})$



In general

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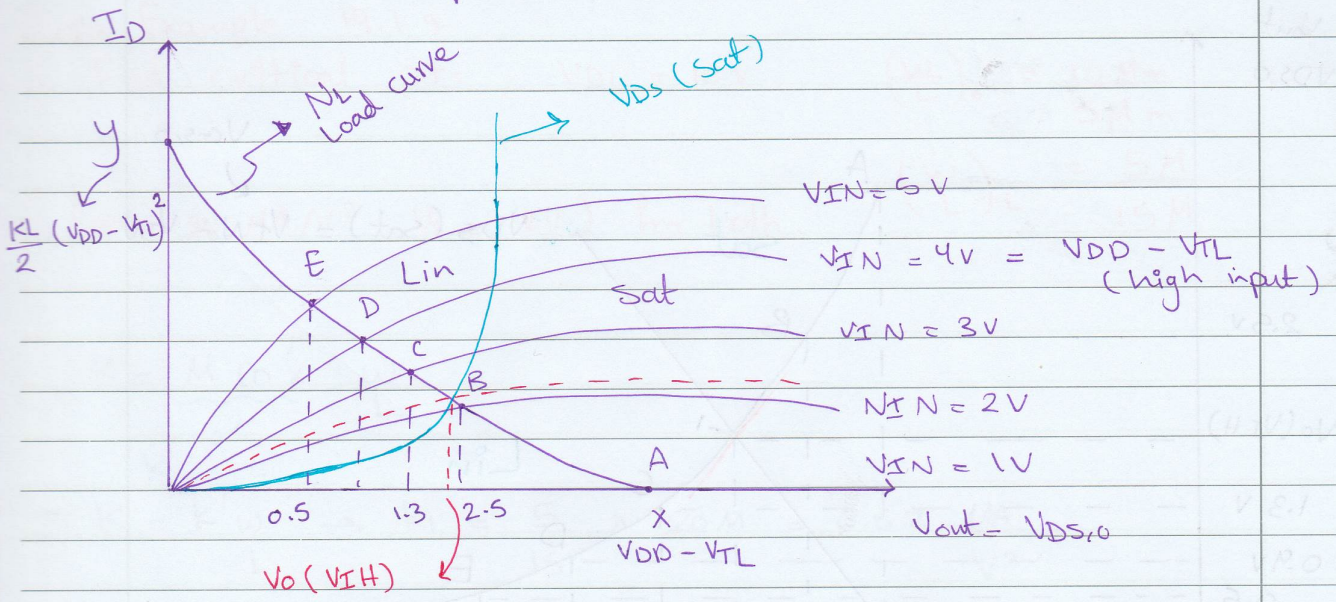
• Graphical solution



$V_{DS}(sat) = V_{GS} - V_T$

$V_{out} = V_{DD} - V_{DSL}$

$= V_{DD} - V_{GS,L}$

↝ $V_{DSL} = V_{GSL}$

$V_{out} = V_{DD} - V_{TL}$

V_{OL} ↵

• at y ⇒

$V_{DS,0} = 0$

$I_{D,L}(sat) = \frac{K_L}{2}(V_{GSL} - V_{TL})^2$

$V_{GS,L} = V_{DSL} = V_{DD} - V_{out} = V_{DD} - V_{DS,0}$ (0)

∴ $V_{GS,L} = V_{DD}$

$I_{D,L} = \frac{K_L}{2}(V_{DD} - V_{TL})^2$

• at X ⇒

$I_{D,L}(sat) = 0 = \frac{K_L}{2}(V_{GSL} - V_{TL})^2 = 0$

→ $V_{GS} = V_{TL}$

V_{OL}: $V_{IN} = V_{OH} = V_{DD} - V_{TL}$

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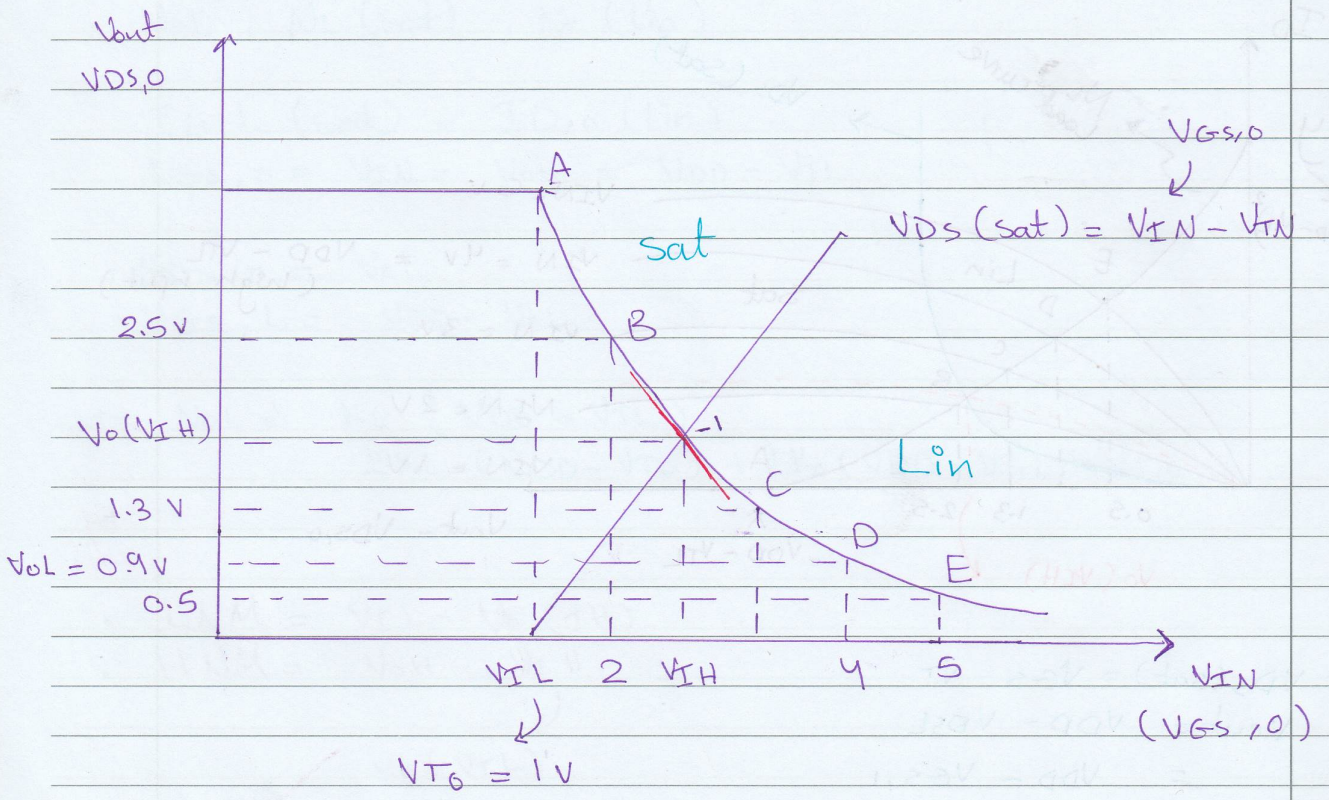

CH "19" ⇒ 19.5 Power Dissipation

$$P_{DD,stat} = \frac{I_{DD(oH)} + I_{DD(oL)}}{2} \cdot V_{DD}$$

⇒ $I_{DD(oH)}$ ↝ input low ↝ NL sat ↝ No off

$$I_{DL} = I_{DN} = 0 = I_{DD(oH)}$$

⇒ $I_{DD(oL)}$, input high ↝ NL sat → No lin

$$I_{DD(oL)} = I_{DL(sat)} = I_{D0(lin)} = K_0 \left[(V_{GS,0} - V_{T0}) V_{DS0} - \frac{V_{DS0}^2}{2} \right]$$

$$P_{DD,Dyn} = C_L V V_{DD}^2$$

- read example 19.3 &-

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⇒ Example 19.1 &
Find critical pts, $V_{DD} = 10\,V$, $\left(\frac{W}{L}\right)_0 = \frac{10\,\mu m}{5\,\mu m}$

$(k' = 20\,\mu A/V^2, V_t = 1.2\,V)$ for both. $\left(\frac{W}{L}\right)_L = \frac{5\,\mu}{15\,\mu}$

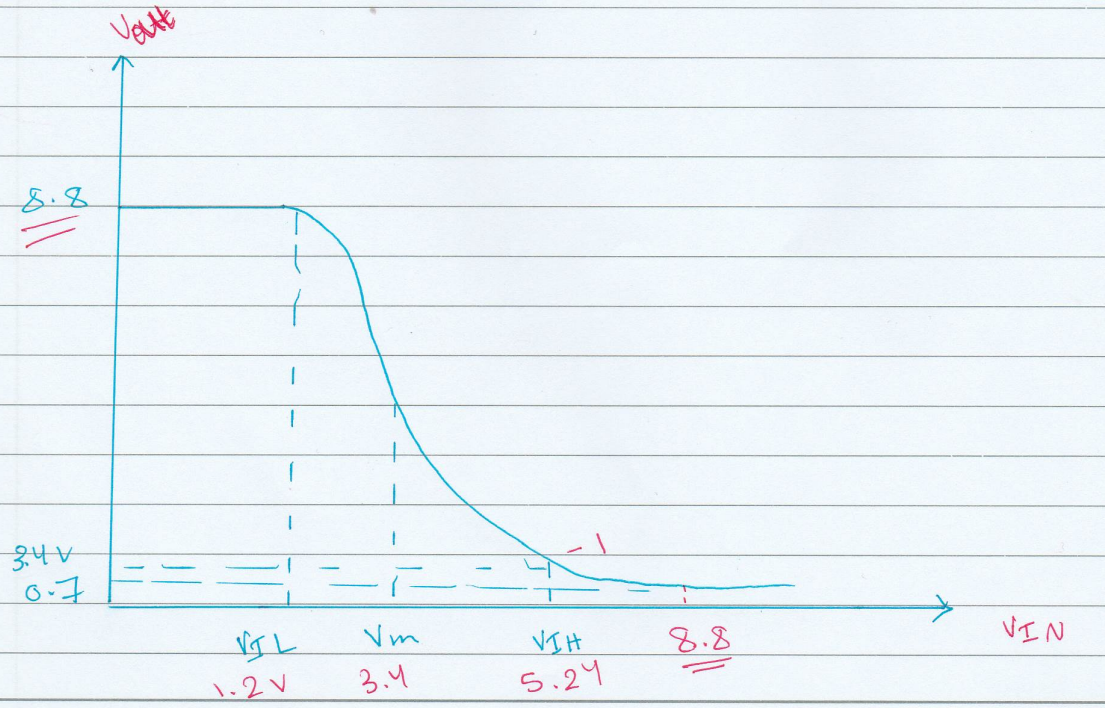
$$K = \underbrace{\mu C_{ox}'}_{k'} \frac{W}{L}$$

$$K = k'\frac{W}{L} \rightarrow K_L = \frac{5}{15} \times 20\,\mu = 6.67\,\frac{\mu A}{V^2}$$

$$K_0 = \frac{10}{5} \times 20 = 40\,\frac{\mu A}{V^2}$$

$$\frac{K_0}{K_L} = \frac{40}{6.67} = 6$$

$V_{oH} = 10 - 1.2 = 8.8\,V$; $V_{IL} = V_{T,0} = 1.2\,V$
$V_{oL} = 0.71\,V$, $V_{IH} = 5.24\,V$
$V_{out}(V_{IH}) = 2.25\,V$, $V_M = 3.4\,V$



CHAPTER 23

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Sunday

CHAPTER 23: 23.1+23.4 CMOS Inverter / VTC

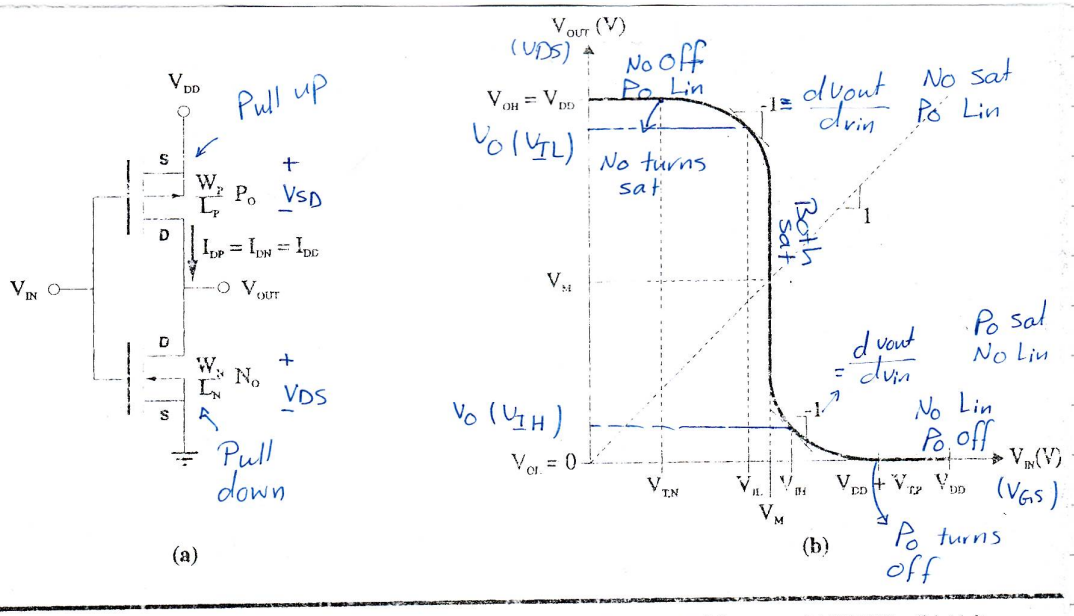

FIGURE 23.1 CMOS Inverter: (a) Circuit with complementary NMOS and PMOS output MOSFETs, (b) Voltage transfer characteristic

→ P_O turns off when:-

$$V_{SG} \leq -V_{TP}$$

$$V_{DD} - V_{IN} \leq V_{TP} \rightarrow V_{IN} \geq V_{DD} + V_{TP}.$$

→ V_{OH}

$$V_{IN} = V_{GS} = 0 \quad , \quad V_{GS} < V_{TN}$$

→ N_O is off

$$V_{SG} = V_{DD} - \cancel{V_{IN}^{0}} = V_{DD} > -V_{TP}$$

$$V_{SDP} < V_{SGP} + V_{TP} \rightarrow P_O \text{ is Lin}$$

$$I_{DN}(off) = I_{DP}(Lin) = k_P \left[(V_{SG} + V_{TP}) V_{SDP} - \frac{V_{SDP}^2}{2} \right]$$

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$V_{SDP} = 0$

$V_{out} = V_{DD} - V_{SDP}$

$\star\ V_{OH} = V_{out} = V_{DD}$

→ V_{OL} : $V_{IN} = V_{DD} \Rightarrow$ N_O is Linear

for P_O: $V_{SG} = V_{DD} - V_{IN} = V_{DD} - V_{DD} = 0 < -V_{TP}$

$\Rightarrow$ P_O is off

$I_{DP}(off) = I_{DN}(lin) = 0$

$K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right] = 0 \rightarrow V_{DSN} = 0$

$\star\ V_{OL} = V_{out} = V_{DSN} = 0$

→ Mid V_M:

Both sat: $I_{DN}(sat) = I_{DP}(sat)$

$\frac{K_n}{2} (V_{GS} - V_{TN})^2 = \frac{K_P}{2} (V_{SG} + V_{TP})^2$

$V_{IN} = V_M$ $\qquad$ $V_{DD} - V_{IN} = V_{DD} - V_M$

Solve for V_M:

$$V_M = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\frac{K_n}{K_P}}}{1 + \sqrt{\frac{K_n}{K_P}}}$$

→ V_{IL} at $\frac{dv_{out}}{dv_{in}} = -1 \Rightarrow$ P_O Lin, N_O sat

$I_{DP}(Lin) = I_{DN}(sat)$

$K_P \left[(V_{SGP} + V_{TP}) V_{SDP} - \frac{V_{SDP}^2}{2} \right] = \frac{K_n}{2} \left[V_{DS} - V_{TN} \right]^2$

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$$K_P\left[(V_{DD}-V_{IN}+V_{TP})(V_{DD}-V_{out})-\frac{(V_{DD}-V_{out})^2}{2}\right]=\frac{K_n}{2}(V_{IN}-V_{TN})^2 \quad \text{---(1)}$$

$$dI_{DP}(V_{IN}, V_{out}) = dI_{DN}(V_{IN})$$

$$\frac{dI_{DP}}{dV_{IN}}dV_{IN}+\frac{dI_{DP}}{dV_{out}}dV_{out}=\frac{dI_{DN}}{dV_{IN}}dV_{IN}$$

$$\frac{dV_{out}}{dV_{in}}=\frac{\frac{dI_{DN}}{dV_{in}}-\frac{dI_{DP}}{dV_{IN}}}{\frac{dI_{DP}}{dV_{out}}}=-1$$

$$\frac{dI_{DN}}{dV_{IN}}-\frac{dI_{DP}}{dV_{IN}}=\frac{-dI_{DP}}{dV_{out}}$$

$$\frac{2K_n}{2}(V_{IN}-V_{TN})-[-K_P(V_{DD}-V_{out}]=-K_P[-(V_{DD}-V_{IN}+V_{T,P})+V_{DD}-V_{out}]$$

rearrange: $$* V_{IL}=\frac{2V_{out}-V_{DD}+V_{TP}+\frac{K_n}{K_P}\cdot V_{TN}}{1+\frac{K_n}{K_P}}$$

$V_{out}(V_{IL})$

→ To find $V_{out}(V_{IL})$ use eq [1]

→ V_{IH} N_o (Lin), P_o (sat)

$$I_{DN}(Lin)=I_{DP}(sat) \quad \text{---(2)}$$

$$K_n\left[(V_{GS}-V_{TN})V_{DS}-\frac{V_{DS}^2}{2}\right]=\frac{K_P}{2}(V_{DD}-V_{IH}+V_{TP})^2$$

V_{IN} V_{out}^2

$$* V_{IH}=\frac{V_{DD}+V_{TP}+\frac{K_n}{K_P}(V_{IN}+2V_{out})}{1+\frac{K_n}{K_P}}$$

→ other I_N / Op relation from eq [2]

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→ For symmetry:

$V_M - V_{IL} = V_{IH} - V_M$

When $K_n = K_p$:- $\mu_n C_{ox} \left(\frac{W}{L}\right)_N = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$

$580 \left(\frac{W}{L}\right)_N = 230 \left(\frac{W}{L}\right)_p$

$* \quad \frac{W_p}{L_p} \cong 2.5 \frac{W_N}{L_N}$

CH23: 23.2 Power Dissipation

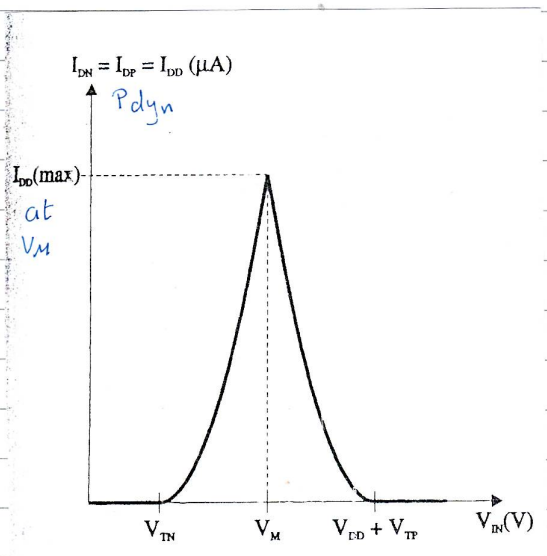
* $P_{stat} = 0$ because $I_{DD(avg)} = 0$

1) input Low → No off → $I_{DD(OH)} = 0$

2) input high → Po off → $I_{DD(OL)} = 0$

* $P_{dyn} = C_L \cdot V \cdot V_{DD}^2$ ⟹ between $V_{TN} < V_{IN} < V_{DD} + V_{TP}$

→ CMOS has smaller power diss. among small Digital logic circuits



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CH23 : 23.9 fan_out

→ Fan_out is determined by Load capacitance, which affects propagation delay.

$$t_{PHL} = C_L \cdot \left[\frac{2V_{TN}}{K_N (V_{DD} - V_{TN})^2} + \frac{1}{K_N (V_{DD} - V_{TN})} \ln \left(\frac{1.5 V_{DD} - 2V_{TN}}{0.5 V_{DD}} \right) \right]$$

dis. o/p → NMOS on (Pull down)

$$t_{PLH} = C_L \cdot \left[\frac{-2V_{TP}}{K_P (V_{DD} + V_{TP})^2} + \frac{1}{K_P (V_{DD} + V_{TP})} \ln \left(\frac{1.5 V_{DD} + 2V_{TP}}{0.5 V_{DD}} \right) \right]$$

charging o/p → PMOS on (Pull up)

→ t_{PHL} : Propagation delay when o/p switches from H to L (I/p L → H)

More exact: Time difference between when input rises from min to 50% of max and when o/p drops from max to 50%

→ t_{PLH} : Time difference between when input drops to 50% of max and o/p rises to 50% of max.

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t_{pHL} :

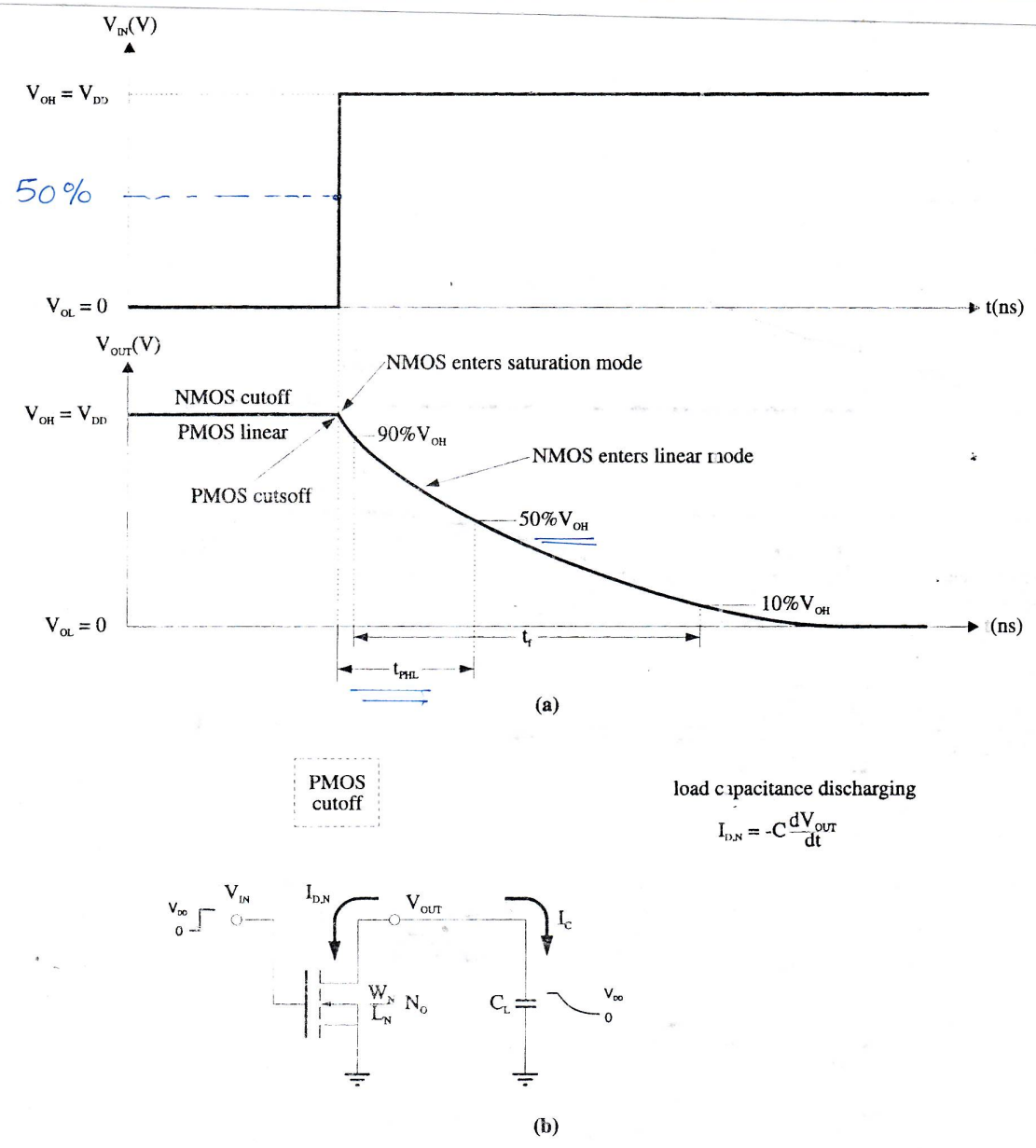

FIGURE 23.10 CMOS Inverter Output High-to-low Transition: (a) Step-up input and output response curves, (b) Load capacitance discharges through active NMOS transistor

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t_{PLH}:

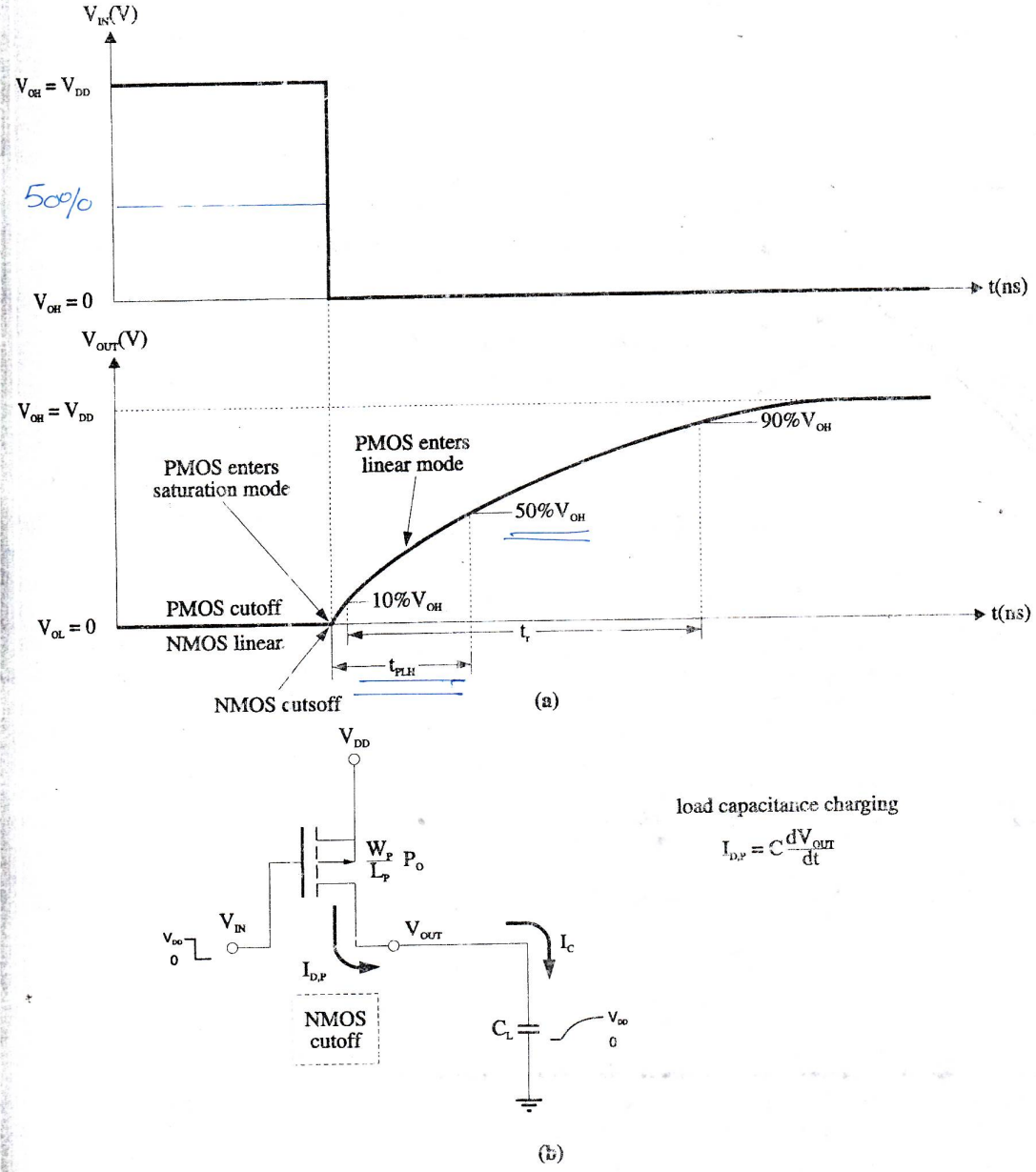

FIGURE 23.11 CMOS Inverter Output Low-to-high Transition: (a) Step-down input and output response curves, (b) Load capacitance charges through PMOS transistor

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* For a certain propagation delay, find C_L from both equations and choose the smaller one.

→ Fan-out for symmetry :-

Assume for symplicity: 1) $L_P = L_N$
2) Load and driver are identical

for a single gate:

$$C_{IN}' = (W_N' L_N' + W_P' L_P') C_{ox}'$$

for symmetry : $\frac{W_P}{L_P} = \frac{2.5 W_N}{L_N}$

$$C_{IN} = (W_N L_N + 2.5 W_N L_N) C_{ox}'$$

$$C_{IN} = 3.5 W_N L_N C_{ox}' \quad \ldots (1)$$

$$K_N = \mu_N C_{ox} \frac{W_N}{L_N} \quad \ldots (2)$$

$$C_L = F C_{IN} \quad \ldots (3)$$

$$\frac{(3)}{(2)} = \frac{C_L}{K_N} = \frac{F C_{IN}}{\mu_n C_{ox} \frac{W_N}{L_N}} = \frac{F (3.5 W_N L_N)(C_{ox})}{\mu_n C_{ox} \frac{W_N}{L_N}}$$

* $$F = \frac{\mu_N}{3.5 L_N^2} \cdot \frac{C_L}{K_N}$$

* $$F = \frac{\mu_N \cdot t_p}{3.5 L_N^2 \left[\frac{2 V_{TN}}{(V_{DD} - V_{TN})^2} + \frac{1}{(V_{DD} - V_{TN})} \ln \left(\frac{1.5 V_{DD} - 2 V_{TN}}{0.5 V_{DD}} \right) \right]}$$

* $$F = \frac{C_L}{C_{IN}}$$

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→ Read Example 23.10

Example 23.3: Design for symmetry and check;

$V_{DD} = 5V$, $k_n' = 40\ \mu\frac{A}{V^2}$, $k_p' = 16\ \mu\frac{A}{V^2}$

$W_N = 4\mu m$, $L_N = L_p = 2\mu m$

Solution: $\frac{W_p}{k_p} = \frac{W_N}{k_N}(2.5) \Rightarrow W_p = 4 \times 2.5 = 10\ \mu m$

1)

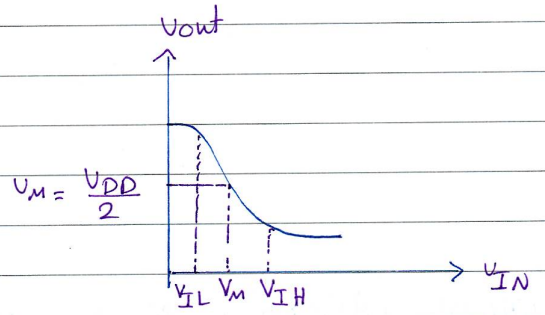
$K_N = 40\mu\left(\frac{4}{2}\right) = 80\ \mu A/V^2$

$k_p = 16\mu\left(\frac{10}{2}\right) = 80\ \mu A/V^2$

$\Rightarrow k_N = k_p$ ∟

2)

$V_M - V_{IL} = V_{IH} - V_M$



$V_M = \frac{5 + (-1) + 1\sqrt{\frac{80}{80}}}{1 + \sqrt{\frac{80}{80}}} = 2.5\ V$, or $V_M = \frac{V_{DD}}{2} = 2.5\ V$

$V_{IL} = \frac{2\,V_{out}(V_{IL}) - 5 + (-1) + \frac{80}{80}(1)}{1 + \frac{80}{80}} \Rightarrow V_{out}(V_{IL}) = V_{IL} + 2.5$ ... ①

(P_o(Lin)) (N_o(sat))

$I_{DP}(Lin) = I_{DN}(sat)$

$\frac{80\mu}{2}[V_{IL} - 1]^2 = 80\mu\left[(5 - V_{IL} - 1)(5 - (V_{IL} + 2.5)) - \frac{(5 - (V_{IL} + 2.5))^2}{2}\right]$ ... ②

Solve ① and ②: $V_{IL} = 2.125$

$V_{IH} = \frac{5 - 1 + \frac{80}{80}[1 + 2\,V_{out}(V_{IH})]}{1 + \frac{80}{80}} \longrightarrow V_{out}(V_{IH}) = V_{IH} - 2.5$

Also $I_{DN}(Lin) = I_{DP}(sat)$

$80\mu\left[(V_{IH} - 1)(V_{IH} - 2.5) - \frac{(V_{IH} - 2.5)^2}{2}\right] = \frac{80\mu}{2}[5 - V_{IH} - 1]^2$

$V_{IH} = 2.875\ V \Longrightarrow V_M = 2.5 - 2.125 = 0.375\ V$ ∴ Symmetry ∟

$V_M = 2.875 - 2.5 = 0.375\ V$

CHAPTER 24 CMOS logic gates

4-12-2016 Sunday

24. (2+3+4) NAND, AND, OR and NOR

1) NAND Gate

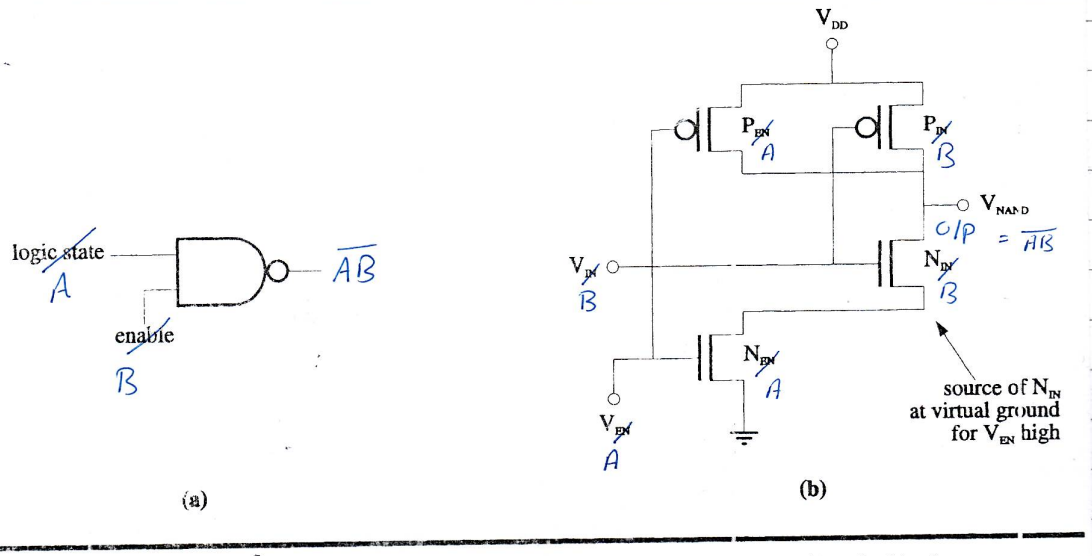


FIGURE 24.7 NAND Gate Used as an Enabling Inverter; Output is held high regardless of V_{IN} for V_{EN} low

A	B	out
L	L	H
L	H	H
H	L	H
H	H	L

NAND

* For NANDing / ANDing → Nmos in series
  → Pmos in parallel

* For NORing / ORing → Nmos in parallel
  → Pmos in series

→ Output high state :-

1) All input, (or any) low.

N_A and N_B are off $I_{DN} = 0$

P_A and P_B are Linear, $I_{DP(Lin)} = 0$
→ $V_{DS} = 0$

$V_{out} = V_{DD} - 0 = V_{DD}$

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2) V_{INA} Low, V_{INB} high.

$N_A \rightarrow$ off , N_B has no path to the ground

P_B is off , P_A is Lin

$I_{DPB} = I_{DNB} = 0 \rightarrow V_{out} = V_{OH} = V_{DD} - 0 = V_{DD}$.

3) V_{INA} high, V_{INB} Low.

N_A (Lin) $\rightarrow V_{DSA} = 0 \rightarrow N_B$ is off.

P_B is (Lin) and P_A is off $\rightarrow V_{SDB} = 0 \Rightarrow V_{OH} = V_{DD}$.

4) All A,B high.

P_A, P_B off $\rightarrow I_{DP} = 0$

N_A, N_B Lin $\rightarrow V_{DSN} = 0$ ← why?

$I_{DN} = 0 \rightarrow V_{DSN} = 0$

$V_{out} = V_{OL} = 0$

* AND Gate:-

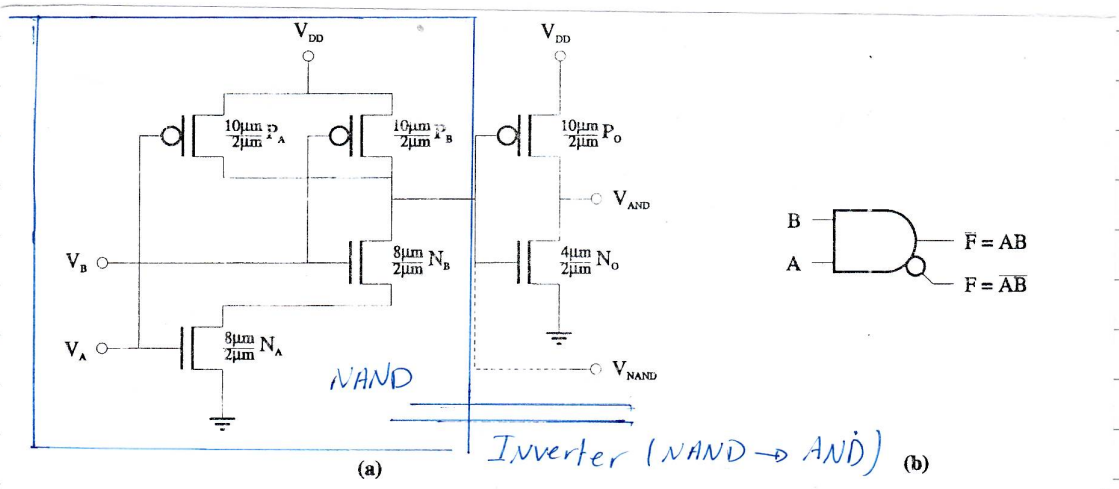

FIGURE 24.13 CMOS AND/NAND Gate: **(a)** NAND fed inverter, **(b)** Circuit symbol indicating both AND and NAND functions are available

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* For symmetry:

for a symmetric VTC → $\frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

for a 2-input NAND Gate → $\frac{2W_P}{L_P} = \frac{2.5 W_N}{L_N}$

for an i-input NAND Gate → $\frac{i W_P}{L_P} = \frac{2.5 W_N}{L_N}$

* CMOS NOR Gate.

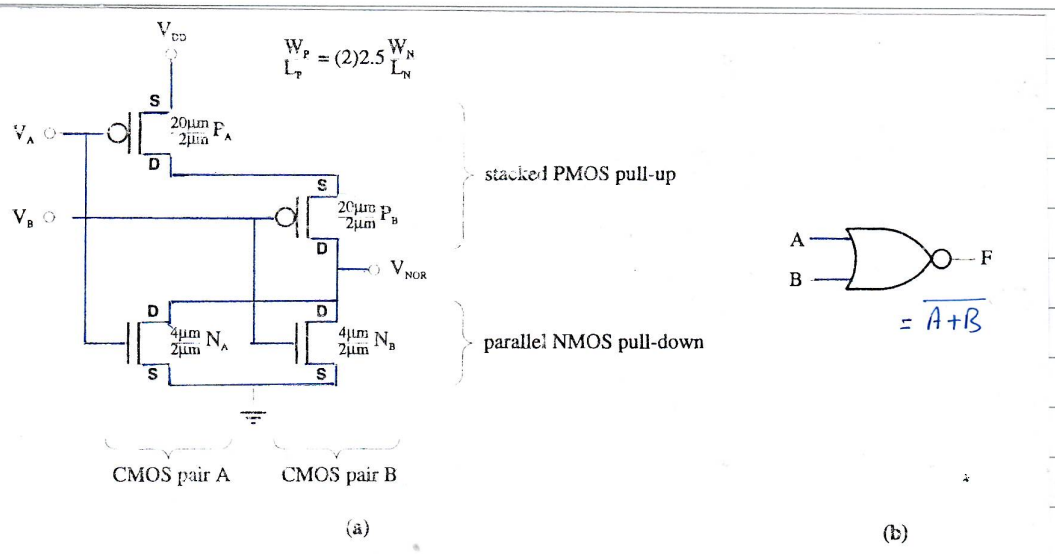

FIGURE 24.9 Two-input CMOS NOR Gate with W/L Ratios in Microns (μm): **(a)** Circuit schematic, **(b)** Circuit symbol

→ V_{OL}: All or any input high.

N_A, N_B Lin → $V_{DS}=0$

$V_{out} = V_{OL} = 0$

→ Any input high (i.e. V_A high, V_B low)

The corresponding N is Linear → $V_{DS}=0$

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The corresponding p is off

$V_{out} = V_{OH} = V_{DD}$

→ Both inputs low:

N_A, N_B are off ; P_A, P_B are linear

$V_{SD} = 0 \rightarrow V_{out} = V_{OH} = V_{DD}$

* CMOS OR Gate

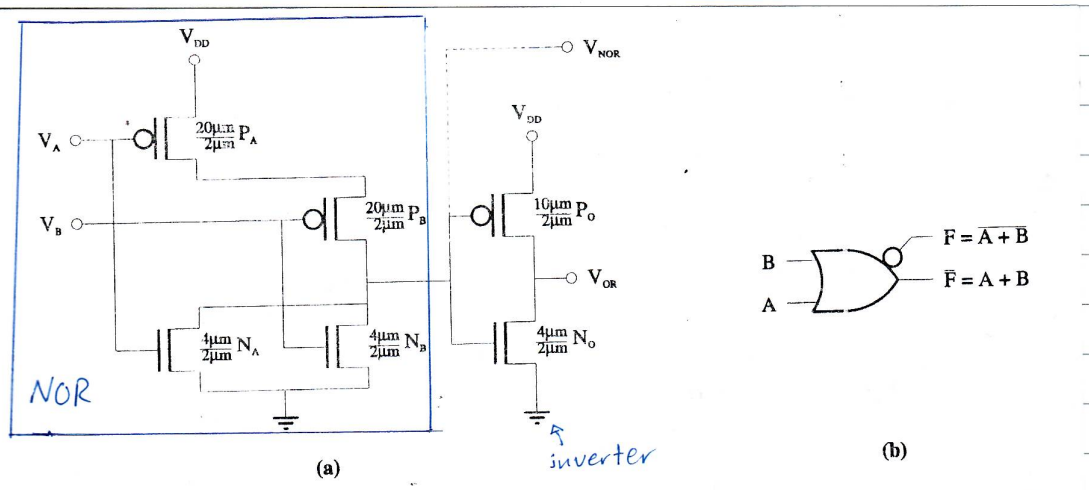


FIGURE 24.14 CMOS OR/NOR Gate: (a) NOR fed inverter, (b) Circuit symbol indicating both OR and NOR functions are available

* for symmetry:

→ 2 inputs OR Gate: $\frac{W_P}{L_P} = 5\frac{W_N}{L_N}$

→ i inputs OR Gate: $\frac{W_P}{L_P} = 2.5i\frac{W_N}{L_N}$

6-12-2016
Tuesday

CH24: 24.4 „AND_OR_Inverter Logic function (AOI)„

AOI

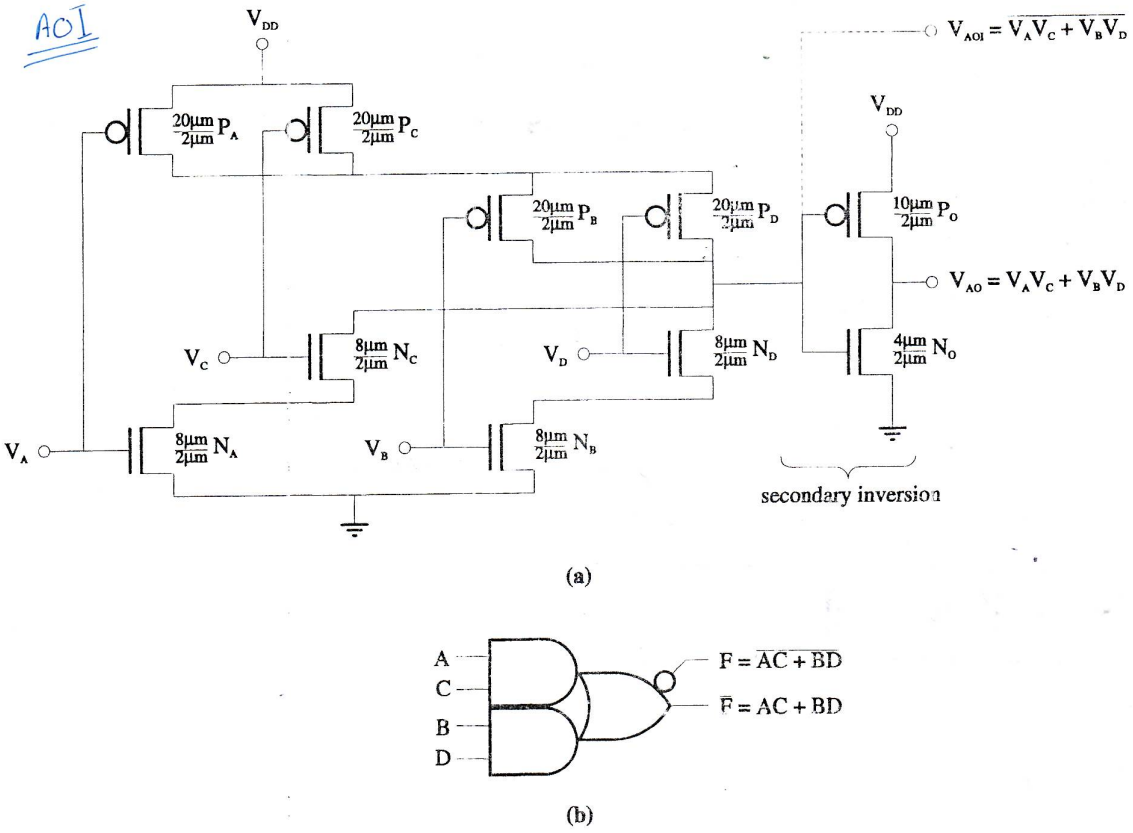


FIGURE 24.18 Four-input CMOS AND-OR gate: **(a)** Circuit with cascaded inverter, **(b)** Logic schematic

Example: Draw the CMOS Logic cct:

1) $y = \overline{(A+B+C)(DE+F)}$

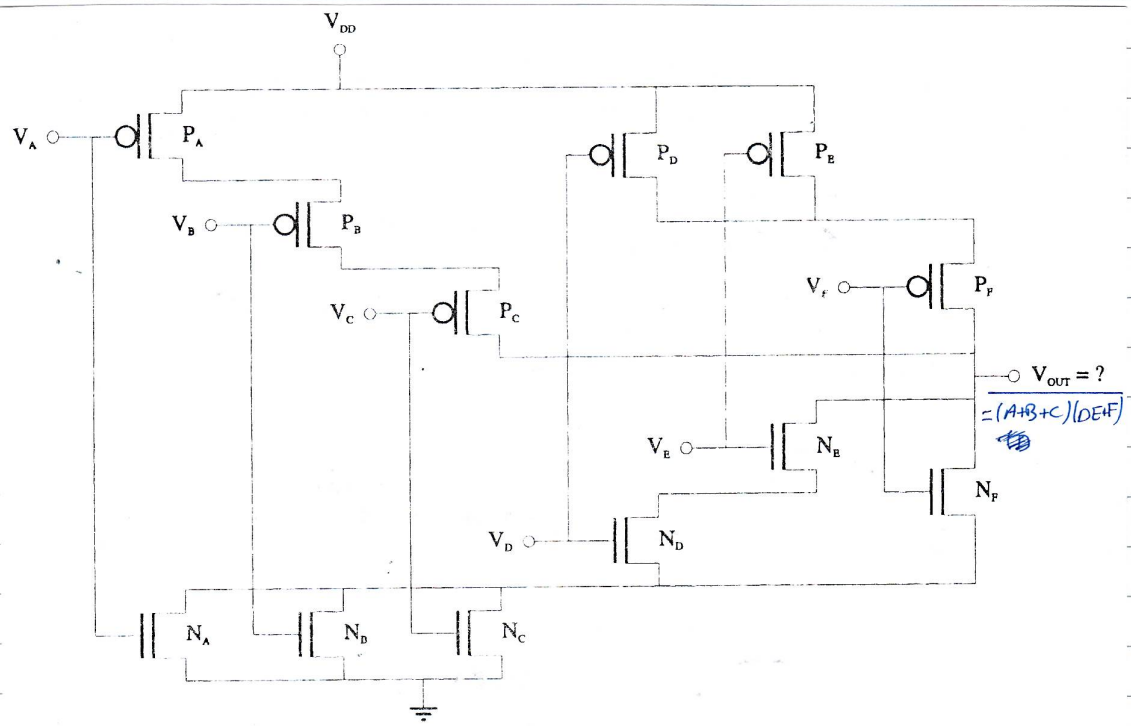
2) $y = (AB+C)D + (E+F)(G+H)$

1 → on the next page.

2 → Home work.

6-12-2016
Tuesday

1) $y = \overline{(A+B+C)(DE+F)}$



6-12-2016
Tuesday

CHAPTER 32 ROM: Read only memory

32.1+32.2 → Diode Rom, BJT ROM (The same)

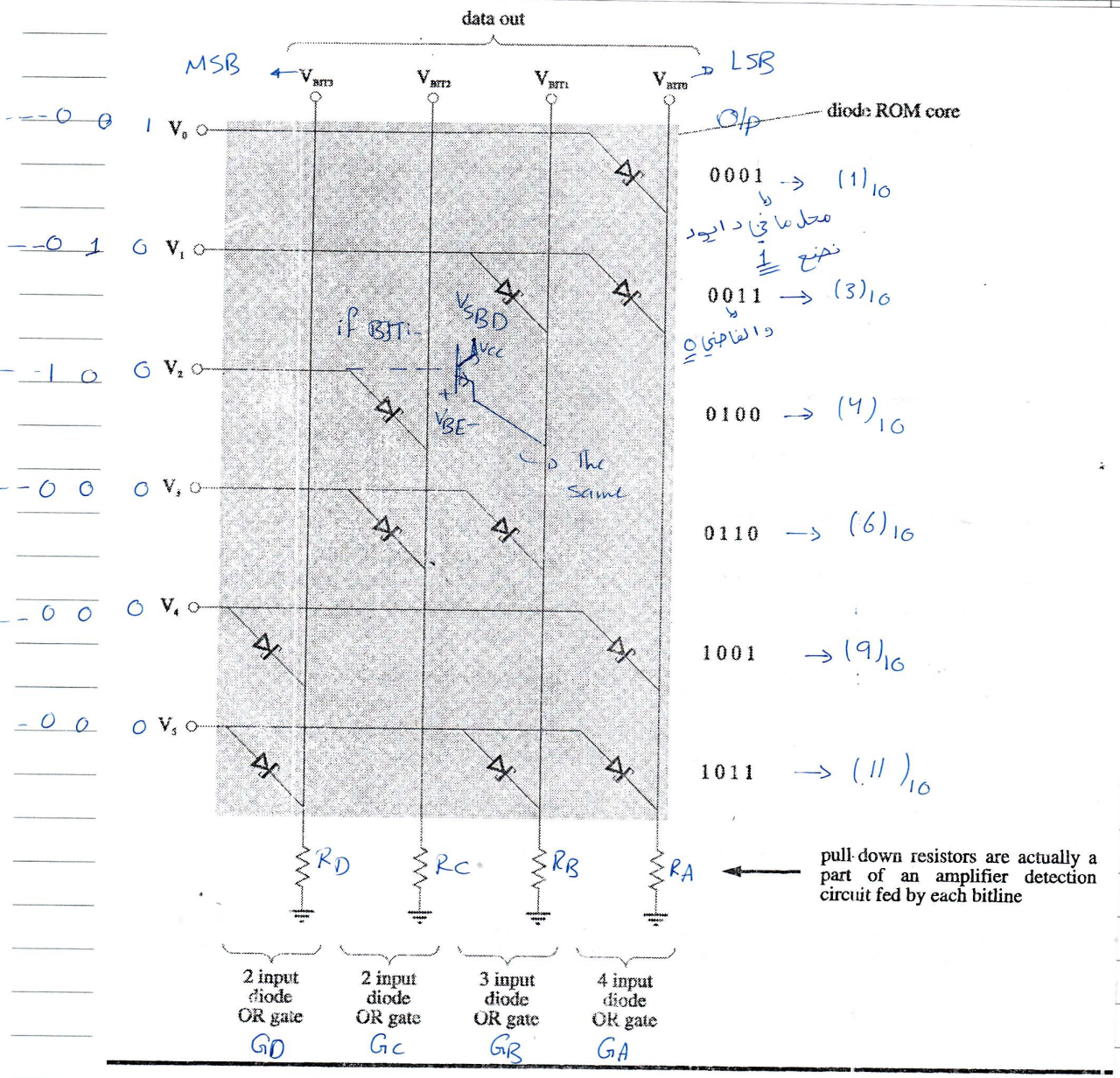


FIGURE 32.2 Diode ROM Cell

G_A, G_B, G_C, G_D are Diode_Resistor OR gates.

function: Single input is high at a time and the rest is Low.

i.e. when $V_0 = 1$

$V_{Bit\,0} = V_0 + V_1 + V_4 + V_5 = 1 + 0 + 0 + 0 = 1$

$V_{Bit\,1} = V_1 + V_3 + V_5 = 0 + 0 + 0 = 0$

8-12-2016
Thursday

	V_{Bit3}	V_{Bit2}	V_{Bit1}	V_{Bit0}
output 1:	0	0	0	1
output 2:	0	0	1	1
output 3:	0	1	0	0
output 4:	0	1	1	0
output 5:	1	0	0	1
output 6:	1	0	1	1

L
L→R →

see V_{Bit0} down ↓

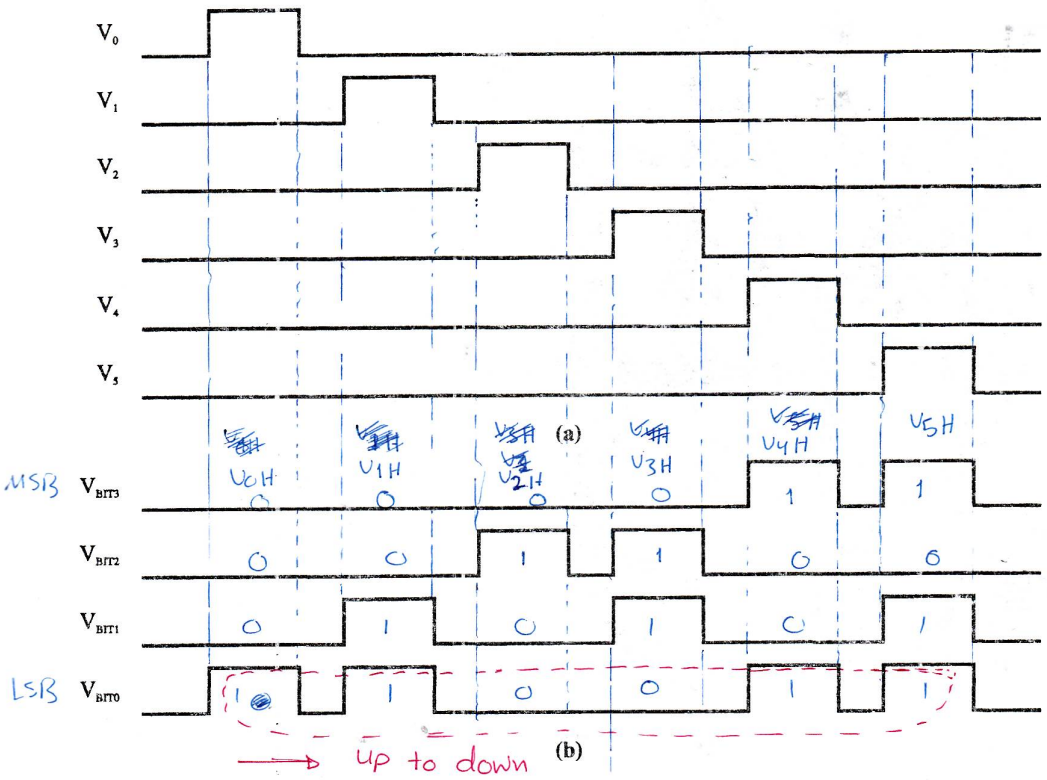


FIGURE 32.3 Addressing Each Row of Figure 32.2 Diode ROM Cell: **(a)** Input stimulus: each input brought high one at a time, **(b)** Resulting outputs

8-12-2016
Thursday

32.7 CMOS Read-only memories:-

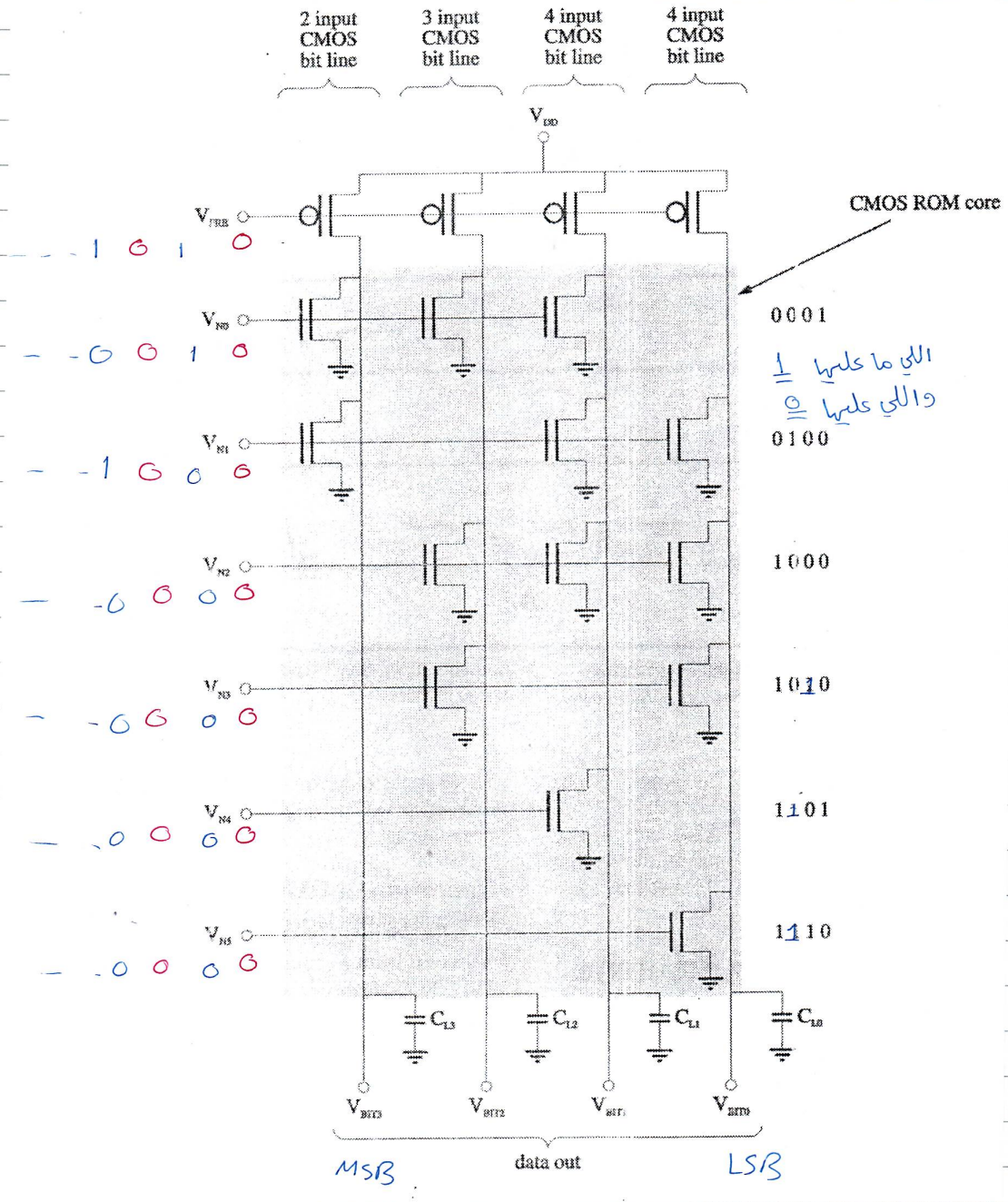


FIGURE 32.26 CMOS Four-bit, Six-input ROM Cell with Capacitive Loading

→ Initially V_{PRE} is set at Low and all inputs V_N are Logic Zero too.

8-12-2016
Thursday

⟹ Capacitors will charge to V_{DD} since PMOS's are Linear and $V_{SD}=0$, and NMOS's are off ⟹ pull up to V_{DD}.

→ Next, V_{WO} is set to Logic 1 and rest all 0; V_{PRE} is set to Logic 1.

⟹ NMOS with Logic 1 will be Linear and the rest are off, Also PMOS's are off too.

→ Any gate with a Lin. NMOS will have a path to ground ($V_{DS}=0$), and cap will discharge → o/p will be Logic 0

→ Any gate with all NMOS off → Cap. Can't discharge and $V_C = V_{out} = V_{DD}$ (Logic 1)

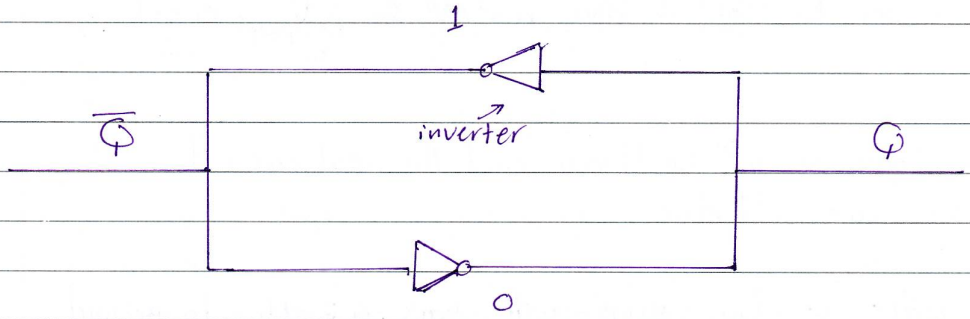
→ Next before setting V_{WL} to Logic 1 all input including V_{PRE} are set to Logic 0 to recharge capacitors

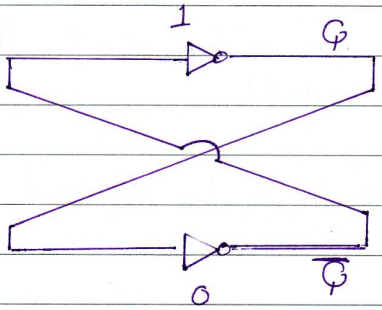
CHAPTER 33: Semi-Conductor static Random access memories (RAM)

8-12-2016
Thursday

33.1 SRAM with transmission gates

33.2 static MOSFET SRAM cell. ← Cross Coupled Inverter Latch.





→ RAM: Data can be read in a sequence independent of the order it was originally written.

→ SRAM: maintain storage of data as long as power is applied to the Semi-Conductor.

11-12-2016
Sunday

CHAPTER 33

* Basic static RAM Cell

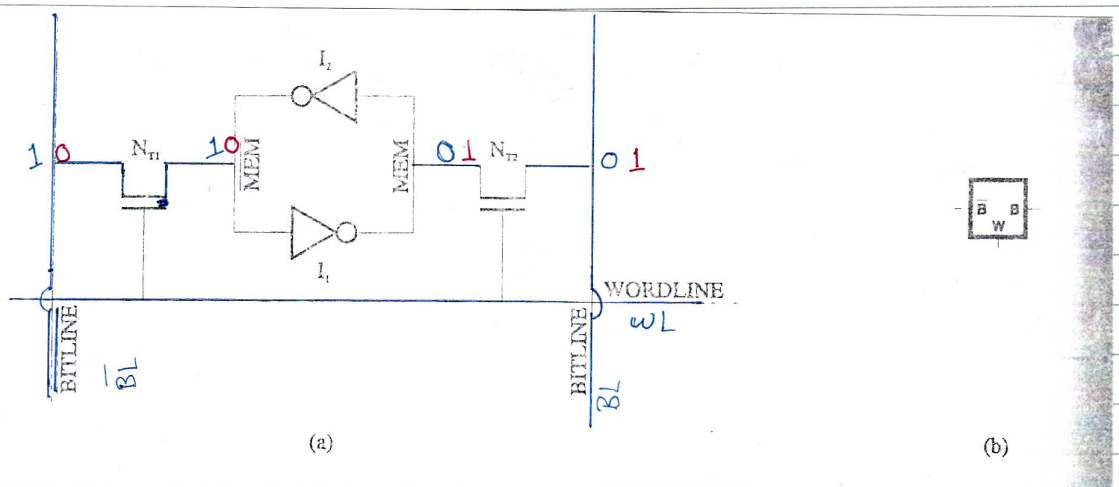
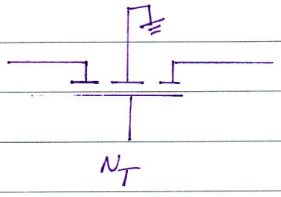


FIGURE 33.1 Basic Static RAM Cell with Transmission Gates: (a) Cross coupled inverter latch with complementary NMOS transmission gates, (b) Circuit symbol used in multi-bit static RAM cell

NT_2 and NT_1 are transmission gates



* when input high at N_T, N_T conduct and data is transmitted to or from cell.

* when input at N_T is low → N_T is off and there is no data transmission.

* Storage of a single bit data:

For storge → $W_L = 0$
N_{T_1} and N_{T_2} are off → no data transmission.

if MEM = 1 → $\overline{MEM} = 0$ → MEM = 1

if MEM = 0 → $\overline{MEM} = 1$ → MEM = 0

11-12-2016
Sunday

* Writing a single bit to cell:

To write to cell, $WL = 1 \Rightarrow N_{T_1}$ and N_{T_2} are both on and transmit data from BL to MEM and $\overline{BL}$ to $\overline{MEM}$

if $BL = 1 \Rightarrow MEM = 1$
$\overline{BL} = 0 \Rightarrow \overline{MEM} = 0$

if $BL = 0 \Rightarrow MEM = 0$
$\overline{BL} = 1 \Rightarrow \overline{MEM} = 1$

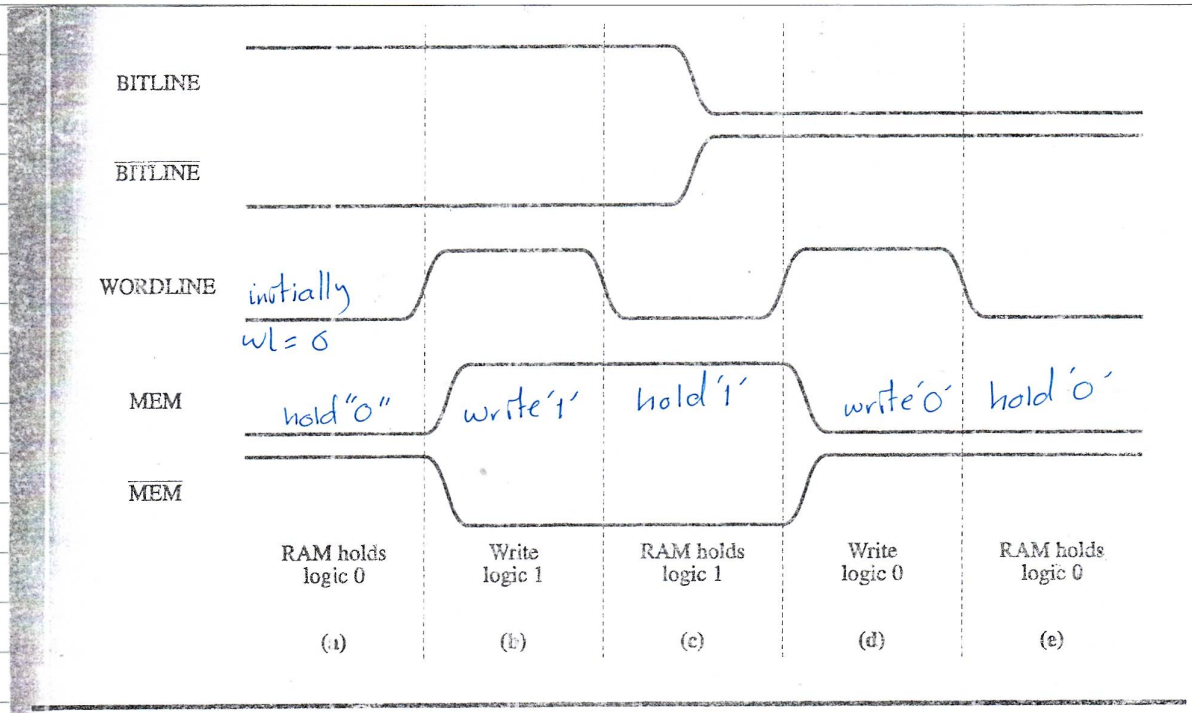


FIGURE 33.4 WRITE Into RAM Bit Cell: (a) RAM initially holds a zero, (b) WORDLINE brought active with BITLINE driven high—WRITEs logic 1 into RAM bit, (c) RAM holds logic 1 after WORDLINE brought inactive, (d) WORDLINE brought high and BITLINE driven low—WRITEs logic 0 into RAM bit, (e) RAM holds logic 0 after WORDLINE brought low

11-12-2016
Sunday

* Reading from a Single bit:

WL=1, N_{T1} and N_{T2} are on

BL and $\overline{BL}$ are allowed to read data from MEM and $\overline{MEM}$

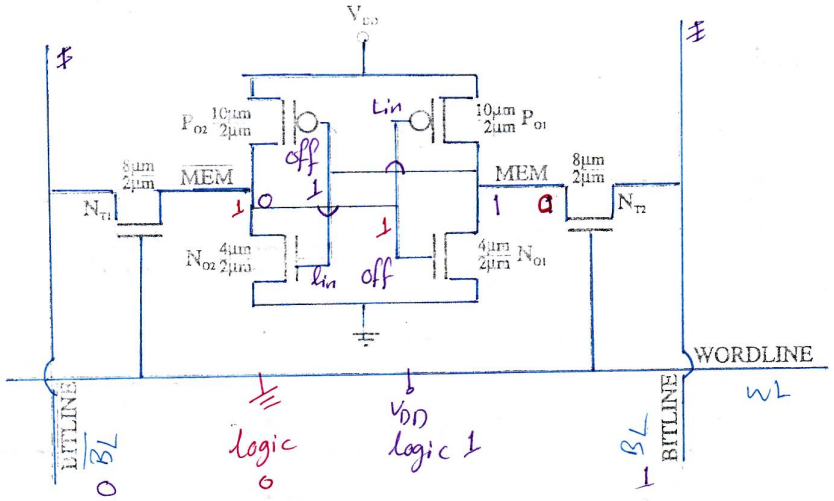


FIGURE 33.6 CMOS Static RAM Cell

Multivibrators

11-12-2016
Sunday

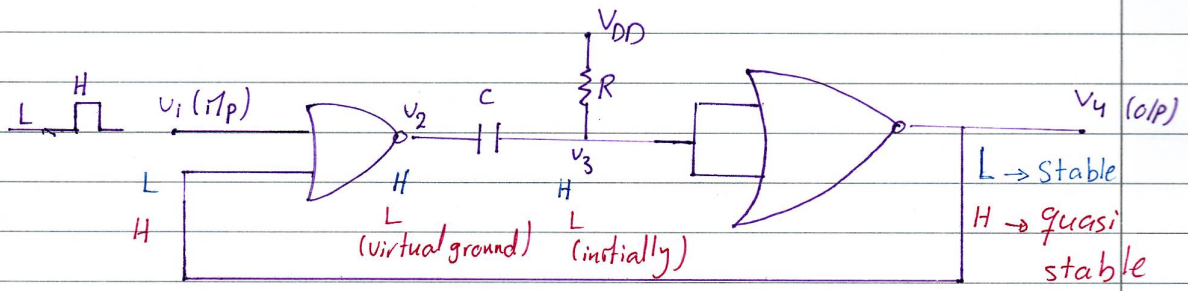
* Multivibrators.

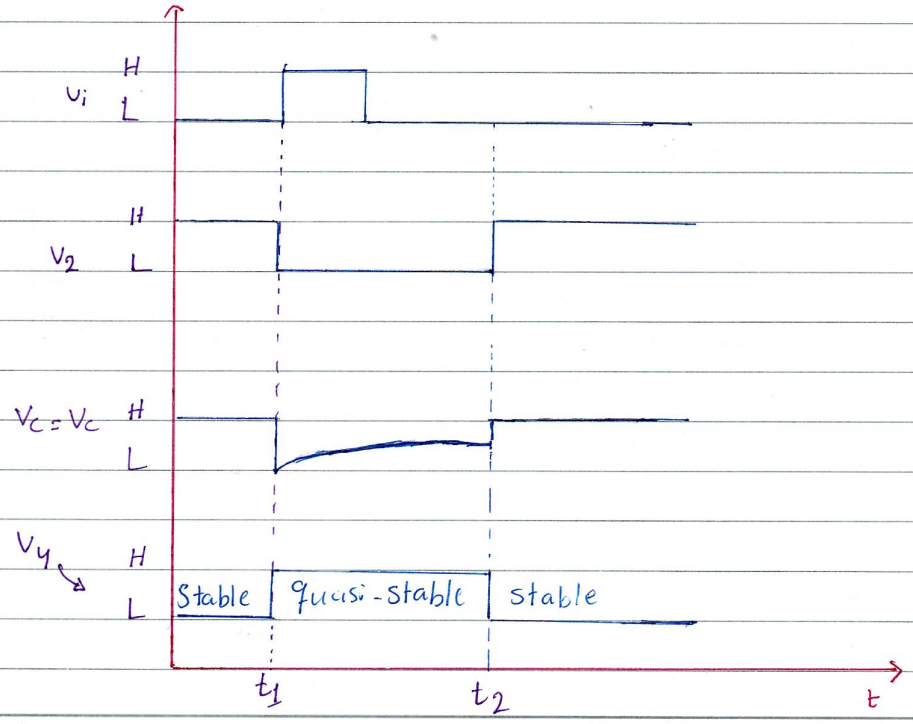
1) Monostable → stable
   → quasi-stable (needs a trigger).

2) Astable (no stable state): both states do need a trigger

3) Bistable state (flip-flop)

* CMOS monostable Circuit.





11-12-2016 Sunday → Tuesday

Multivibrators

$$V_{th} = V_C = V_i + (V_t - V_i)(1 - e^{-t/RC})$$

V_i → 0V initially; V_t → target V_{DD}; V_i → 0V; t → $T = t_2 - t_1$.

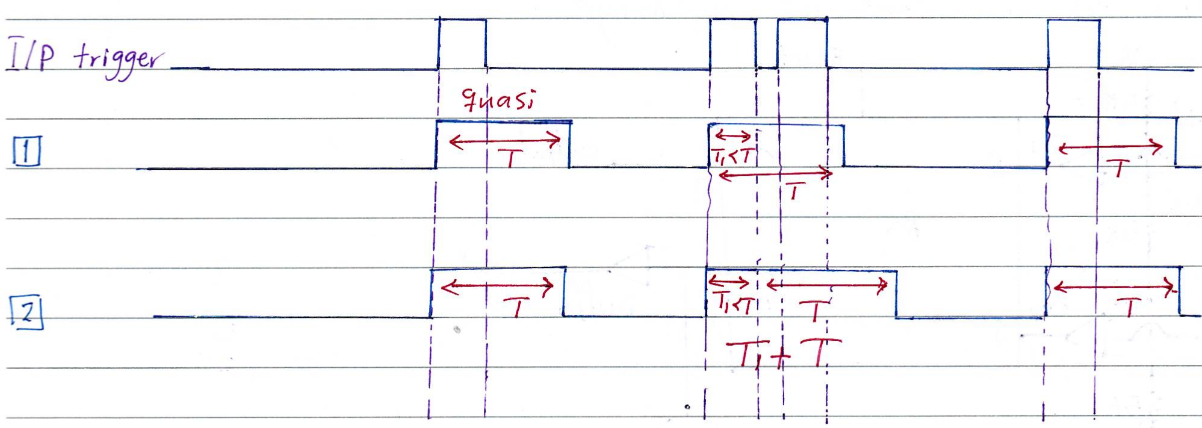
$$T \Rightarrow \quad t_2 - t_1 = ((R + R_{on}) \ln \left(\frac{R}{R + R_{on}} \cdot \frac{V_{DD}}{V_{DD} - V_{Th}} \right)$$

(R_{on}: Cmos ten ohms)

→ if $R \gg R_{on}$, $V_{Th} = \frac{V_{DD}}{2}$:-

$$* \; T = RC \ln 2 = 0.7 RC$$

* Two types of o/p: ⇒ 1) Non Retriggable
⇒ 2) Retriggable.



* The 555 IC timer: 555 timer as a Monostable multivibrator:

1) $t < t_0$, at $V_0 = 0$ ⇒ $Q = 0$, $\bar{Q} = 1$

T_1 is on and discharges ⇒ $V_{TH} = 0$

C_1 output low (no change).

The 555 circuit

13 ← 11-12-2016 Sunday → Tuesday

* at $t = t_0$ ⇒ trigger is applied

$$V_{trig} < \frac{1}{3} V_{cc}$$

⇒ CO_2 o/p is high ⇒ flip-flops is high. $Q = 1$

T_1 is off $\bar{Q} = 0$

* Capacitance will charge through R_T until

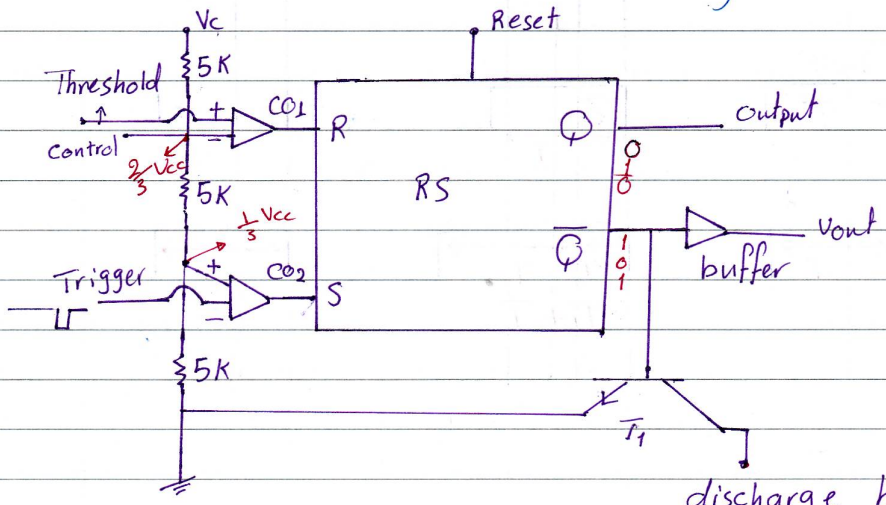
$$V_c = V_{th} = \frac{2}{3} V_{cc}$$

⇒ CO_1 output will be high

$R = 1 \Rightarrow \bar{Q} = 1$

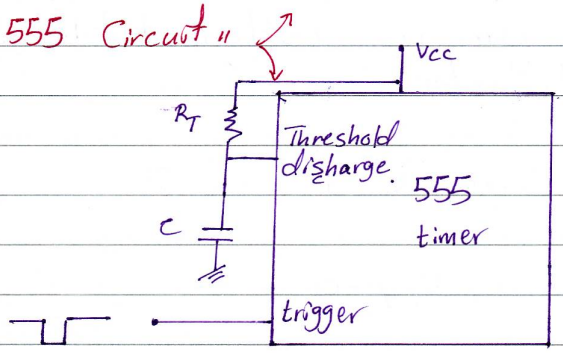
$Q = 0$

T_1 is on and will discharge.



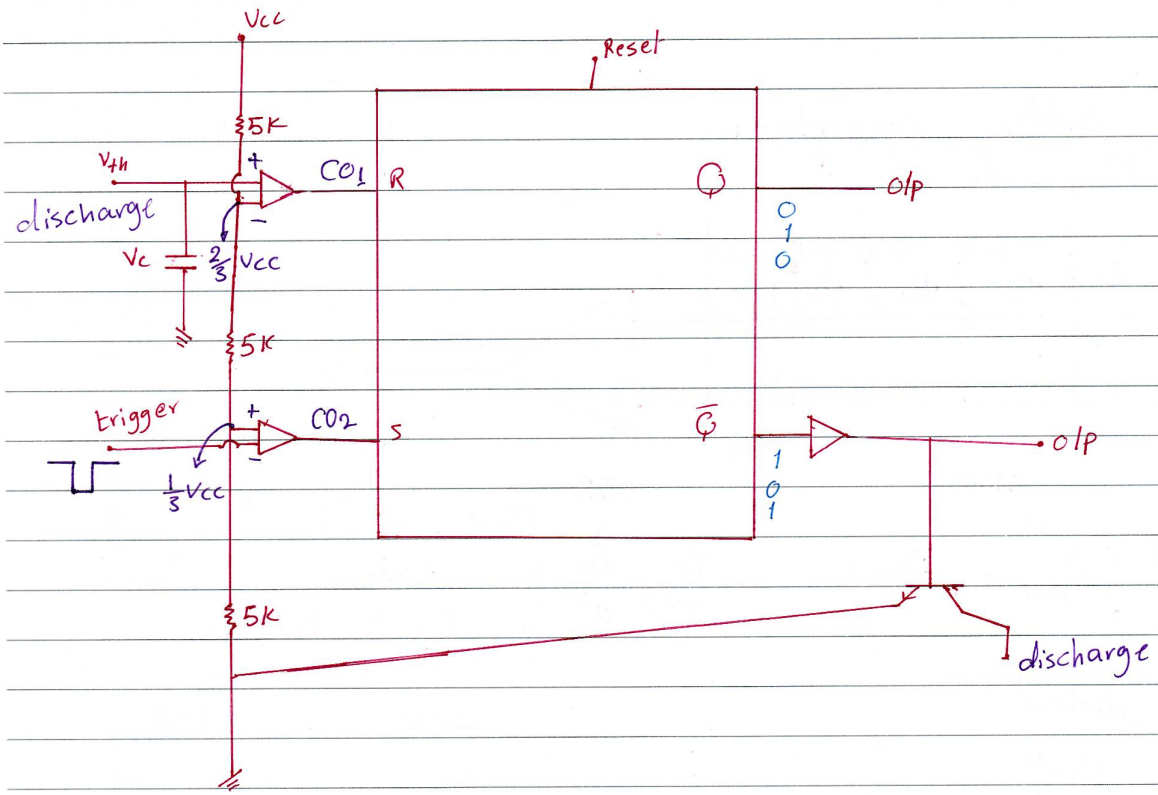
discharge bath (connected to threshold)

"The 555 Circuit"

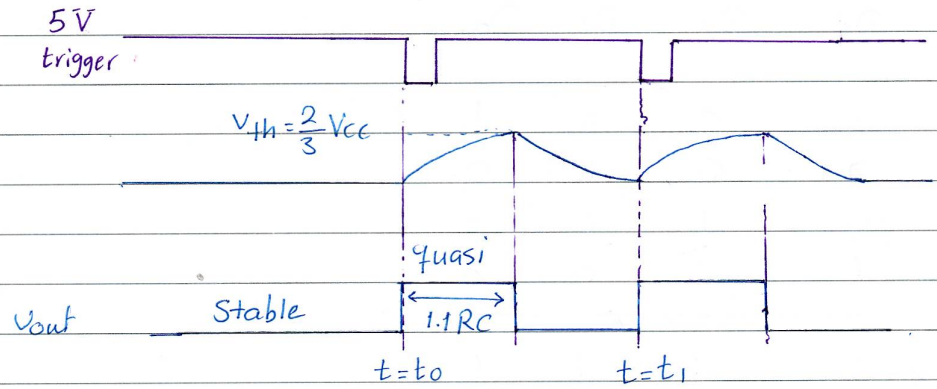


The 555 Circuit

13 ← 11-12-2016 Sunday
Tuesday



Ex:-



Ex: $V_{cc} = 5\,V \rightarrow V_{th} = \frac{2}{3}V_{cc} = \frac{2}{3} \times 5 = 3.3\,V$

$$V_c = V_f + (V_i - V_f)\, e^{-t_p/RC}$$

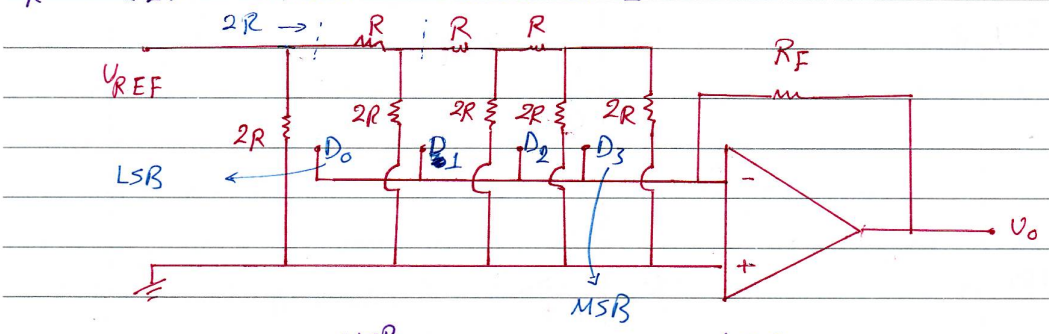
$$3.3 = 5 + (0-5)\, e^{-t_p/RC}$$

$$\rightarrow t_p = 1.08\,RC \approx 1.1\,RC$$

15-12-2016
Thursday

Digital to Analog Converters (DAC)

* R-2R ladder converter:



$$V_{out} = \frac{-V_{ref}}{2}\left(D_{N-1} + \frac{D_{N-2}}{2} + \cdots + \frac{D_1}{2^{N-2}} + \frac{D_0}{2^{N-1}}\right)$$

MSB ↙ LSB ↘

$N = 4 \rightarrow$ # of bits

e.g. $D_3\ D_2\ D_1\ D_0$

1 1 0 0

MSB LSB

$$V_{out} = \frac{-n}{2^{N-1}} V_{ref}$$

n ← decimal

if

D_3	D_2	D_1	D_0	
0	0	0	1	
0	0	1	0	
0	1	0	0	
1	0	0	0	
1	1	1	1	← 15

5V

$V_{out}\ (D_0 = 1) = \frac{-5}{2}\left(\frac{1}{8}\right) = -0.312\ V$

$V_{out}\ (D_1 = 1) = \frac{-5}{2}\left(\frac{1}{4}\right) = -0.625\ V$

$V_{out}\ (D_2 = 1) = \frac{-5}{2}\left(\frac{1}{2}\right) = -1.25\ V$

$V_{out}\ (D_3 = 1) = \frac{-5}{2}(1) = -2.5\ V$

$V_{out\ total} = -(0.312 + 0.625 + 1.25 + 2.5) = -4.687$

15.12.2016 Thursday

DAC

$\frac{5}{16} = 0.315$ ← Vref

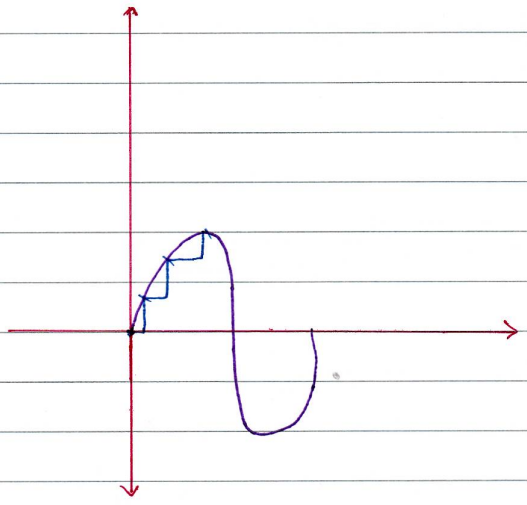
↳ actual # of levels (including 0000)

$\frac{5}{16} \times 15 = 4.68\ V$ ← # of counts; 16 ← # of levels

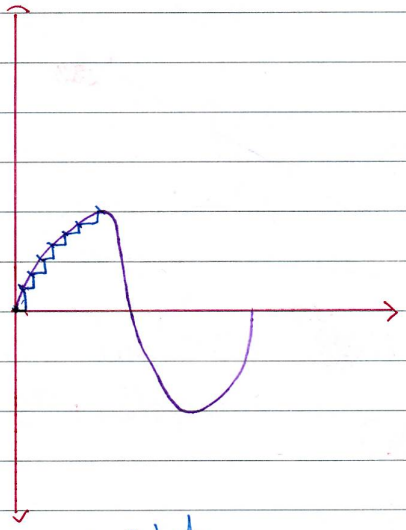
$$V_{ref} = \frac{\#\text{ of levels}}{\#\text{ of counts}} \times V_{out}$$ (# of levels = 2^n)

$$V_{ref} = \frac{16}{15} \times 4.68$$

Resolution ≡ $Res = \frac{V_{ref}}{2^N - 1}$



N = 2 bits



N = 3 bits

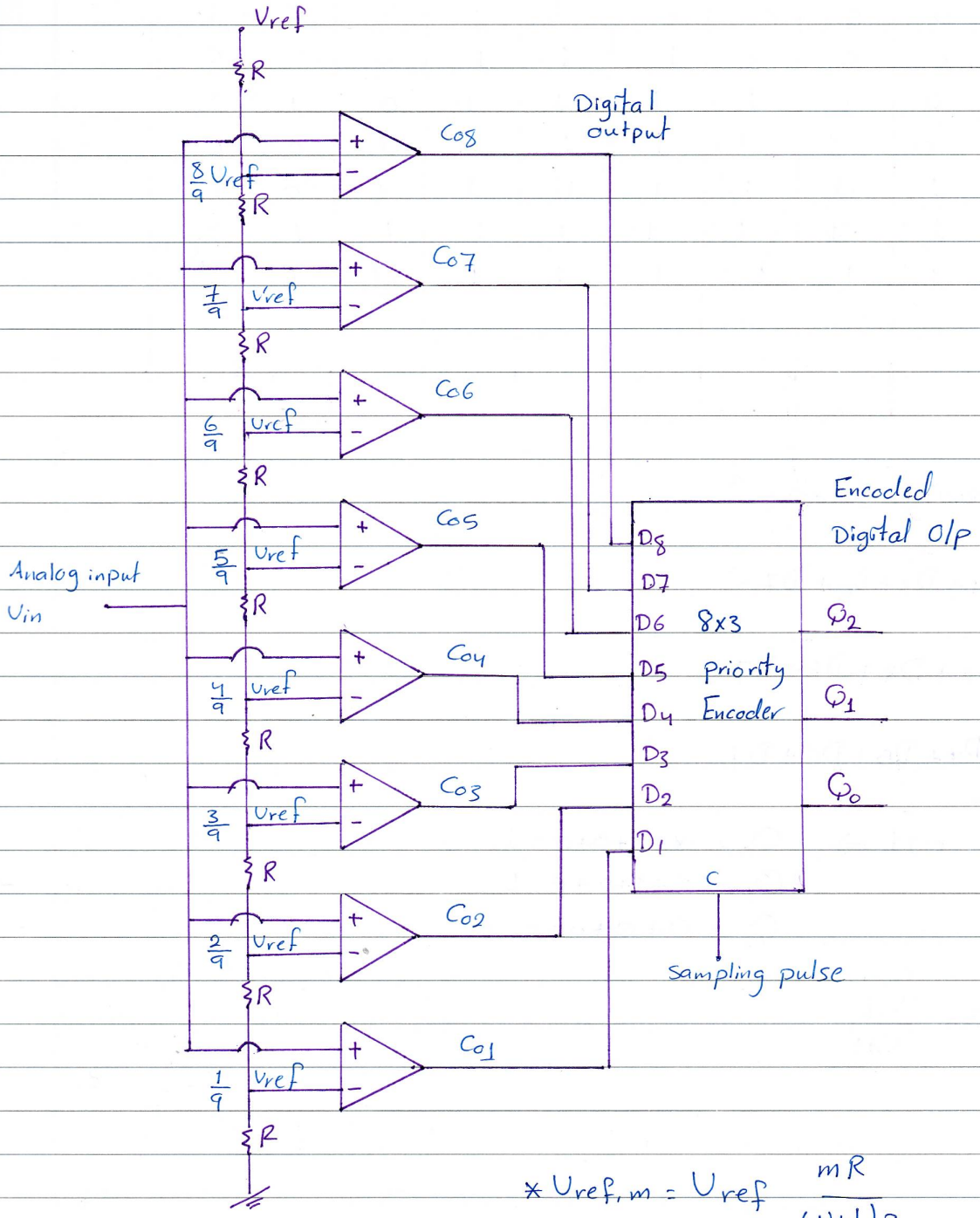
$Res = \frac{V_{ref}}{2^N - 1} = \frac{5}{4-1} = \frac{5}{3}$

$Res = \frac{5}{8-1} = \frac{5}{7}$

$$Accuracy = \frac{Res}{V_{ref}}$$

18-12-2016
Sunday

Analog to Digital Converter
(Binary Encoded A/D Converter)



$$* V_{ref,m} = V_{ref} \frac{mR}{(N+1)R}$$

N: number of O/p bits.

i.g. $V_{ref,2} = V_{ref} \frac{2R}{(8+1)R} = \frac{2}{9} V_{ref}$

18-12-2016
Sunday

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	1	1	0	1	0
0	0	0	0	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

8x3 priority Encoder ↑

$Q_0 = D_1 + D_3 + D_5 + D_7$

$Q_1 = D_2 + D_3 + D_6 + D_7$

$Q_2 = D_4 + D_5 + D_6 + D_7$

i.g. $011 \Rightarrow$ $Q_0 = x + 1 + 0 + 0 = 1$

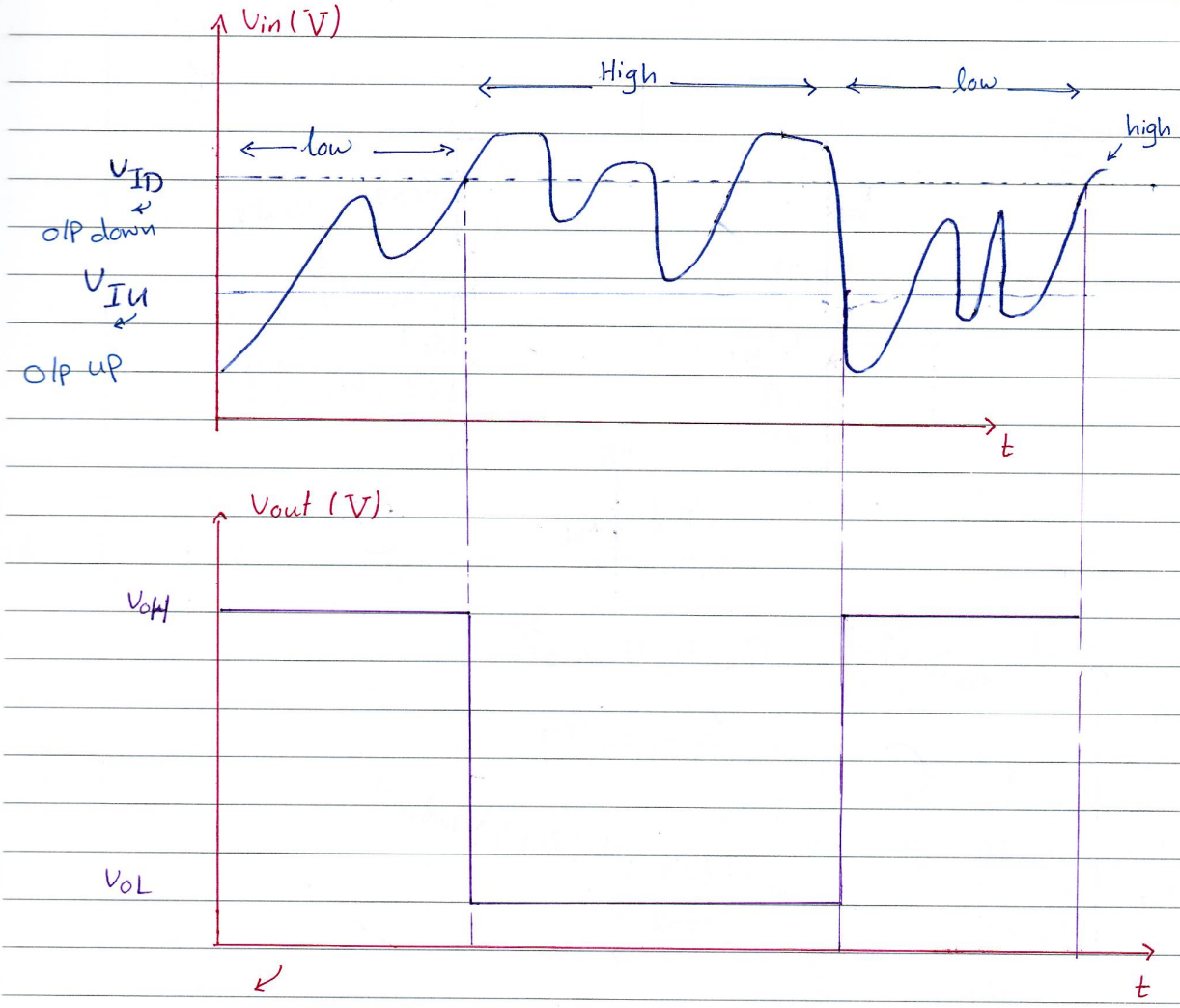
$Q_1 = x + 1 + 0 + 0 = 1$

$Q_2 = 0 + 0 + 0 + 0 = 0$

$Res = \frac{V_{ref}}{N+1}$

18-12-2016
Sunday

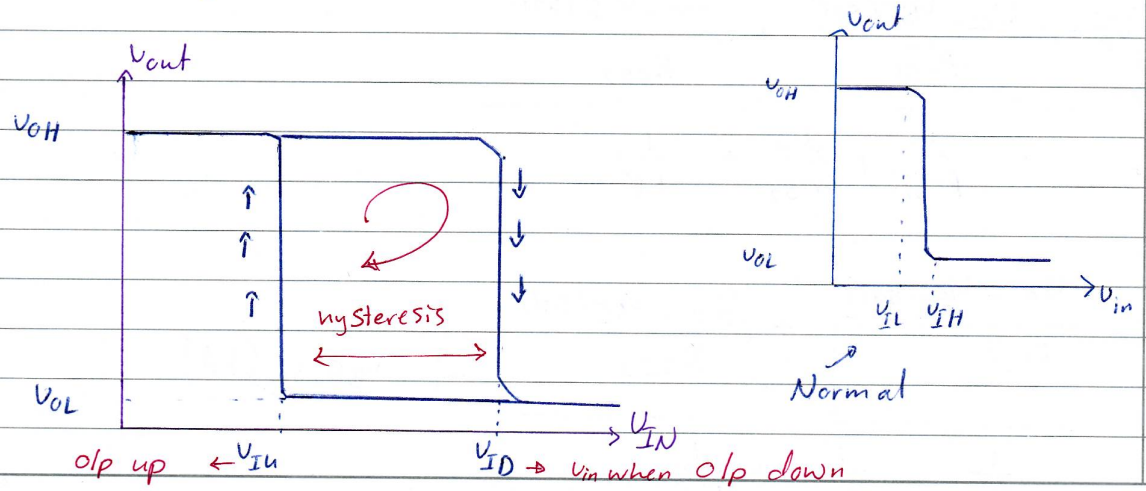
CHAPTER 10: Hysteresis and Schmitt Triggers.



o/p of an inverting schmitt trigger.

o/p high_to_low and o/p low_to_high transition occurs at different input voltages.

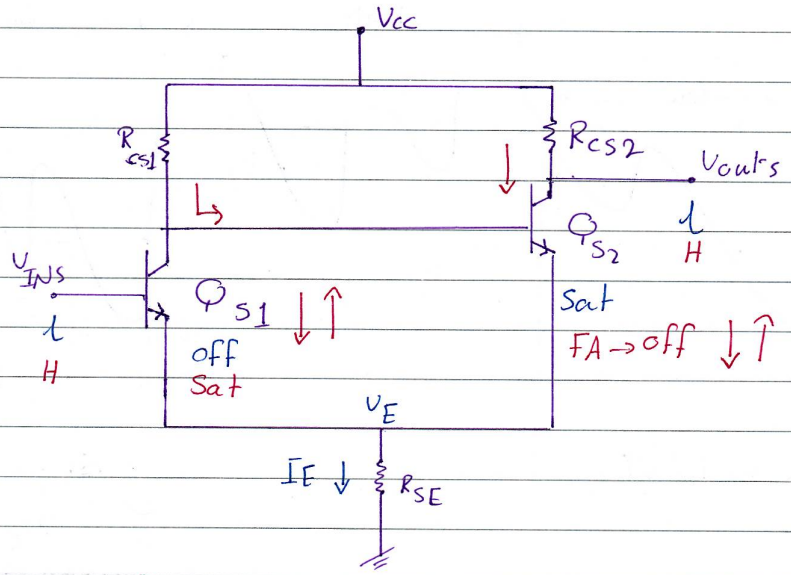
hysteresis = $V_{ID} - V_{IU} \Rightarrow V_{IU} < V_{ID}$

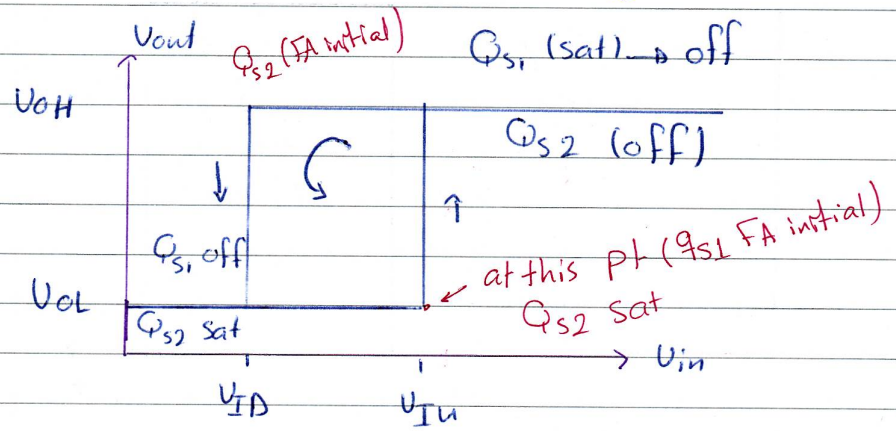


20-12-2016 Tuesday

Emitter coupled schmitt trigger.

Non-Inverting:





$$\Rightarrow V_{OL} = V_{CE_2}(sat) + V_E$$

$$I_{BS_2} + I_{CS_2} = I_{ES_2}$$

$$V_E = \frac{\frac{V_{cc} - V_{BE}(sat)}{R_{cs1}} + \frac{V_{cc} - V_{CE}(sat)}{R_{cs2}}}{\frac{1}{R_{cs1}} + \frac{1}{R_{cs2}} + \frac{1}{R_E}}$$

$$\Rightarrow V_{IUS} = \frac{\frac{V_{cc} - V_{BE}(sat)}{R_{cs1}} + \frac{V_{cc} - V_{CE}(sat)}{R_{cs2}}}{\frac{1}{R_{cs1}} + \frac{1}{R_{cs2}} + \frac{1}{R_E}} + V_{BE,S_1}(FA)$$

20-12-2016 Tuesday

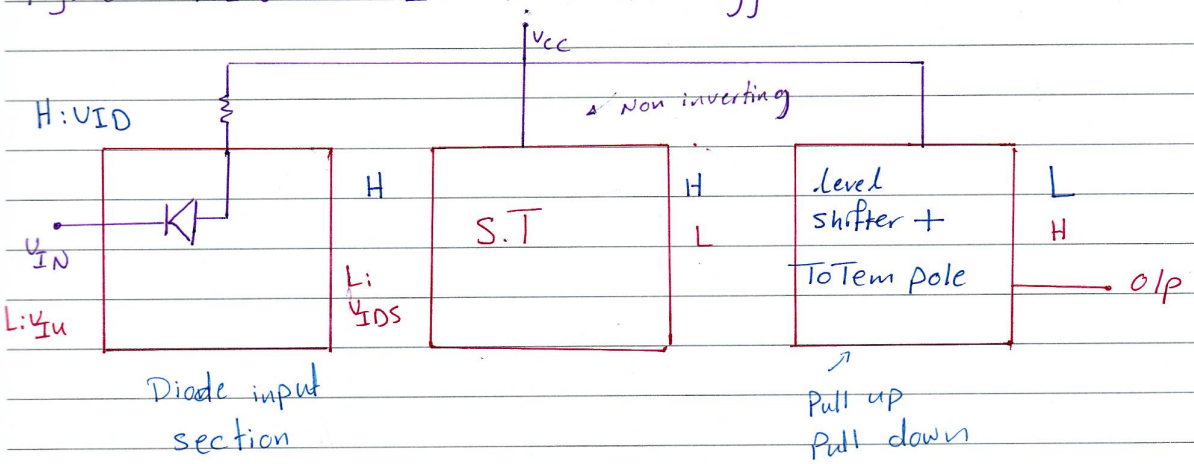
$\Rightarrow V_{OH}$

Q_{S2} off $\rightarrow V_{OH} = V_{cc}$

$\Rightarrow V_{INS}$

$$V_{INS} = V_{IDS} = \frac{V_{cc} + \left(\frac{R_{CS1}}{R_E} + 1\right) V_{BE(sat)} - V_{BE(FA)}}{\frac{R_{CS1}}{R_E} + 1}$$

Figure 10_10 : TTL with schmitt trigger



V_{Iu}, V_{ID} $\Rightarrow$ Trip voltages

$V_{Iu} = V_{IDS} - V_\gamma$ $[V_{IL}]$

$V_{ID} = V_{IUS} - V_\gamma$ $[V_{IH}]$

$V_{OL} = V_{CE(sat)} = 0.2\,V$

$V_{out}(H) = V_{cc} - V_{BE(FA)} - V_\gamma$

$V_{OH} = V_{cc} - 1.4\,V$