تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

الكترونيات رقمية

من شرح:

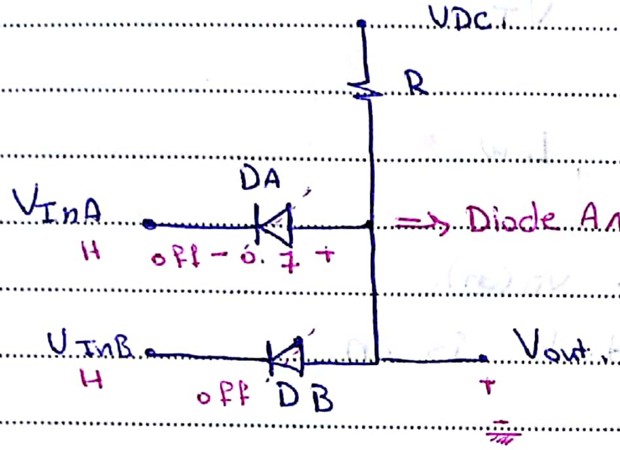
د.رولى طوالبه

جزيل الشكر للطالبة:

روند قطيشات

Subject: ...... 1 / 2 / 2018.

* 2.5 Diode Resistor Logic (DRL) :-



⟹ Diode AND gate.

Low ⟹ Logic 0

H: high ⟹ Logic 1

$V_\alpha = V_D(on) = 0.7$

مفيش Diode يعني H *
off

Diode on ⟸ L

A	B	output
L	L	L
L	H	L
H	L	L
H	H	H

and (out) *

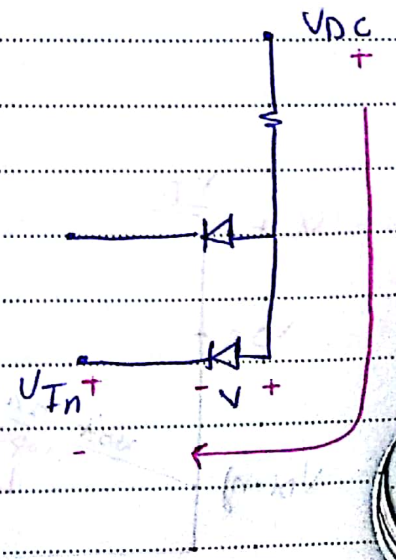
OR (in) *

$$* \; -V_{DC} + V + V_{InB} = 0$$

$$V = V_{In} - V_{DC}.$$

$V > V_D(on) \Rightarrow$ on

$V < V_D(off) \Rightarrow$ off



Subject: 2   / /

$$V_{DC} - V_{In} \underset{off}{\overset{on}{\gtrless}} V_{D(on)}$$

$$V_{DC} - V_{D(on)} \underset{off}{\overset{on}{\gtrless}} V_{In}$$

* Any or all inputs Low :-

1- $V_{In} < V_{DC} - V_{D(on)}$

corresponding diode is on.

$$V_{out} = V_{D(on)} + V_{In}$$

if $V_{In} = 0 \Rightarrow V_{out} = V_{D(on)} = V_{OL}$

$$I_R = \frac{V_{DC} - V_{out}}{R} = \frac{V_{DC} - V_{D(on)} - V_{In}}{R}$$

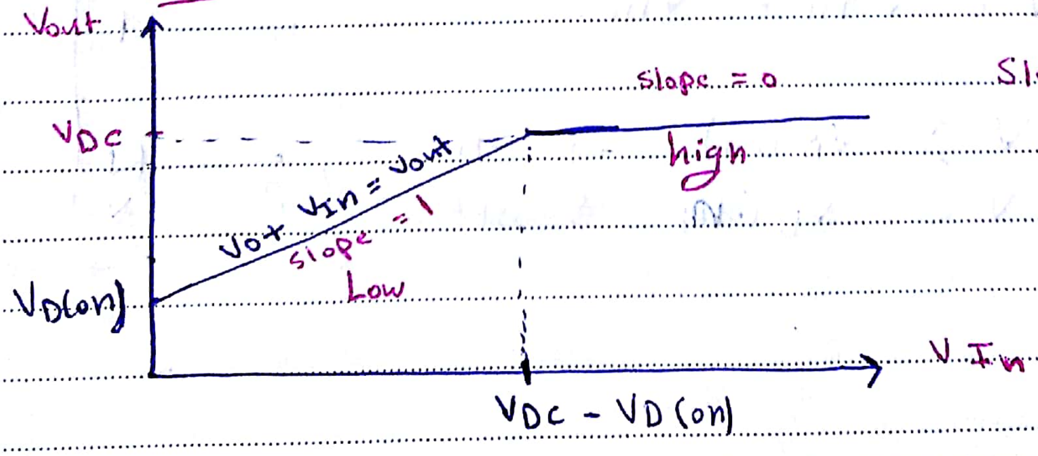
* All inputs high (all diode off)

$$V_{In} > V_{DC} - V_{D(on)}$$

All Diodes off.

$I_R = 0$, $V_{out} = V_{DC} = V_{OH}$

VTC



$$\text{Slope} \rightarrow \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_{DC} - V_{D(on)}}{V_{DC} - V_{D(on)}} = 1$$

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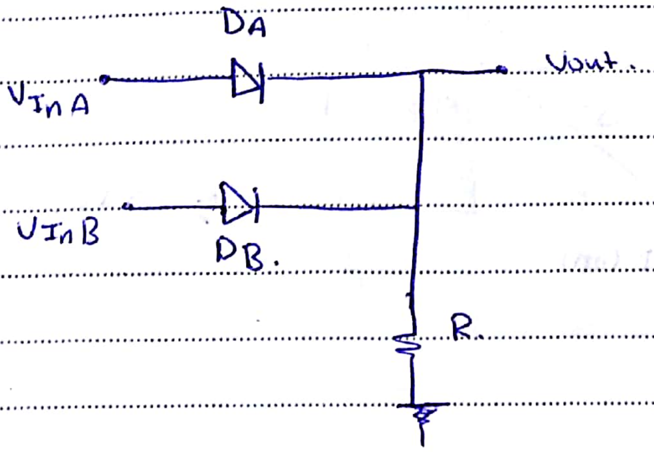
* Diode OR Gate.

* بنحط عدد Input نضيف Diode



$V_{In} > V_D(on) \Rightarrow on.$

$V_{In} < V_D(on) \Rightarrow off.$

A	B	out.
L	L	L
H	L	H
L	H	H
H	H	H

① All input Low: (All Diode: off).

$I_R = 0$, $V_{out} = 0 = V_{oL}$, $V_{In} < V_D(on)$

② Any or all input high (corrisponding didoe on).

$V_{out} = V_{In} - V_D(on).$

$V_{In} > V_D(on).$

$$I_R = \frac{V_{out}}{R} = \frac{V_{In} - V_D(on)}{R}$$

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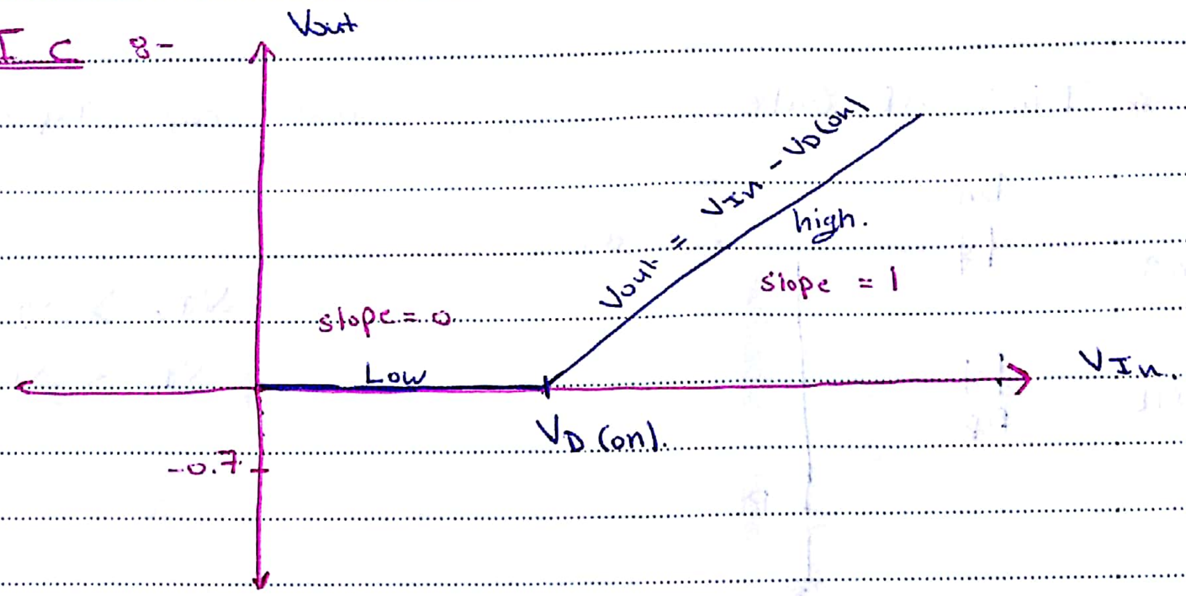
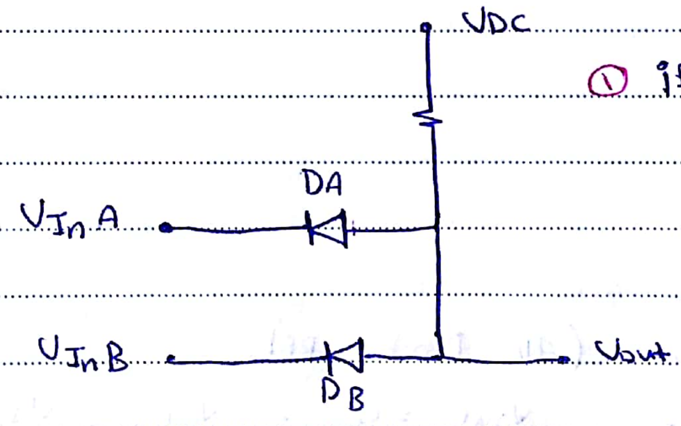
* VTC :-



* Logic Function ⇒ A or B.

* Example :- (2.3)



① if VIn A is higher than VIn B by 1 V
Show that DA is off.

∴ VIn A = 1 + VIn B

① Assume DA on.

Vout = VDA + VIn A = 0.7 + VIn A

VDB = Vout − VIn B
= 0.7 + VIn A − VIn B
= 0.7 + 1 + ~~VIn B~~ − ~~VIn B~~

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$V_{DB} = 1.7$, inapplicable and assumption that D_A is on is incorrect.

D_A is off.

(2) Assume D_B on.

$$V_{out} = V_{InB} + V_{D(on)}$$

$$V_{DA} = V_{out} - V_{InA}$$

$$= V_{InB} + V_{D(on)} - (1 + V_{InB})$$

$$= \cancel{V_{InB}} + V_{D(on)} - 1 - \cancel{V_{InB}}$$

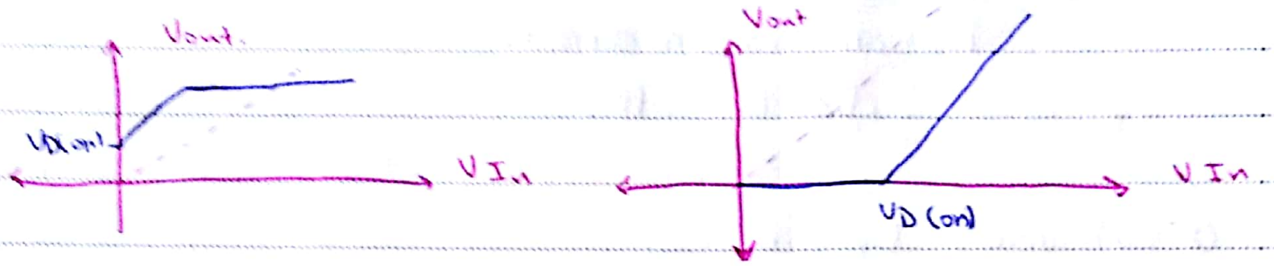
$$V_{DA} = 0.7 - 1 = -0.3$$

$\Rightarrow$ D_A off, and assumption that D_B is correct.

* عشان الـ ٢ بيشتغلو لازم تكون $V_{InA} = V_{InB}$

*

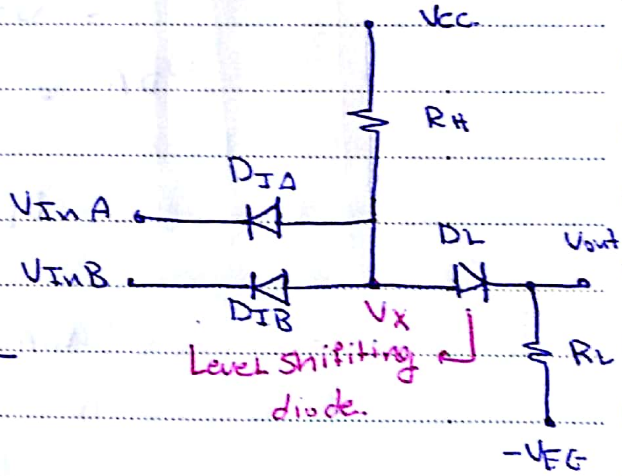
* 2.6 Level Shifted DRL :-



* Degradation : reduction or increase of V_{out} by $V_D(on)$ with respect to V_{In}

حتى تبلش زيادة من صفر لازم $V_D(on)$ تصير صفر.

* Level Shifted AND Gate :-



① All input high

$V_{In} > V_x - V_D(on)$

Both Diode off.

$$I_R = \frac{V_{CC} + V_{EE} - V_{DL}}{R_H + R_L}$$

$V_{out} = I_R R_L - V_{EE}$ **oR** $V_{out} = V_{CC} - I_R R_H - V_{DL}(on)$ ...①

② Any input Low.

$V_{In} < V_x - V_D(on)$.

Corresponding input Diode is on.

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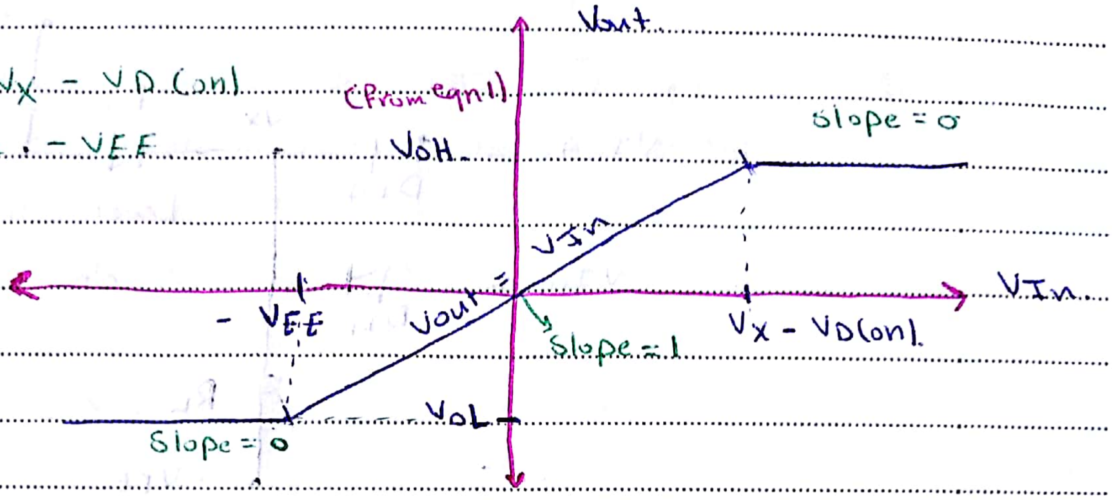
$\begin{cases} V_{OH} = V_X - V_{D(on)} \\ V_{OH} = -V_{EE} \end{cases}$



① $V_X > V_{D(on)} - V_{EE}$, D_L on.

2.a $V_{In} + V_{D(on)} > V_{D(on)} - V_{EE}$

$$V_{In} > -V_{EE}$$

$$-V_{In} - V_{D(on)} + V_{DL(on)} + V_{out} = 0$$

$$V_{In} = V_{out}$$

2.b $V_{In} < -V_{EE}$

$V_X < -V_{EE} + V_{D(on)}$, D_L is off.

$I_{RL} = 0$

$$V_{out} = I_R R_L - V_{EE} = -V_{EE}$$

* Level Shifted OR Gate :-

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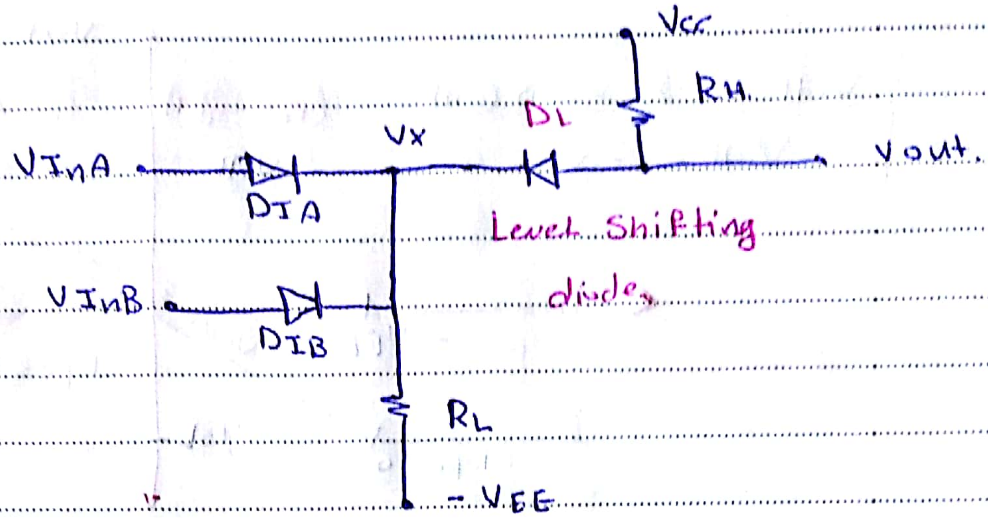


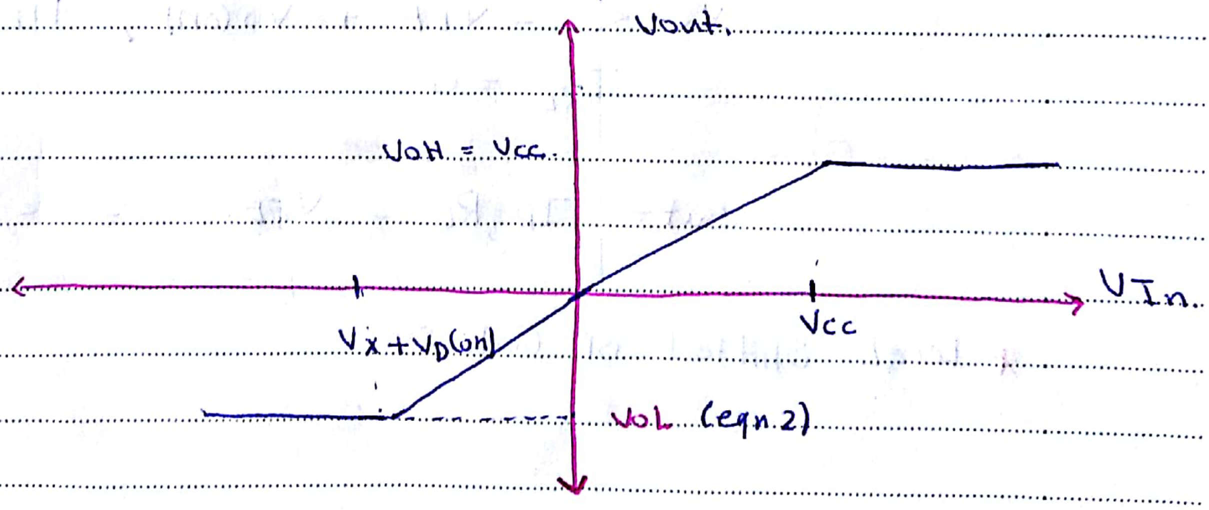
① All Input $V_{In} < V_X + V_D(on)$

Both input diodes off.

$$I_R = \frac{V_{CC} + V_{EE} - V_D(on)}{R_L + R_H}$$

$$V_{out} = V_{CC} - I_R R_H$$

$$= V_{DL}(on) + I_R R_L - V_{EE} = V_{OL} \text{ --- eqn ②}$$



② $V_{In} > V_x + V_{DI}(on)$ (Any or All inputs).
Corresponding input diode conducts.

2.a $V_x < V_{cc} - V_{DL}(on)$ (DL is on).

$V_{In} - V_{DI}(on) < V_{cc} - V_{DL}(on)$ (the "(on)" terms are crossed out)

$V_{In} < V_{cc}$.

$V_{out} = V_{In}$.

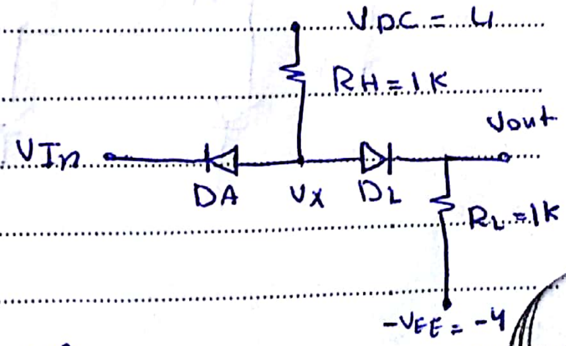
2.b $V_{In} > V_{cc}$. (DL off).

$V_{out} = V_{cc} = V_{OH}$.

* Example 2.4 مطلوب

* 2.7 clamping diode.
* 2.8 Level Shifting diode.

problem * 2.18 :-
For $-4 < V_{In} < 4$
Draw VTC.



① $V_{In} > V_x - V_D(on)$.
DI off,

$I_R = \frac{8 - V_D(on)}{2k} = 3.65$ mA.

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* ممكن يجيب شبه OR gate.

$V_{out} = 1k \times (3.65m) - 4$

$= -0.35\ V = V_{OL}$.

2- $V_{In} < V_x - V_D(on)$. (D_I is on).

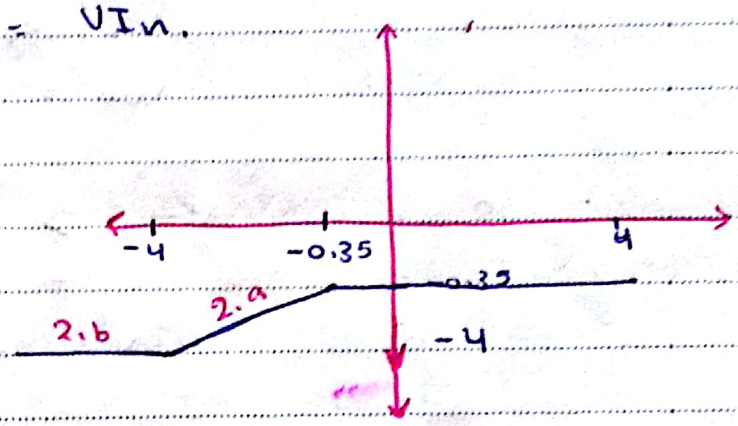
2.a $V_{In} > -4 = V_{DC}$, D_L on.

$V_{out} = V_{In}$.

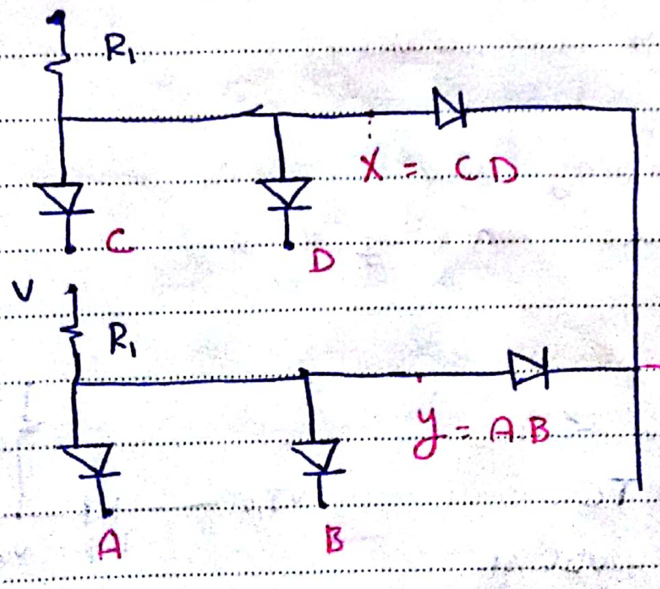
2.b $V_{In} < -4$.

D_L off.

$V_{out} = -4$.



* سؤال امتحان



Logic function.

Z = CD + AB

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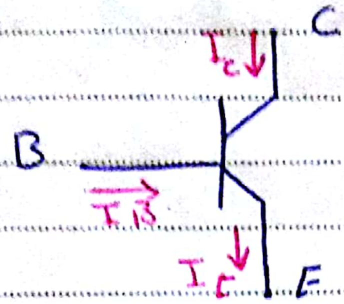
* Chapter 4 : Introduction to Bipolar Digital Circuits.

4.1 Analysis of BJT (operation modes)



① cut off

(B-E) J } Both reverse
(B-C) J } baised.

currents = 0.

② Forward Active (FA).

(B-E) J Forward

(B-C) J. Reverse

V_{BE} (FA) = 0.7

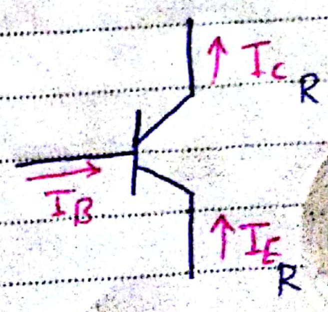
$$I_C = \beta \, I_B$$

$$I_E = I_C + I_B = (1+\beta) \, I_B$$

③ Reverse Active (RA).

(B-E) J Reverse

(B-C) J Forward.



* $-I_C = I_B - I_E$ لو اعطيته تيار I_E في حالة

FA ⟸ بعكس اشارة في RA.

$-I_E = \beta_R I_B$

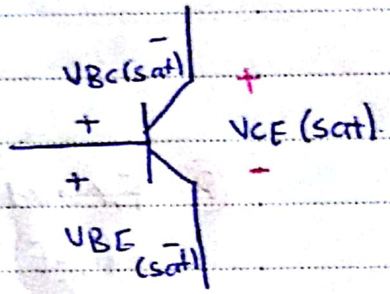
$-I_C = (1+\beta_R) I_B$

$\beta_R << \beta_F$

④ Saturation mode

(B−E) J & (B−C) J ⟹ Forward.

$I_E = I_C + I_B$



$I_C \neq \beta_F I_B$

$I_C = \sigma \beta_F I_B$, $\sigma \leq 1$

$V_{CE(sat)} = 0.2$

$V_{BE(sat)} = 0.8$

$V_{BC(sat)} = V_{BE(sat)} - V_{CE(sat)}$

$= 0.8 - 0.2 = 0.6\ V$

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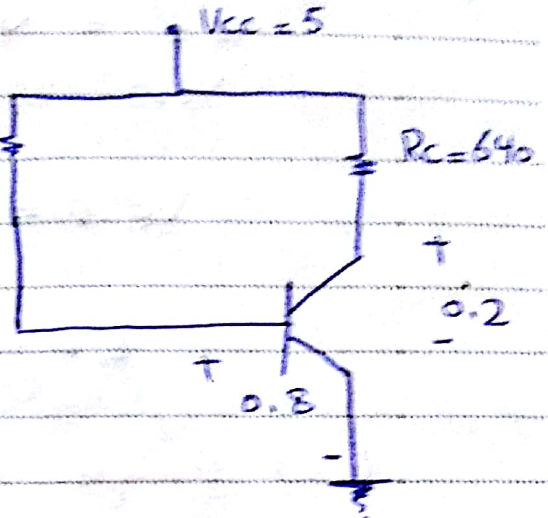
* Example 4.1



⇒ Q_o is in sat mode
Find I_B, I_C and σ :-

$$-5 + I_B R_B + 0.8 = 0$$

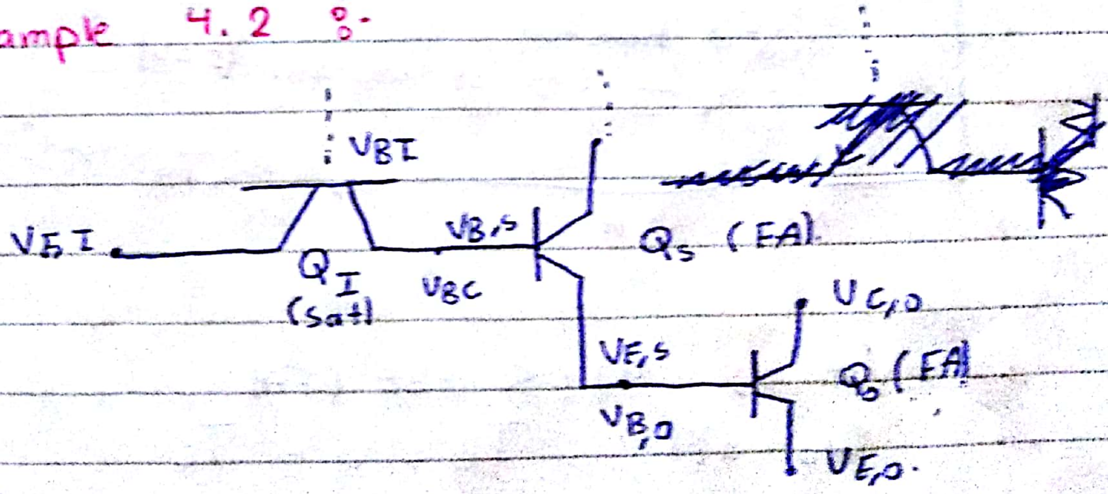
$$I_B = \frac{5 - 0.8}{5} = 840 \mu A.$$

$$I_C = \frac{5 - 0.2}{640} = 7.5 \ mA.$$

$$I_C = \sigma \beta_F I_B.$$

$$\sigma = \frac{I_C}{\sigma \beta_F} = 0.137.$$

* Example 4.2 :-



$V_{E,o}$ = Zero.

$V_{E,s} = V_{B,o} = 0.7$

$V_{B,s} = 2\ V_{BE} = 1.4$

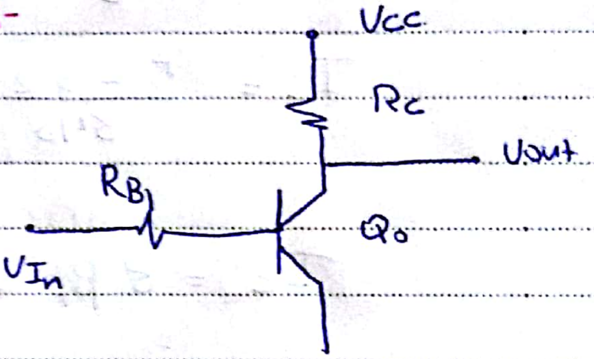
$V_{E,I} = 2\ V_{BE}(FA) - V_{C,E}(sat) = 1.2$

$V_{B,I} = V_{E,I} + V_{BE_I}(sat) = 1.2 + 0.8 = 2.$

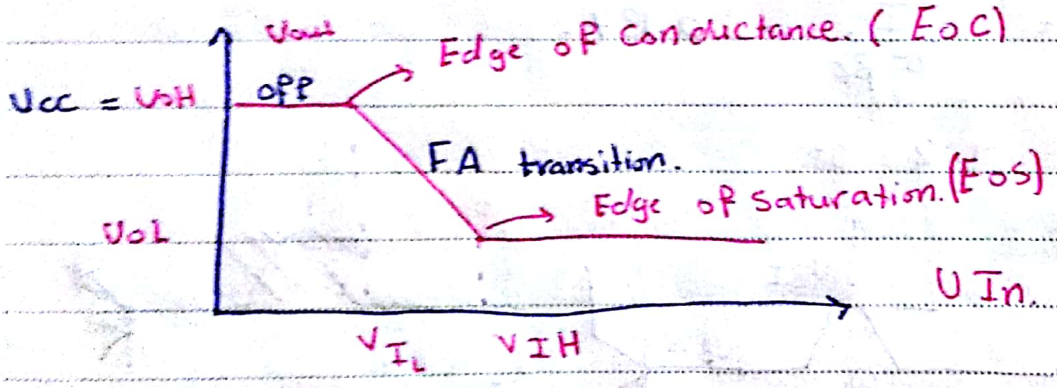
Read Exmple (4.3)

* 4.2 BJT Inverter :-

CE.(common Emiter)



VTC



1- VoH ⇒ $V_{In} < V_{BE}$ (FA).

Q_o off , $I_B = 0 = I_C$

$V_{out} = V_{cc} = V_{oH}$

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2. V_{IL} (input that turns Q_o on FA).

$V_{IL} = V_{BE}$ (FA), Since initially $I_B = 0$ at Edge of conductance.

As input increase, I_B increase, and I_C increase, and Vout decrease.

3. For higher input, Q_o Saturate, and

$$V_{out} = V_{OL} = V_{CE(sat)}.$$

* V_{IH} (voltage at which Q_o saturates EoS)

$$V_{IH} = I_B (EoS) R_B + V_{BE,o}(sat).$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}.$$

$$I_B(EoS) = \frac{I_C}{\beta_F} \quad (\sigma = 1 \text{ at } EoS).$$

* V_{IL}, V_{IH}, V_{OL}, V_{OH} = Critical Voltage.

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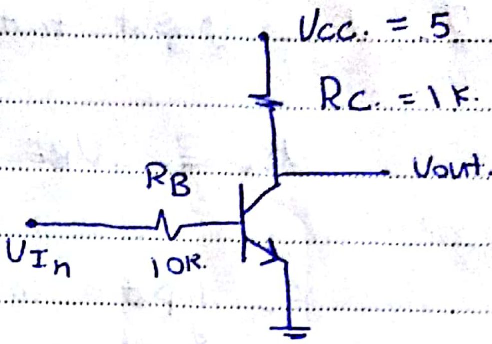
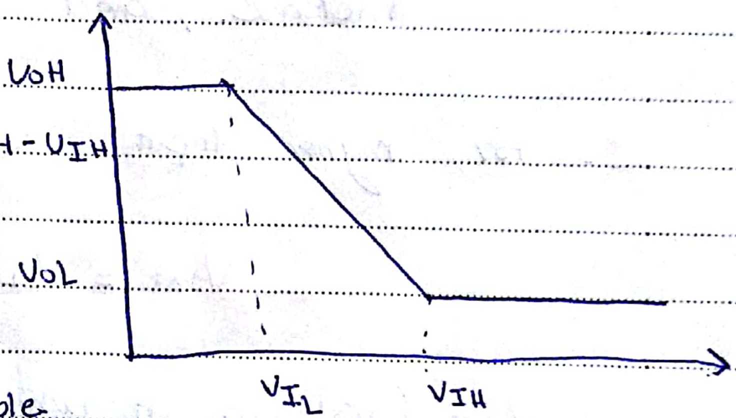
* Example 4.4



$\beta F = 60$

Find the high Low noise margins.



High Noise Margin (HNM) = $V_{OH} - V_{IH}$

~~High~~ Low noise margin (Lnm) = $V_{OL} - V_{IL}$

Sefety margins max affordable noise.

$V_{OH} = V_{cc} = 5$

$V_{OL} = 0.2$

$V_{IL} = 0.7$

$V_{IH} = \frac{5 - 0.2}{1k(60)} \; 10k + 0.8$

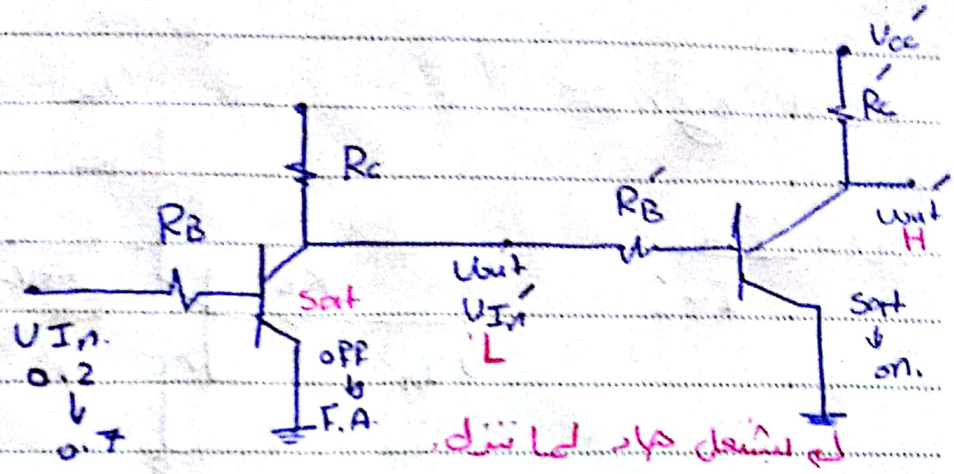
$= 1.6$

$HNM = V_{OH} - V_{IH} = 5 - 1.6 = 3.4$

$LNM = V_{OL} - V_{IL} = 0.7 - 0.2 = 0.5$

pull up → Rc

" down → Qo



لم يشتغل هواد لما نزل

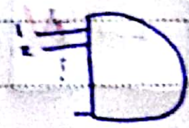
VIn من VIn H حتى يشتغل.

* 4.3 TTL Circuits :-

Block Digram.

pull up, pull down → TTL مشروحين بالكتاب لـ

Fan - in



input عدد مسموح من

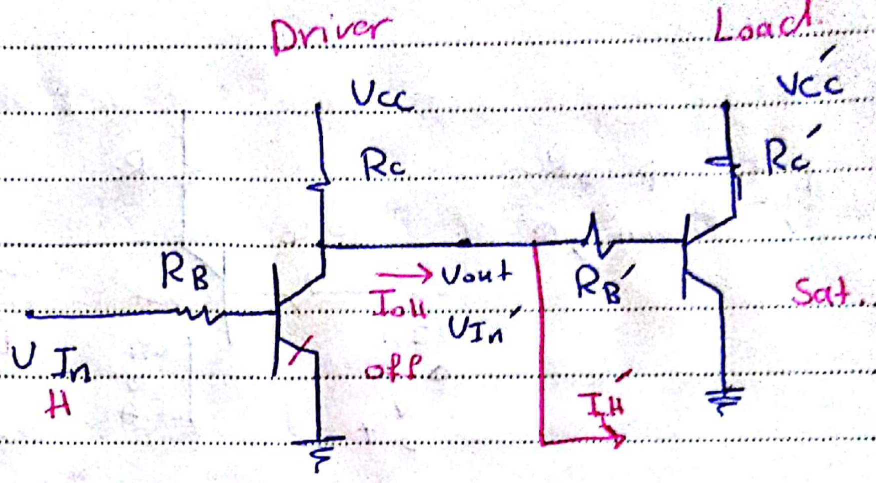
* Fan - in :- max number of inputs at any gate.

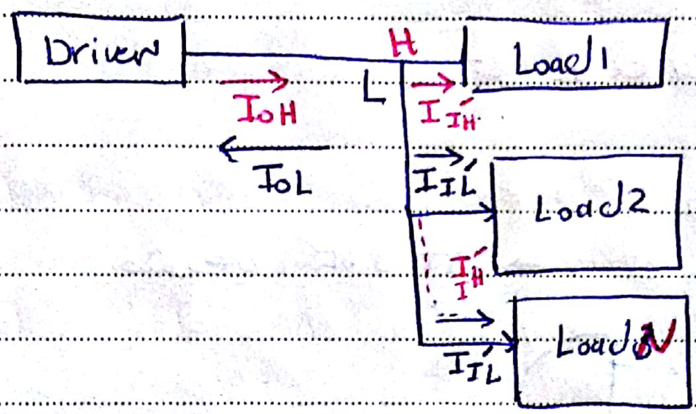
* Fan - out :- maxium number of Load conected at the output of a driver.

* ~~out/trigger~~

* out high :-

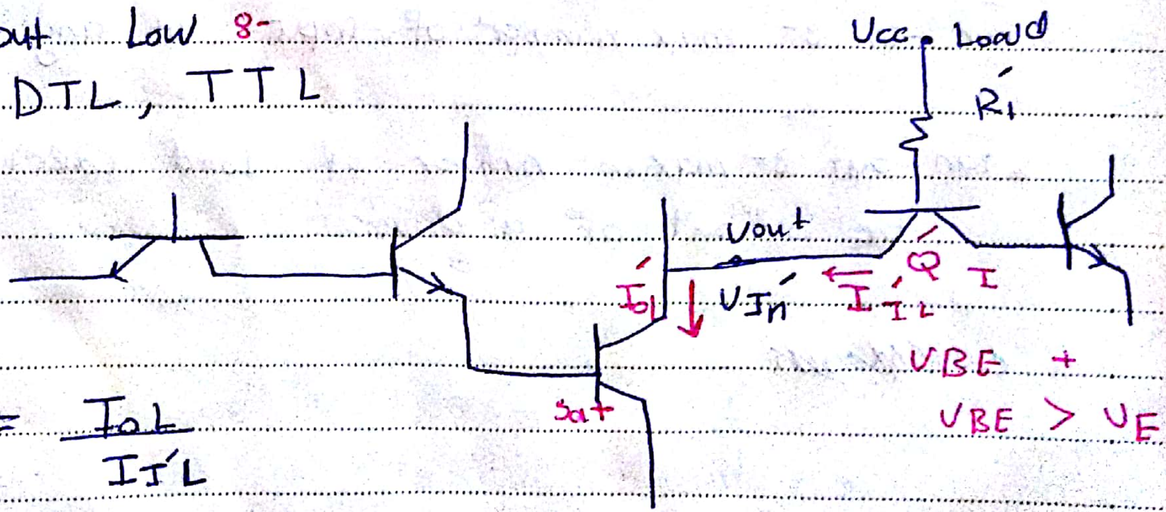
$N = \frac{I_{OH}}{I_{IH}'}$





* out Low :-

DTL, TTL



$N = \frac{I_{OL}}{I_{IL}'}$

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* 4.4 Level shifting BJT :-

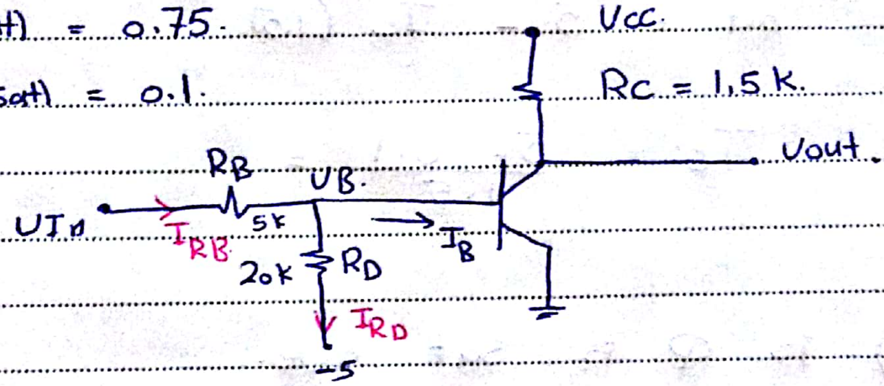
4.5 Discharge path and Base driving ccts.

* ~~Example~~ prop (4.12)

V_{BE} (sat) = 0.75

V_{CE} (sat) = 0.1

$\beta = 100$



a) If $V_{In} = 5$

find I_B.

Assume F.A.

$$I_B = I_{RB} - I_{RD}$$

$$= \frac{5-0.7}{5k} - \frac{0.7+5}{20k} = 0.995 \text{ mA}$$

$$I_c = 100 * 0.995 = 99.5 \text{ mA}$$

$$V_{CE} = V_{CC} - I_c R_c = 5 - 99.5 (1.5) = -ve$$

$\Rightarrow$ Sat.

S T A R S Notebook

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$V_B = V_{BE}(sat) = 0.75.$

$$I_B = \frac{5 - 0.75}{5k} - \frac{0.75 + 5}{20k} = 0.563 \text{ mA.}$$

$V_{CE} = V_{CC} - I_C R_C$

$0.1 = 5 - I_C (1.5).$

$$I_C = \frac{5 - 0.1}{1.5} =$$

b) is Q is sat mode.

c) V_{IL} and V_{IH}.

V_{IL} (EOC).

Initially $I_B = 0$.

$I_{RD} = I_{RB}.$

$$I_{RB} = I_{RD} = \frac{0.7 + 5}{20k} = 0.285 \text{ mA.}$$

$V_{In} - V_B = I_{RB}.$

$V_{InL} = I_{RB} R + V_{BE(F.A)}$

$= 0.285 * 5 + 0.7 = 2.125 \text{ V.}$

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VIH [FOS] σ = 1.

$V_{IH} = I_{RB} R_B + V_{BE(sat)}$.

$I_{RB} = I_B + I_{RD}$.

$I_B = \frac{I_C}{\beta \sigma} = \frac{I_C}{\beta} = \frac{5 - 0.1}{(1.5)(100)(1)} = 0.0327\,mA$.

$I_{RB} = \frac{0.75 + 5}{20} = 0.29$

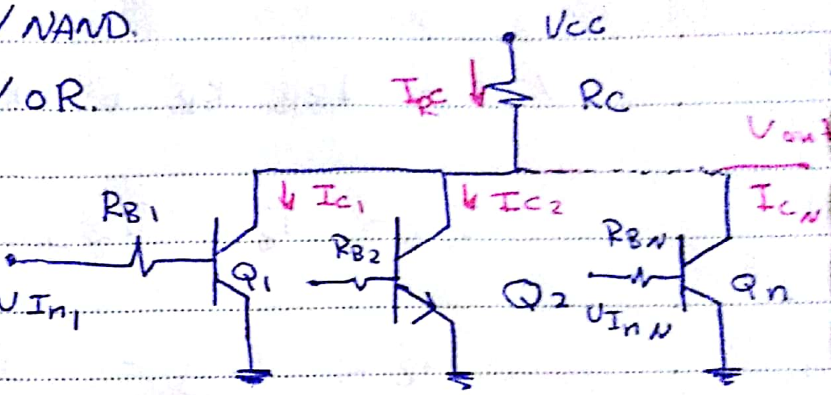
$I_{BR} = 0.29 + 0.0327\,mA$.

$V_{IH} = I_{BR} R_B + 0.75$.

* Chapter 5 RTL :-

npn :- in series AND / NAND.
in perallel NOR / OR.

Pnp :- in series NOR / OR
in parallel AND / NAND



(parralel) NOR.

In general :-

$V_{out} = V_{cc} - I_{Rc} R_c$.

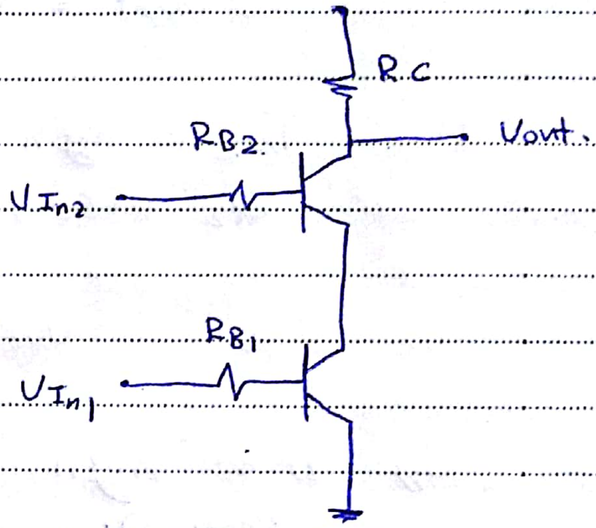
$$I_{Rc} = \sum_{i=1}^{n} I_{c,i} = I_{c1} + I_{c2} + \cdots + I_{cn}.$$

In_1	In_2	In_3	out.
0	0	0	1
0	0	1	0.
0	1	1	0
1	1	1	0

① All inputs Low
All ~~transis~~ tranistors will be off
$V_{out} = V_{cc} = H$

② Any or all inputs high
corresponding transistor saturates.
$V_{out} = V_{CE(sat)} = L$

5.3 Basic RTL NAND Gate.



2 - input NAND Gate.

$V_{out} = V_{cc} - I_{Rc} R_c$.
if Q_1 and Q_2 in F.A.

$I_{E_1} = I_{c_1} = I_{E_2} = I_{c_2}$
$= I_{Rc}$.
↖ I_B neglected

In_1	In_2	out
0	0	1
0	1	1
1	0	1
1	1	0

① Any or all inputs Low.
i.e., all Low, all Q_s off.
$V_{out} = V_a$.

1.b IN$_1$ Low, IN$_2$ high

Q_1 off, Q_2 has no link to ground and is off too.

$V_{out} = V_{cc}$ = high.

1.c IN$_1$ high, IN$_2$ Low.
Q_2 off, Q_1 not power (also off)

$V_{out} = V_{cc}$ = H.

2) both high
when Q_1, turns on (F.A).

$V_{IL_1} = V_{BE}$ (F.A),
when Q_2 turn

$V_{IL_2} = V_{B_2E_2}(FA) + V_{CE,1}$ (sat)

Q_1 saturates at $V_{IH_1} = I_{B_1} R_{B_1} + V_{BE,1}(sat)$
Q_2 " at $V_{IH_2} = I_{B_2} R_{B_2} + V_{BE_2}(sat) + V_{CE}(sat)$.

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- when Q_1 , Q_2 Saturates (input high).

$$V_{out} = 2 V_{CE(sat)}$$

* عند Sat لا يتم تحكم I_B

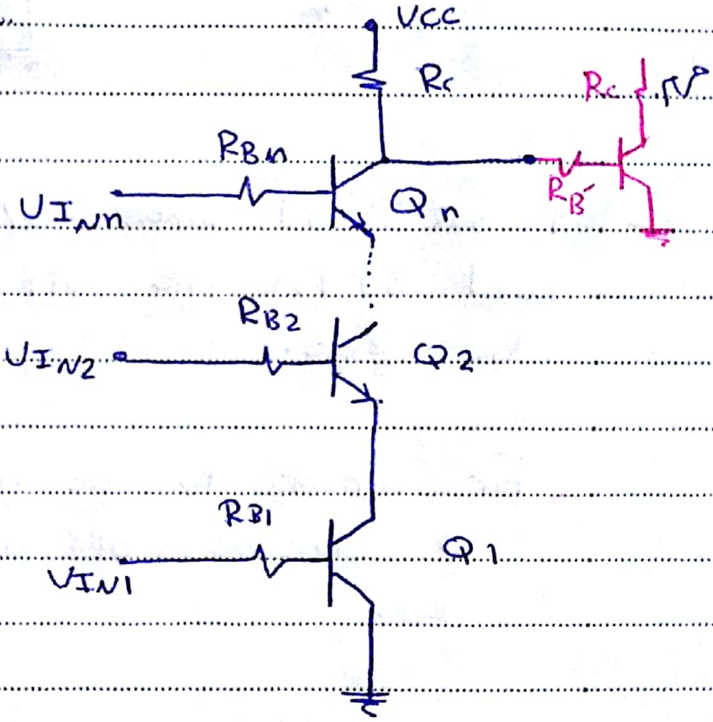
★ Multi-input NAND Gate :-

$V_{out} = V_{cc} - I_{Rc}\ I_c$

$V_{OH} = V_{cc}$.

$V_{OL} = \Sigma V_{CE(sat)}$.

$= n\ V_{CE(sat)}$.



★ Example 5.1 :

Find Fan-in (n = ?)

for Load $V_{BE}(F.A) = 0.7$.

$V_{CE}(sat) = 0.17\ V$ for driver.

بدنا يكون off.

$$n\ V_{CE(sat)} < V_{BE}(F.A).$$

$$n < \frac{0.7}{0.17} = 4.12$$

اقرب عدد صحيح اقل منه .

$n = 4$.

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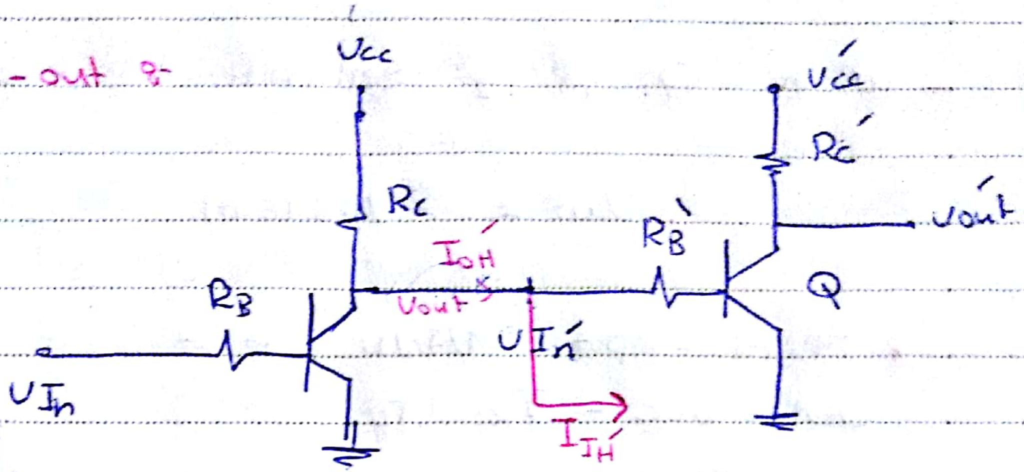
5.4 RTL Fan-out :-

$N = \dfrac{I_{OH}}{I'_{IH}}$



- Fan-out found when o/p high. when output Low, Load BJT,s are off and Input current will be Zero.

- For Driver to be high, Q must be off, for Q to be off input at driver must be Low

* $I_{Rc} = I_{OH} = N I'_{IH}$, $I'_{IH} = I_{R'B}$

بس $V_{out} = V'_{InH}$ حد أقل انه يخلي Q ع sat.

- V_{OH} is limited by V_{IH} for Q to saturate

$V_{out} = V'_{In} = V_{cc} - I_{Rc} R_c$.

$I_{Rc} = I_{OH} = \dfrac{V_{cc} - V_{OH}}{R_c}$,

$$I'_{IH} = I_{RB'} = \frac{V_{out} - V_{BE}(sat)}{R_B}.$$

$$N = \frac{V_{cc} - V_{out}}{V_{out} - V_{B\acute{E}}(sat)} \cdot \frac{R_B}{R_C}$$

$$V_{out} = V_{IH}' = I_B'(EOS)\, R_B' + V_{B\acute{E}}(sat).$$

$$I_B' = \frac{V_{c\acute{c}} - V_{C\acute{E}}(sat)}{R'_c\ (\beta)}, \quad (\sigma = 1) \text{ at EOS.}$$

* Read Example 5.2 ($N = 12.1 \approx 12$).

* RTL power Dissipation.

no Load.

output high (input Low) Q is off.

$$I_{cc}(OH) = I_{Rc} = 0.$$

output Low (input high) Q is saturation

$$I_{cc}(OL) = \frac{V_{cc} - V_{CE}(sat)}{R_c}.$$

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$$- P_{cc}(avg) = \frac{I_{cc}(oH) + I_{cc}(oL)}{2} V_{cc}$$

* with Load :-

output high, Q (Driver) is off, Q′ (Load) saturates

$$I_{Rc(oH)} = N I_B' = I_{cc}(oH)$$

$$= N \left(\frac{V_{IH}' - V_{BE}'(sat)}{R_B} \right)$$

$$= N \left(\frac{V_{cc} - I_{Rc} R_c - V_{BE}'(sat)}{R_B} \right)$$

$$I_{Rc} + \frac{I_{Rc} R_c}{R_B'} N = \frac{V_{cc} - V_{BE}'(sat)}{R_B'} N$$

$$I_{Rc} = \frac{V_{cc} - V_B'(sat)}{\left(1 + \frac{N R_c}{R_B'}\right) R_B'} N$$

$$= \frac{V_{cc} - V_B'(sat)}{(R_B' + N R_c)} N$$

$$= \frac{V_{cc} - V_B'(sat)}{\frac{R_B'}{N} + R_c}$$

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* out Low :-

$$I_{CC}(OL) = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

Load → off
ليس لها تأثير

Example 5.3

* find avarge power Dissipation.
  a) no Load.
  b) $N=1$ (one gate), $V_{CC}=5$, $R_B=10$.
  $R_C = 1K$, $\beta_F = 25$, $V_{BE}(sat) = 0.8$
  $V_{CE}(sat) = 0.2$.

a) no Load.

$I_{CC}(OH) = 0$.

$$I_{CC}(OL) = \frac{5-0.2}{1K} = 4.8\,mA.$$

$$P_{CC}(avg) = \frac{0 + 4.8m}{2} \times 5 = 12\,mW.$$

b) with Load $N=1$

$I_{CC}(OL) = 4.8\,m$ (same as no Load Q' is off)

$$I_{CC}(OH) = \frac{5-0.8}{1K + \frac{10K}{1}} = 382\,\mu A. = 0.382\,mA.$$

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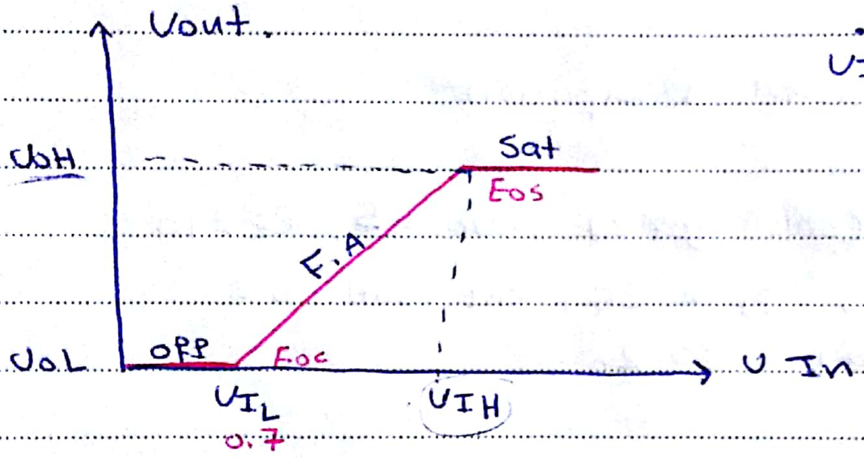
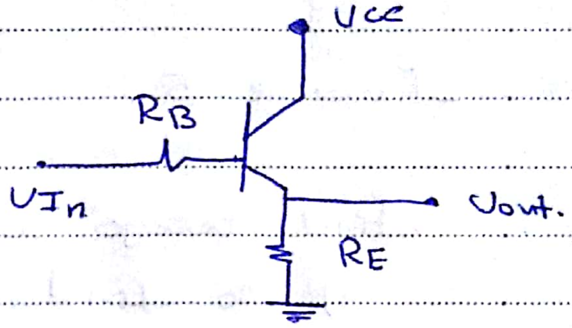
P_{cc} (avg) = $\frac{4.8m + 0.382m}{2}$ × 5 = 12.96 mW.

* 5.6 Basic RTL inverter :-

CC = Emite F.





1- VoL ⇒ Input < VBE (F.A), Q is off

$I_E = 0$.

$V_{out(OL)} = I_E R_E = 0$.

2- V_{IL} (when Q turns F.A)

$V_{IL} = V_{BE}$ (F.A).

* when Q is FA, I_B & I_E start to increase

$V_{out} = I_E R_E$ increaces as input increase.

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Input keeps increasing until Q saturates at V_{IH}.

③ $V_{OH} \Rightarrow V_{OH} = V_{CC} - V_{CE(sat)}$ Eos.

× V_{IH} (Eos)

$$V_{IH} = I_B R_B + V_{BC(sat)} + V_{CC}$$

$$I_B = \frac{I_E}{\beta+1} \quad \text{Eos } (\sigma=1)$$

$$I_E = \frac{V_{CC} - V_{CE(sat)}}{R_E}$$

$$V_{IH} = \frac{V_{CC} - V_{CE(sat)}}{\beta+1} \cdot \frac{R_B}{R_E} + V_{BC(sat)} + V_{CC}$$

OR

$$-V_{IH} + I_B R_B + V_{BE(sat)} + I_E R_E = 0$$

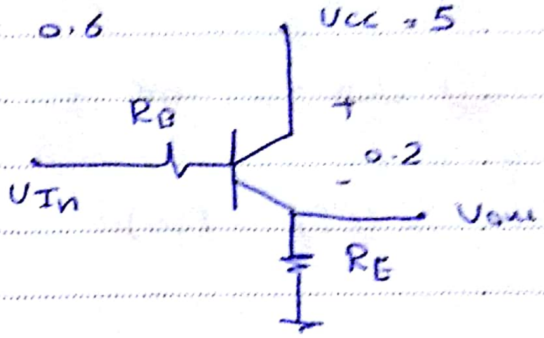
$$V_{IH} = I_B R_B + V_{BE(sat)} + I_E R_E$$

$V_{IH} > V_{CC} \Rightarrow$ sat كده بعمل ممكن
لازم تعطيه ضمانة اعلى

* Example (5.4) :

$V_{BE(sat)} = 0.8$, $V_{BC(sat)} = 0.6$

$\beta_F = 25$, $R_B = 10k$.



$V_{IL} = 0.7$

$V_{OL} = 0$.

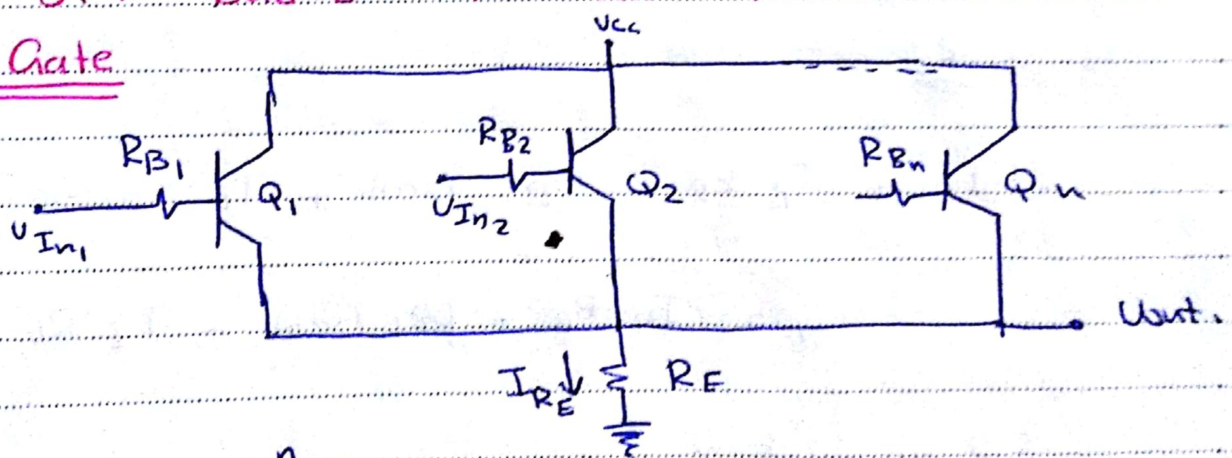
$V_{OH} = 5 - 0.2 = 4.8$.

$V_{InH} = \frac{5 - 0.2}{26} \left(\frac{10}{1} \right) + 0.6 + 5$.

$= 7.4$

5.7 Basic "OR" and "AND" Gates.

OR Gate



$$I_{RE} = \sum_{i=1}^{n} I_{Ei}$$

$$V_{out} = I_{RE} R_E = V_{CC} - V_{CE}$$

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* All inputs Low (Logic 0).

All Q's off.

$I_B = I_E = I_{RE} = 0$.

$V_o = 0$.

* Any (or all) inputs high

(Logic 1), corresponding

Q saturates

$V_{out} = V_{cc} - V_{CE(sat)}$.

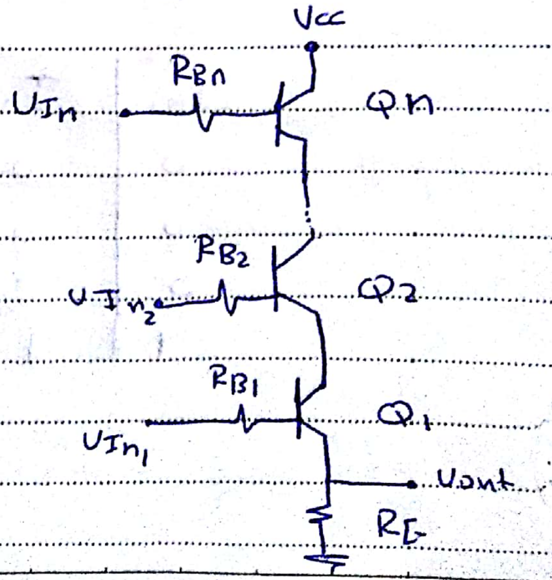
In_1	In_2	In_3	out
0	0	0	0
0	0	1	1
0	1	1	1
1	1	1	1

* AND gate :-

- In general

$V_{out} = I_E R_E$

$= V_{CC} + n\ V_{CE}$



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* Any or all inputs Low.
  Corresponding Q is off

$V_{out} = 0$ (Logic 0) $I_{RE} = 0$.

* All inputs high.
  2 - input AND Gate.

If Q_2 is F.A and Q_1 Sat ~~V_{out}~~

$V_{out} = V_{cc} - V_{CE_2}$ (F.A) $- V_{CE_1}$ (sat).

if both Saturates.

$V_{OH} = V_{cc} - 2 V_{CE}(sat)$.

- If n transistors.

$V_{OH} = V_{cc} - n V_{CE}(sat) \geq V_{IH}$.

Logic input at 1 Logic output at 1

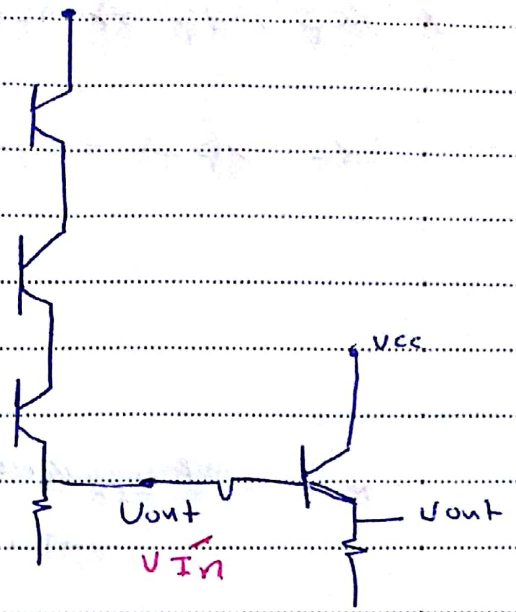
In1	In2	In3	out
0	0	0	0
0	0	1	0
0	1	1	0
1	1	1	1

- $V_{In} \Rightarrow$ high

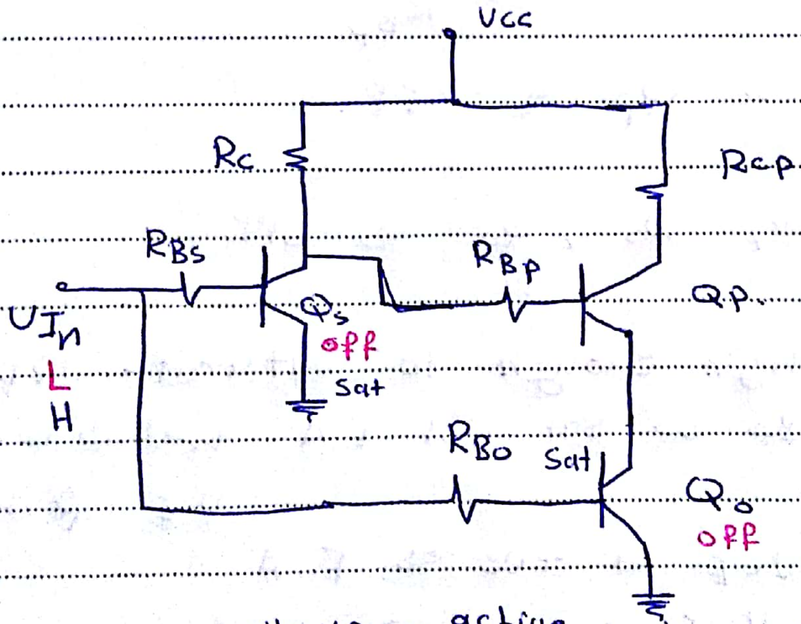
  $V_{out} \Rightarrow$ high (Sat)

  $V_{out} > V'_{InH}$ (Load).

  inverter.



* 5.8 RTL with active pull-up.



* $R_{BS} = R_{Bo} = R_B$ for Q_s and Q_o to opperate at the same time

pull up - active

لـ لانه بجيب high من خلال Q_P

* لو كانت هيجيب active من خلال مقاومة هيبقى pull up passive ,

* R_{cp}, Q_p ⇒ Active pull-up cct.

Q_o ⇒ pull-down, Sink ⇒ (Load)

V_{out} (Low) Load (off)

لما يسحب تيار في Q_o لازم sat

* input high, Q_s, Q_o are saturating.

$$-V_{CE,s}(sat) + I_B R_{Bp} + V_{BE,p}(?) + V_{CE,o}(sat) = 0$$

$$I_B = -\frac{V_{BE,p}(?)}{R_{Bp}}$$

∴ Q_p ⇒ off.

* input Low, Q_s, Q_o ⇒ off.

I_B high enough to Saturate Q_p.

لازم نتأكد اننا F.A او sat من خلال حساب I_B

من قيم V_{CE}

V_{CE} ⇒ +ve ⇒ F.A

V_{CE} ⇒ -ve ⇒ sat.

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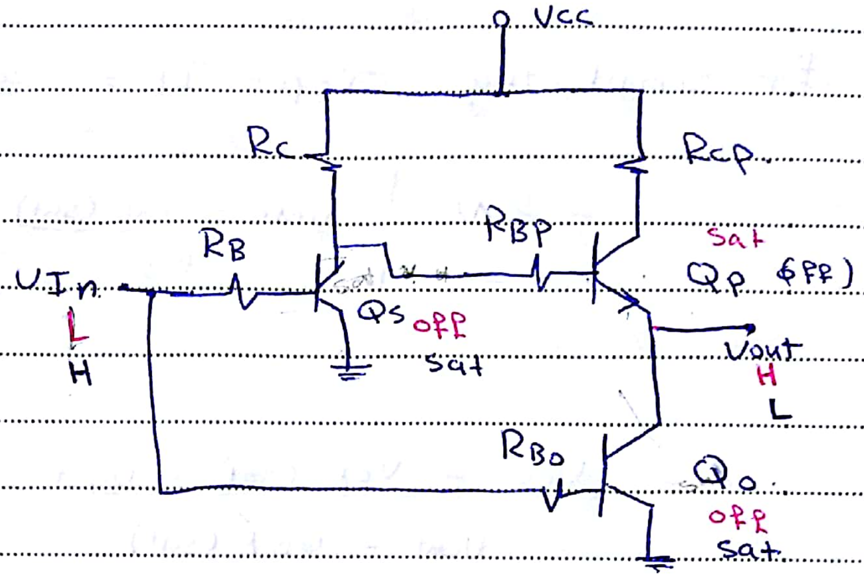
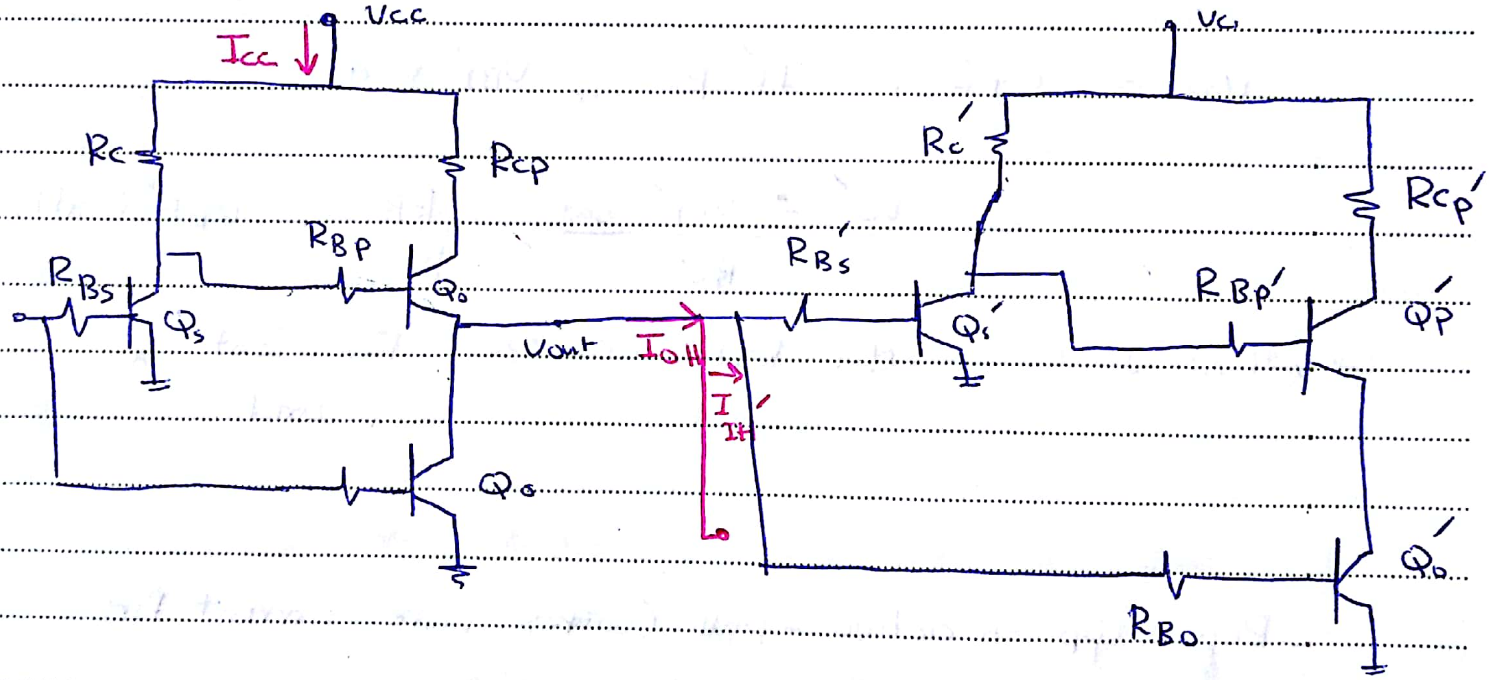
* 5.8 Cont.

$R_{cp} \approx 0.1 R_c$





* Fan out is limited by Vout which is limited by V_{IH}' ∴

$N = \frac{I_{OH}}{I_{IH}'}$

$I_{OH} = N I'_{IH} = 2N I'_B$

for simplicity $I_{cp} = I_E = \frac{V_{cc} - V_{CE,P(sat)} - V_{OH}}{R_{cp}}$

$= 2N \left[\frac{V_{OH} - V_{BE}'(sat)}{R_B} \right]$.

$N = \frac{V_{cc} - V_{CE}(sat) - V_{out}}{V_{out} - V_{BE}'(sat)} \cdot \frac{R_B'}{2 R_{cp}}$.

$V_{out} = V_{IH}' = I_B' R_B + V_{BE}'(sat)$.

$= \frac{V_{cc}' - V_{CE}'(sat)}{R_c'} \cdot \frac{R_B}{\beta_F'} + V_{BE}'(sat)$.

* Fan - out اعلى من RTL اعلى تقدر اوصل عدد اكبر من Load.

- Rcp - Qp ⇒ active - pull (soures more current for Load).

- Read Example 5.5. *

* 5.11 , 4-20, 4.4, 5.17, 4.22 *

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/ /

* 5.32

$R_{cp} = 100$, $R_C = 3.6K\ \Omega$, $R_{BP} = 1.5K$

$R_{BS} = 1.5\ K$, $\beta_F = 100$

find I_{Bp}, I_{cp}, V_{out}.

for $N = 4$.

a) $V_{In} = 0\ V$.

$$N = \frac{V_{cc} - V_{CE}(sat) - V_{out}}{V_{out} - V_{BE}(sat)} \quad \frac{R'_{BP}}{2R_{cp}}$$

$$4 = \frac{5 - 0.2 - V_{out}}{V_{out} - 0.8} \times \frac{1.5}{2 \times 100}$$

$V_{out} = 3.4\ V.$

$$I_{Rc} = I_{Bp} = \frac{5 - 0.8 - 3.4}{(1.5 + 3.6)\ K} = 0.157\ mA.$$

$$I_{Rcp} = \frac{5 - 0.2 - 3.4}{100} = 14\ mA.$$

$I_{cc}(oH) = I_{Rc}(oH) + I_{Rcp}(oH)$

$= 14 + 0.157 = 14.157$ mA

b) $V_{In} = 5$ volt.

Q_s & $Q_o \rightarrow$ sat $Q_p \rightarrow$ off

$$I_{Rc} = \frac{V_{cc} - V_{CE(sat)}}{R_c} = \frac{5 - 0.2}{3.6\,k} = 1.33 \text{ mA.}$$

$I_{RBP} = 0.$

$I_{Rcp} = 0.$

$I_{cc}(oL) = I_{Rc}(oL) = 1.33$ mA.

$V_{out} = V_{CE}(oL) = 0.2.$

5. Q/o : Find the Avg power dissipation.

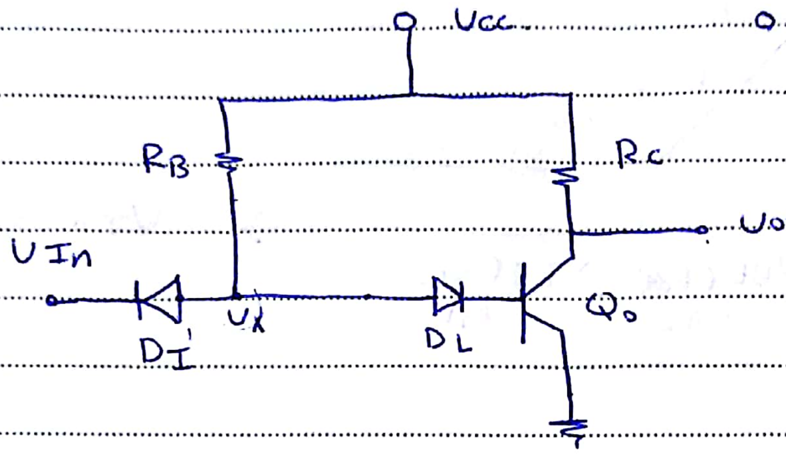
$$P_{cc}(avg) = \frac{I_{cc}(oH) + I_{cc}(oL)}{2} V_{cc}$$

$$= \frac{1.33 + 14.16}{2} \times 5 = 38.7 \text{ mW.}$$

Subject: 4.1 19/2/2018

* Chapter 6 Diode transistor Logic (DTL).

– 6.1 Basic DTL.



– $V_{IN} < V_X$, D_I on.

$V_X = V_{DI} + V_{IN}$

$V_X = V_{DL} + V_{BE}$ (F.A).

* V_{OH} ⇒ $V_X < V_{DL} + V_{BE}$ (F.A)

D_L , Q_o off.

$I_{RC} = 0$, $V_{out} = V_{OH} = V_{CC}$.

$V_{DI} + V_{IN} < V_{DL} + V_{BE}$ (F.A)

$V_{IN} < V_{BE}$ (F.A).

S T A R S

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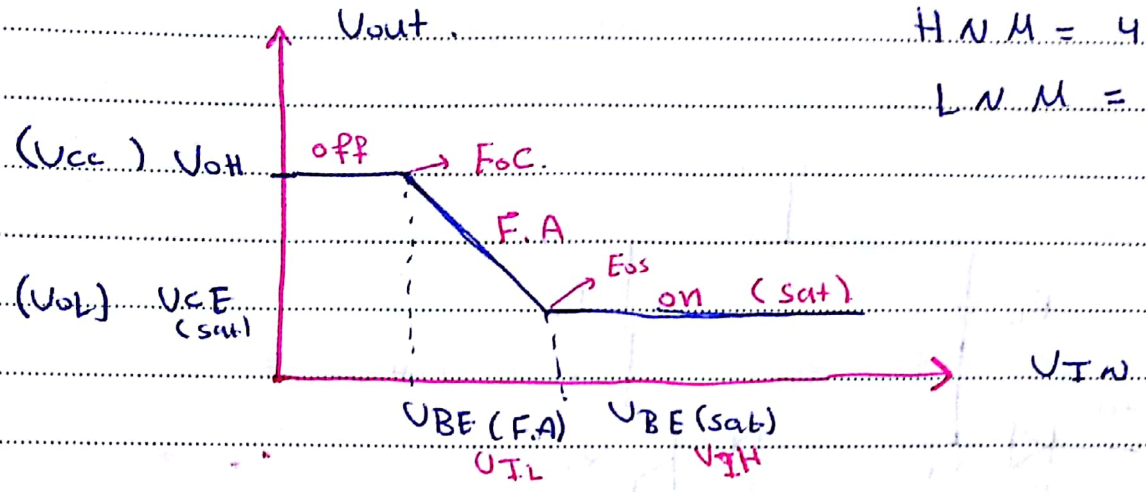
* VTC :-



HNM = 4.2

LNM = 0.5

* V_{IL} ⇒ Q_o turns on when

$$V_x = V_{DL}(on) + V_{BE}(F.A)$$

$$V_{IN} + V_{BE}(on) = V_{DL}(on) + V_{BE}(F.A)$$

$$\therefore V_{IN_L} = V_{BE}(F.A)$$

* Q_o saturates when

$$V_{IH} = V_{BE}(sat)$$

$$V_{OL} = V_{CE}(sat)$$

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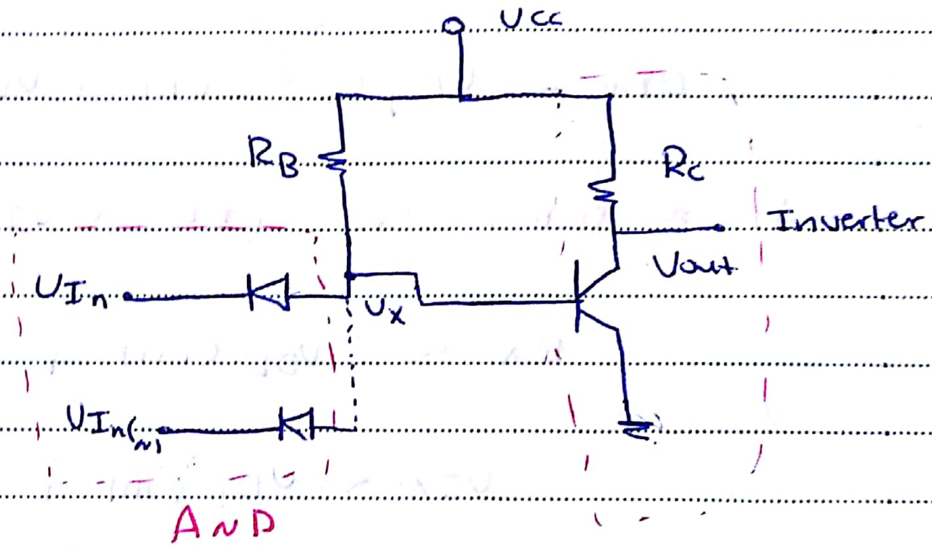
* $V_{IN} > V_x \rightarrow$ DI is off.

R_B must be small for Q_o to saturate.

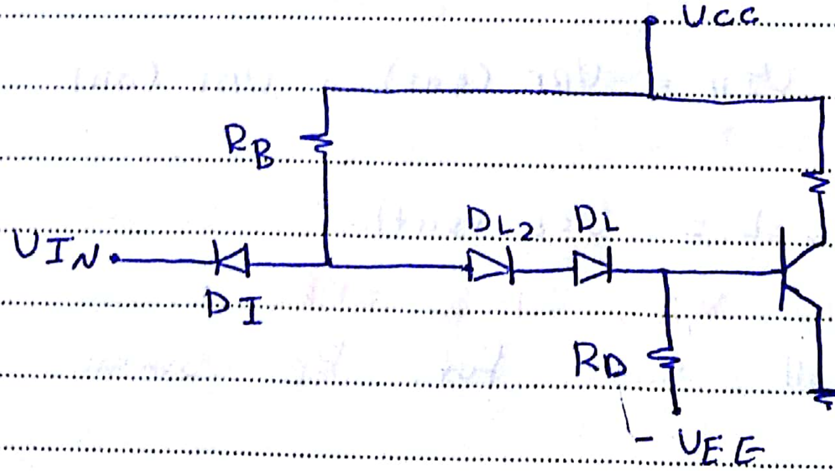
* NAND gate.

I_{N1}	I_{N2}	out
0	0	1
0	1	1
1	0	1
1	1	0



* 6.2 Modified DTL

Additional Level - shifting (LNM



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* R_D, V_{EE} : discharge path of Q_o when it turns from sat

- V_{EE} can be replaced with Gnd (R_D decrease)
لـ المحافظة على تيار سالب ده عيزين.

D_{L2} to improve LNM.

$-V_{IN} - V_{D_I} + 2V_{DL} + V_{BE} = 0.$

1) * V_{oH} Q_o off ($V_{IN} < V_X$, D_I on)

$V_X < 2V_{DL}(on) + V_{BE}(F.A).$

$V_{IN} < V_{DL}(on) + V_{BE}(F.A).$

$V_{oH} = V_{cc}.$

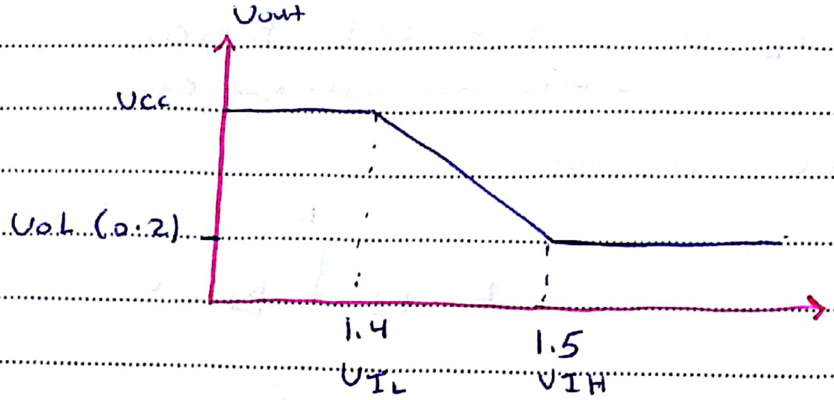
- EoC ⇒ $V_{IL} = V_{BE}(F.A) + V_{DL}(on).$

- EoS ⇒ $V_{IH} = V_{BE}(sat) + V_{DL}(on).$

$V_{oL} = V_{CE}(sat).$

2) $V_{IN} > V_X$, D_I off

Q_o still sats for R_B small.



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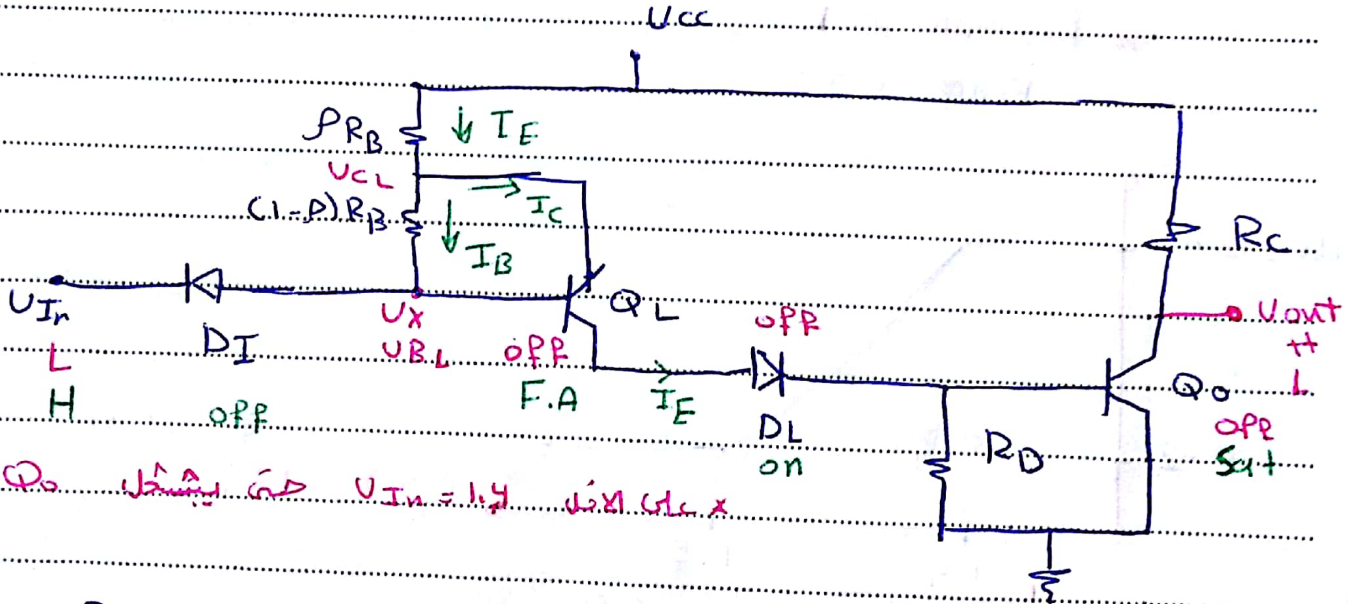
الارقام اعتماداً على قيم الدائرة
عكس تغيير

* VHNM = 3.5 , VLNM = 1.2 V → better than VLNM in Basic DTL.

* 6.3 Transistor Modified DTL.



Q_L , Q_o بيشتغل لما $V_{In} = 1.4$ على الأقل *

* R_D and the ground → discharge part.

* $\rho < 1$, $\rho R_B + (1-\rho) R_B = R_B$

$$N = \frac{I_o}{I_I'}$$

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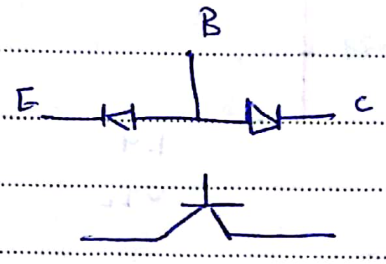
* $\beta = 1$, $(1-\beta) R_B = 0$ (short cct B , C).

لم حنزء علوي للتغني تأثيره .

Q_L acts like a diode.



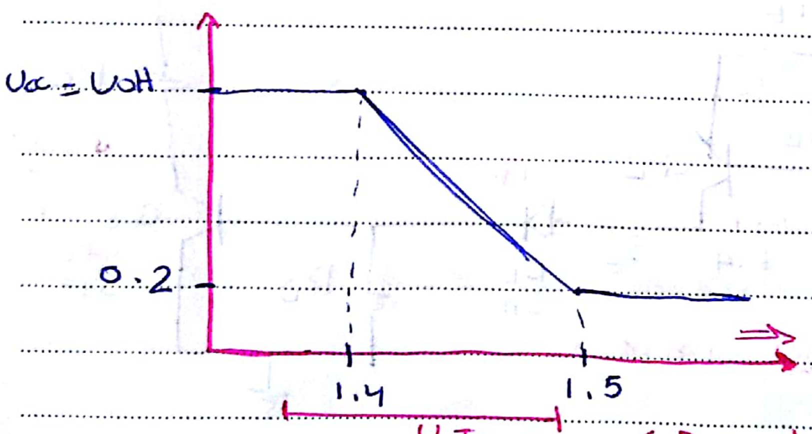
* Input high , $V_C > V_B$.

V_{BC} - ve → Q_L F.A.

$- V_{IL_1} - V_{DI}(on) + V_{BE}(F.A) + V_{DC}(on) + V_{BE,0} = 0$

* Example 6.1

Find VTC.



$V_{OH} = V_{CC} = 5$, $V_{OL} = 0.2$.

$V_{IL} = 2 V_{BE}$ (F.A) = 1.4.

$V_{IH} = V_{BE,L}$ (F.A) + $V_{BE,}$ (sat)

= 1.5

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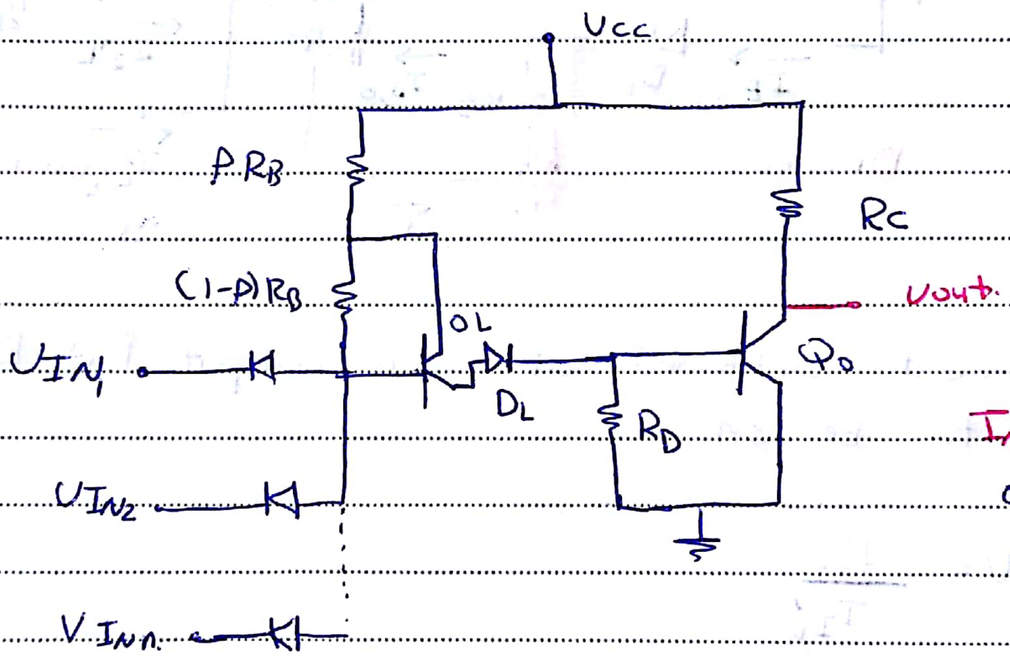
* $V_{IN} < V_x$:- DI on VTC.

$V_{IN} > V_x$:- DI off Power, Fan-out.

6.4 NAND Gate.



In1	In2	out
0	0	1
0	1	1
1	0	1
1	1	0

* Any input $< 2V_{BE}$ (F.A), Qo off. (at Least DI on).

$V_{out} = V_{OH} = V_{cc}$ = Logic H.

* All input high, all DI's off
Q_o sat $\Rightarrow V_{out} = V_{OL} = V_{CE}$ (sat)
= Logic Low.

$V_{IN} \geq V_{BE_L}$ (F.A) $+ V_{BE,o}$ (sat).

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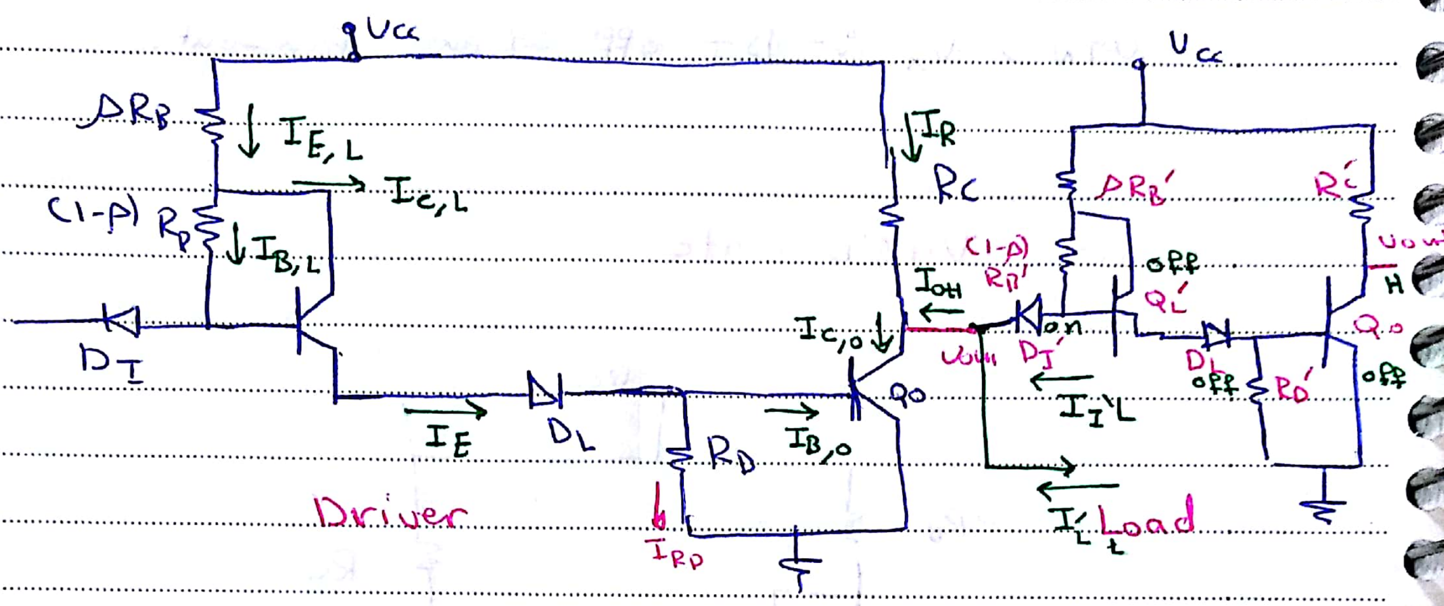
* 6.5 DTL Fan - out .



* Fan -out obtained at Low output for D_I' to be on.

$$N = \frac{I_{OL}}{I_{IL}'}$$

$$I_{IL}' = \frac{U_{cc}' - U_{ID}'(on) - U_{C,E,o}(sat)}{R_B} \quad \text{---- (1)}$$

→ all R_B , I_{IL} Small, N high

$= I(\rho R_\beta)$ off → for power dissipation

$I_{OL} = I_{c,o} - I_{Rc}$

$$= \frac{V_{cc} - U_{C,E,o}(sat)}{R_c} = I_{Rc,(OL)} \quad \text{---- (2)}$$

$$I_{C,o} = \alpha \beta_F I_{Bo}. \qquad (\alpha = 1).$$

$$I_{B,o} = I_{E,L} - I_{RD}.$$

$$I_{RD} = \frac{U_{BE}(sat)}{R_D}$$

$$-U_{CC} + I_E \, \rho R_B + I_{B,L} (1-\rho) R_B + U_{BE,L} (F.A) + U_{D_L}(on) + U_{BE,o}(sat) = 0.$$

$$I_{B,L} = \frac{I_{E,L}}{\beta_F + 1}.$$

* $$I_{\rho R_B}(oH) = I_E = \frac{U_{CC} - U_{BE,L}(F.A) - U_{D,L}(on) - U_{BE}(sat)}{\rho R_B + \frac{(1-\rho) R_B}{\beta + 1}} \quad (3)$$

$\frac{(1-\rho) R_B}{\beta+1}$ → igonre

* Less than R_B (→ ρR_B)

* زيادة I_E

I_E high ⇒ I_{OL} ⇒ high . N ↑ ← I_{OH} يزداد

* Read Example 6.2 ⇒ $N = 54$.

* 6.6 Power Dissipation.

$$P_{CC}(avg) = \frac{I_{CC}(oH) + I_{CC}(oL)}{2} U_{CC}.$$

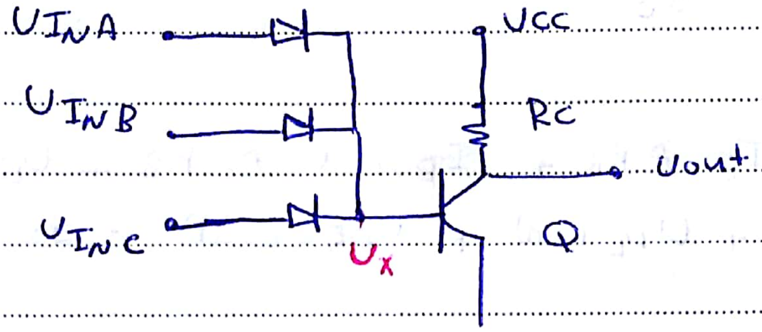
$$I_{CC}(oH) = I_{RC}(oH) + I_{\rho R_B}(oH) = I_{\rho R_B}(oH) \; \ldots$$

from eqn (1)

* $I_{CC}(OL) = I_{R_C}(OL) + I_{PRB}(OL)$

eq (2) eq (3)

- DTL NOR gate.



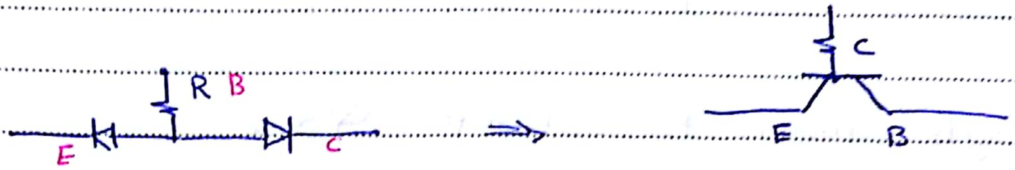
$V_{out} = V_{CE}(sat) \Leftarrow$ Q sat. $\Leftarrow$ high واحد Input *

Q off $\Leftarrow$ Low كل Input *

V_{out} = high

Subject: 5.1 / /

* Chapter 7 Transistor Logic (TTL).

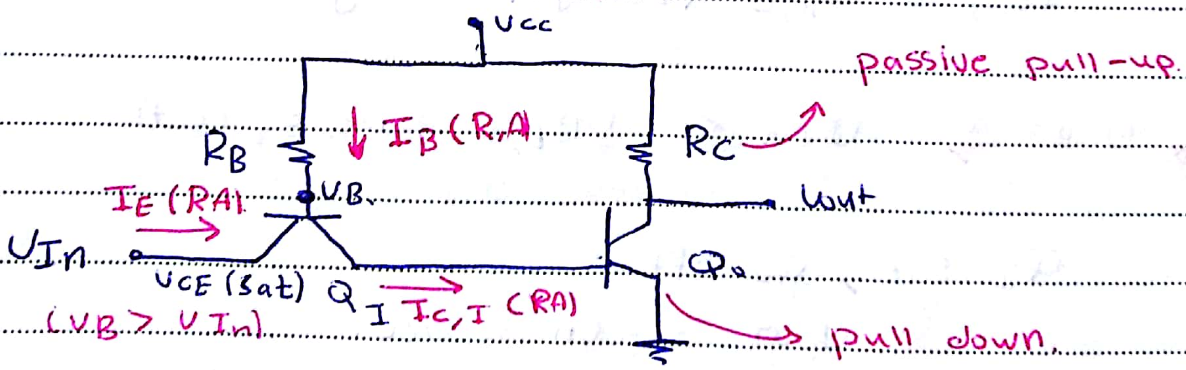


- Main different between TTL and DTL that DI and DL in DTL are replaced.

- TTL in general uses an active pul cct (higher fan-out).
- TTL faster than DTL.

* The most common families in TTL, 7400 series. (0 → 70 c°).
5700 series (-55 → 125 c°)

- 7.1 Basic TTL Inverter.



- At Low input VBE (+ve)
QI ⇒ provides Qo with current also if input is Low QI is a discharge path for Qo.

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$I_{B,I} = \frac{V_{CC} - V_{BE,I(sat)} - V_{CE(sat)}}{R_B}$ (VIN)

— $I_{B,I}$ high enough to saturate Q_I.

— $V_{In} - V_{CE(sat)} + V_{BE}(?) = 0$.

$V_{BE} = V_{In} + V_{CE(sat)}$.

Q_o off I_C = zero V_{out} = high.

* Q_I opereats in an unconventional way: when input is Low, I_B enters, Q_I and generates I_E, This for collector current into current.

$I_{C,I} = I_{B,o}$ (Leakge) very Small.

* $V_{OH} \Rightarrow$ $V_{In} < V_{BE,o} - V_{C,E_I(sat)}$.

Q_I Sat, Q_o off.

$V_{out} = V_{OH} = V_{CC}$.

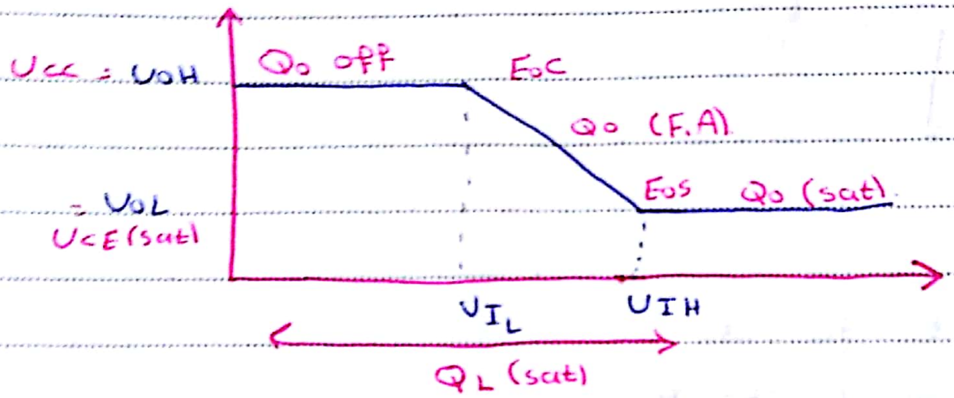
* $V_{IL} \Rightarrow$ $-V_{CE,I(sat)} + V_{BE,o}$ (F.A)

Q_o F.o.c, Q_I Sat.

③ $V_{IH} = -V_{CE}(sat) + V_{BE,o}(sat)$.

Q_o EOS , Q_I sat.

④ $V_{OL} = V_{CE}(sat)$.



If input increases beyond V_{IH}, at some point (Logic high)

$V_{IN} = V_{E,I} > V_{B,I}$

V_{BE}, -ve (B-E) J is reverse biased

$V_{BC,I} = V_{CC} - I_{B,I} R_B - V_{BE,o}(sat)$.

$\Rightarrow V_{BC}$ +ve $\Rightarrow Q_I$ operates in the RA mode.

$I_E = \beta_R I_{B,I}$ — β_R very small.

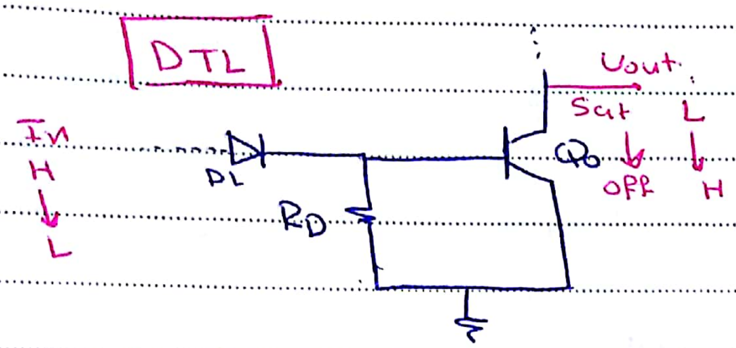
* عكس اتجاه تيار معناها سالب .

$I_{C,I} = (1+\beta_R) I_{B,I}$.

R.A. $\Leftarrow Q_I$ يعتبر high in power * لما يدي أعلى

* 7.2 Comparison of Stored-charge Removal. (between DTL and TTL).

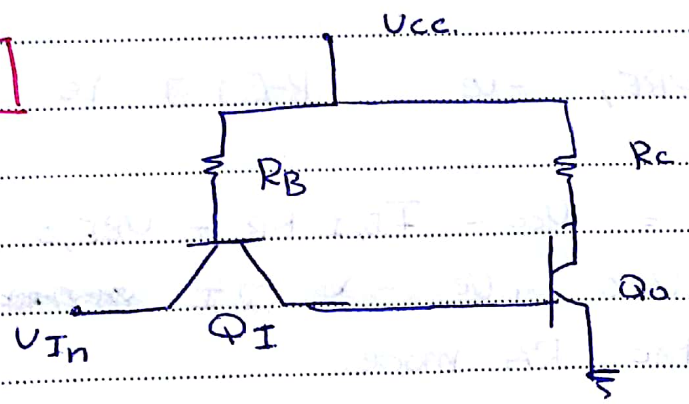
DTL



- Q o went from Sat to off
- output went from L to H.
- Input " " H to L.

* I_D (charge removal) = $I_{R,D}$, DTL = $\frac{V_{BE}(sat)}{R_D}$.

TTL



$V_{In} = V_{E,I} = V_{CE}(sat)$. (Low)

$V_{B_I} = V_{BE} + V_{CE}(sat)$.

$V_{C,I} = V_{BE,O}(sat)$.

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$V_{BC,I} = V_{BE,I} + V_{CE}(sat) - V_{BE,o}(sat)$

$= 0.2$ max

$= 0.1$ min.

but Less than $V_{B,C}(sat)$.

$\Rightarrow$ Q_I in F.A mode.

$I_{B,o}$ (discharge) $= I_{C,E}$ (F.A).

$I_{C,I} = \beta_F \, I_{B,I} =$ $I_{B o, TTL}$.

$$I_{B,I} = \frac{V_{cc} - V_{BE,I}(F.A) - V_{CE}(sat)}{R_B}$$

($V_{CE}(sat) \rightarrow V_{In}(Low)$)

$$I_{Bo,TTL} = \beta_F \left[\frac{V_{cc} - V_{BE,I}(F.A) - V_{In}(Low)}{R_B} \right]$$

تفريغه أسرع من DTL.

* T_{TTL} charge removal $\gg$ I_{DTL} (ch. removal).

أسرع.

* Example 7.1 :-

Find factor of improvement of stored charge removal (between TTL and DTL).

$R_D = 5K$ for DTL

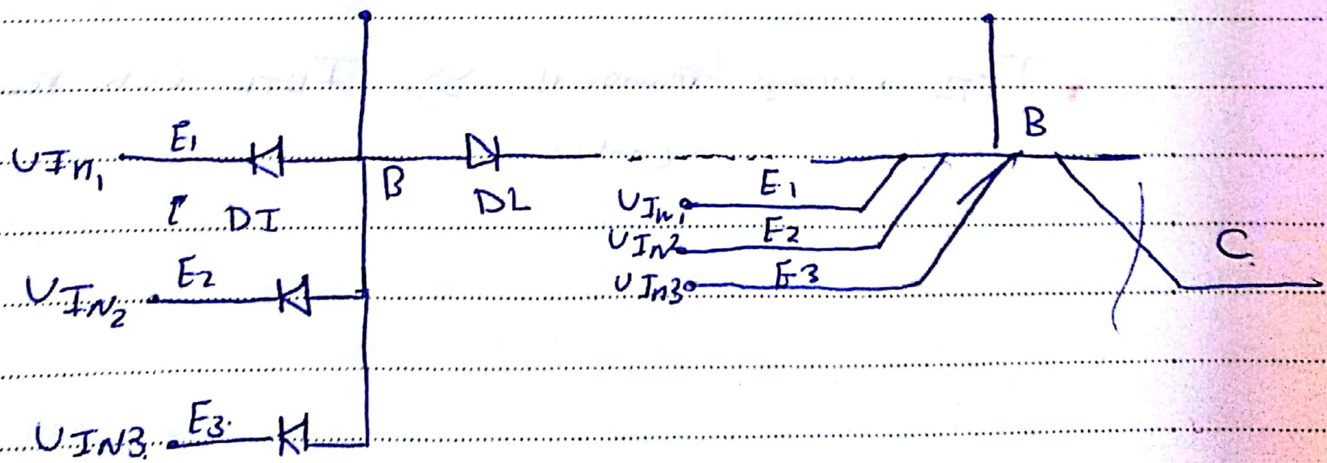
$R_B = 2K$ for TTL.

$$I_{RD} = \frac{V_{BE0}(sat)}{R_D} = \frac{0.8}{5K} = 160 \mu A.$$

$$I_{B,0} = 50 \left[\frac{5 - 0.2 - 0.7}{2K} \right] = 102.5 m.$$

$$\text{Factor of improvement} = \frac{102.5 m}{160 \mu} = 640.6.$$

– 7.3 Basic TTL NAND Gate and the multi-emitter BJT.



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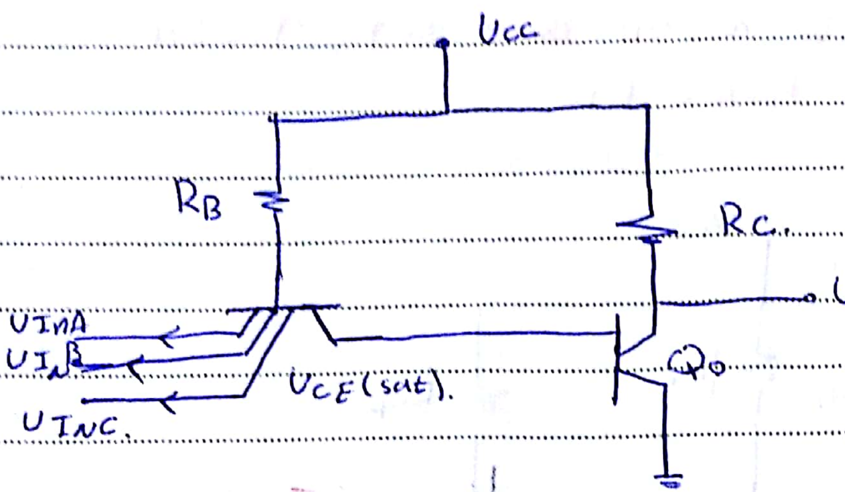
NAND Gate.



* Any input Low :-

$V_{IN} < V_{BE,0}\ (F.A) - V_{CE,I}\ (sat).$

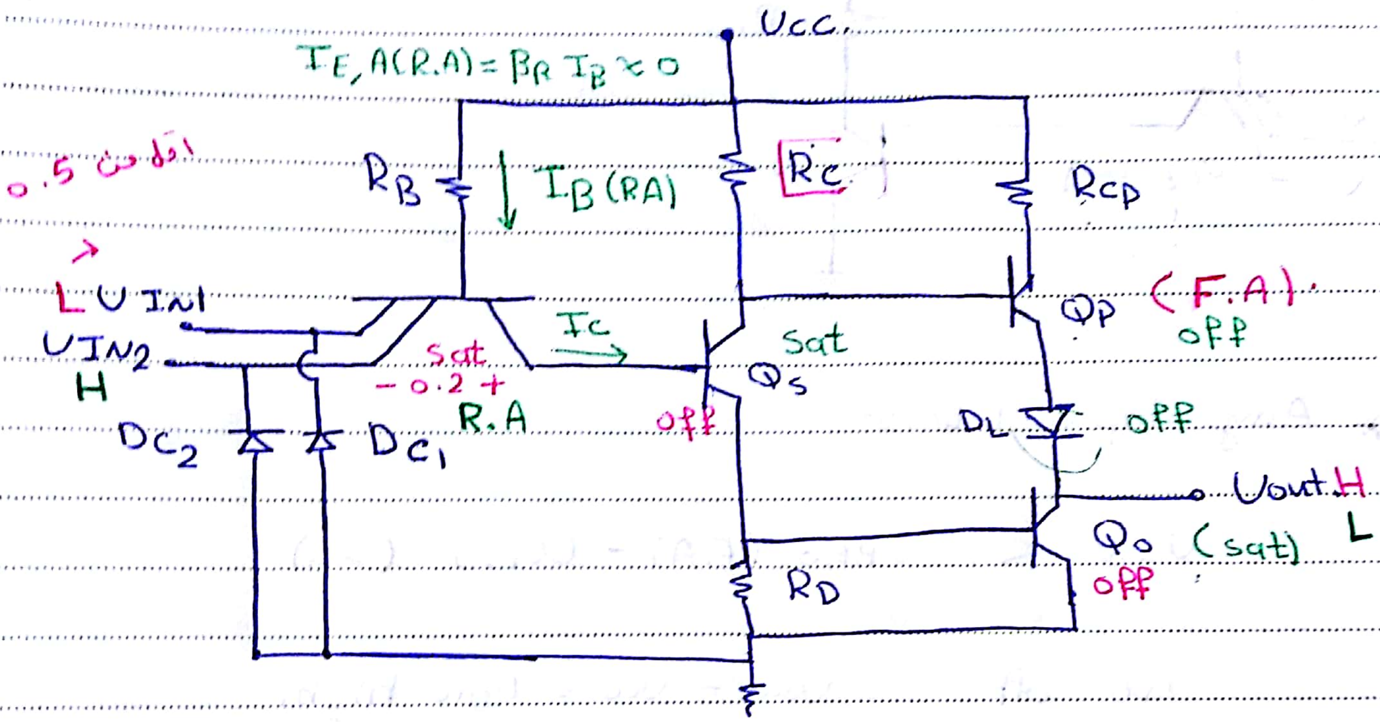
Q0 off   Vout = Vcc = Logic high.
QI sat.

* All input high :-

$V_{BE,I}$ -ve ⟹ QI in R.A mode.
Q0 Saturate.
$V_{out} = V_{CE,0}(sat)$ = Logic Low.

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

* 7.4 Standard TTL NAND Gate with TOTEM pole (pull-up, pull down cct).



- Qp ⇒ active pull up, more current provided at output.
- Qo ⇒ discharge path.
- R_D ⇒ " path.
- Q_s ⇒ Drive splitter or Logic inversion. Q_s also feeds Q_o.

- Q_I ⇒ when input Low acts as discharge path, also provide Q_s and Q_o with current.

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* when Input is Low

$V_{IN} < V_{BE,S}$ (F.A) $- V_{CE,I}$ (sat).

Q_s, Q_o off

$I_{B,P}$ is enough run Q_P and DL but

$R_c > R_{cp} \Rightarrow V_{Rc} > V_{Rcp}$

$V_{B,P} < V_{C,P} \Rightarrow V_{B,C,P}$ -ve.

$\Rightarrow Q_P$ in F.A.

$- V_{IN} + V_{CE,I}$ (sat) $+ V_{B,S} = 0$.

$V_{In} = V_{B,S} - V_{CE,I}$ (sat).

$Q_s \Rightarrow$ on $\Rightarrow V_{B,S} = 0.7$.

* when input is high :-

Q_I, R.A modes.

Q_s, Q_o Sat.

$V_{B,P} = V_{BE,S}$ (sat) $+ V_{BE,O}$ (sat) $=$ 1 Volt.

not enough to run DL an Q_P.

note * $Q_P \rightarrow$ on   if

$V_{B,P} = 1.6$.

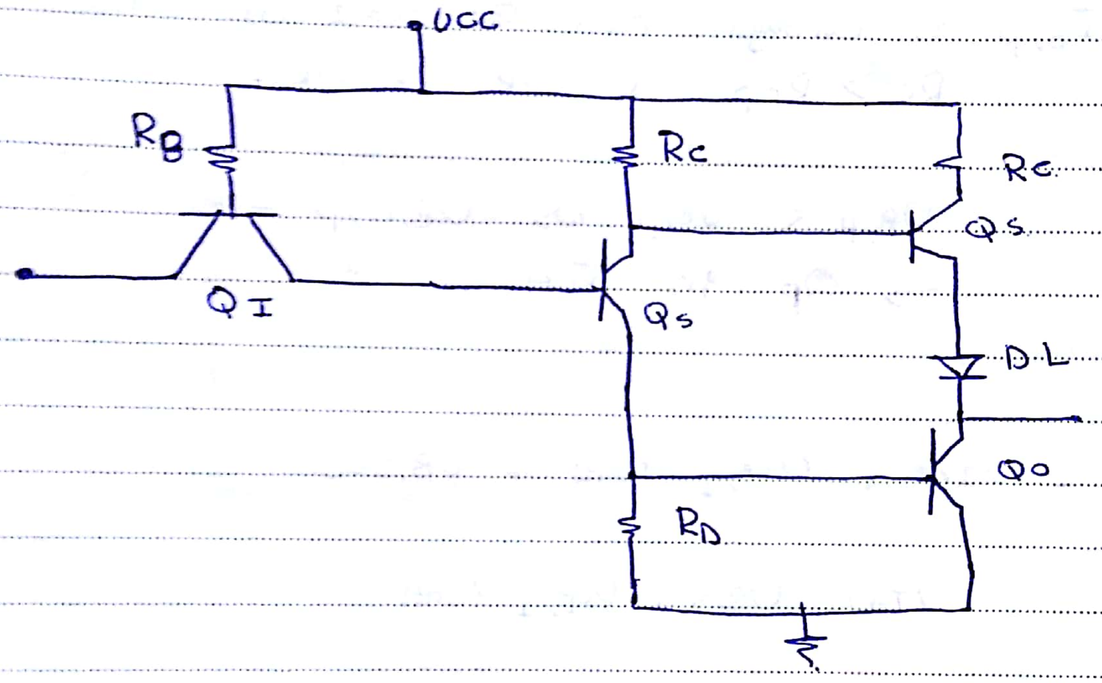
Subject: 60

4 / 3 / 2018.

UTC ⇒ QI sat.

Power disipation ⇒ QI R.A.

* 7.5 Standard TTL UTC.



* at Low input Input < 2 UBE − UCE (sat).

$$I_{RB} = \frac{U_{CC} - U_{BE,I}(sat) - U_{I,N}(Low)}{R_B}$$

Large enough to saturate QI.

Qs, Qo off.

$I_{C,I}(sat) = I_{B,o}$ (leakage).

Qp in F.A mode, DL on

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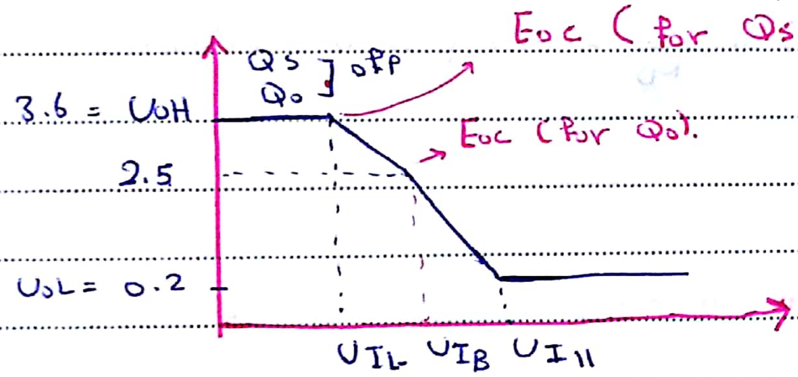
Ignore $I_{B,P}$ (F.A) = I_{RC}.

$V_{out} = V_{CC} - V_{BE,P}(F.A) - V_{DL}(on)$.

$V_{OH} = 3.6\ V$.

- V_{IL} → input at which Q_S turns to F.A mode,

$V_{In} = V_{BE,S}(F.A) - V_{CE}(sat) = 0.5$.



- As input increases, Q_S draws more current.

$V_{out} = V_{CC} - I_{RC} R_C - V_{BE,P}(FA) - V_{DL}(on)$ → dec.

(I_{RC} increases)

- V_{IB} → input Break point :- Eoc for Q_o

$V_{IB} = 2 V_{BE}(F.A) - V_{CE}(sat) = 1.2$.

at which Q_o turns to F.A mode.

when Q_o & Q_S are both on current through R_C increase even more.

V_{out} drops faster → VTC curve is steeper.

S T A R S Notebook

* V_{OB} ⇒ output Break point.

$V_{OB} = V_{CC} - I_{RC} R_C - V_{BE,P} - V_{DL(on)}$.
ignore $I_{B,P}$ (F.A), $I_{B,S}$ (F.A).

$I_{B,O}$ (E.o.c), also ingore.

$$I_{RC} \approx I_{C,S} \approx I_{E,S} \approx I_{RD} = \frac{V_{BE,O}\ (F.A)}{R_D}$$

$$V_{OB} = V_{CC} - V_{BE,O}\ (F.A)\ \frac{R_C}{R_D} - V_{BE,P}\ (F.A) - V_{DL}\ (on).$$

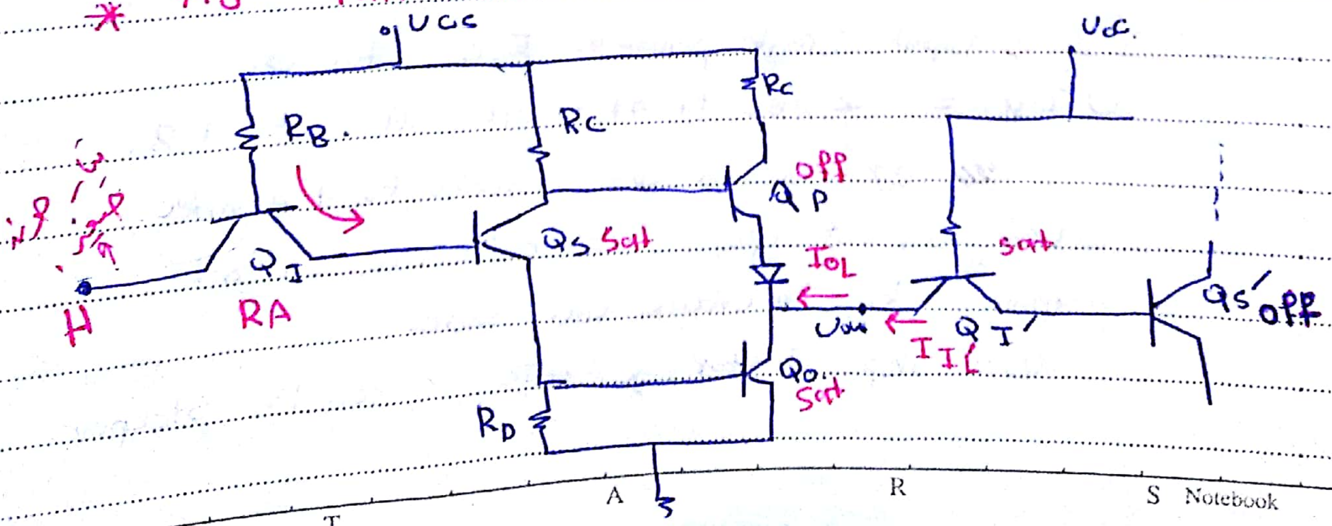
≈ 2.5.

* V_{IH} :- Q_S, Q_O saturate.

$V_{IH} = 2\, V_{BE}(sat) - V_{CE,I}(sat) = 1.4$.

$V_{OL} = V_{CE,O}(sat) = 0.2$

* 7.6 Fan - out



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Fan-out analysis performed at Driver output Low, for Q_I' to operate in sat mode.

If Q_I' opreate in R.A (high input at Load)

$$I_{In}' = I_{E,I} \quad (R.A).$$

$$N = \frac{I_{OL}}{I_{IL}'}$$

$$I_{IL}' = I_{RB}' = \frac{V_{CC} - V_{BE(sat)} - V_{CE,I(sat)}}{R_B}.$$

$$I_{OL} = I_{C,O} = \sigma \beta_F \, I_{B,O}.$$

$$I_{B,O} = I_{E,S} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,O(sat)}}{R_D}$$

$$I_{E,S} = I_{B,S} + I_{C,S}.$$

$$I_{C,S} = I_{RC} = \frac{V_{CC} - V_{CE,S(sat)} - V_{BE,O(sat)}}{R_C}.$$

$$I_{B,S} = I_{C,I} = (1 + \beta_R) \, I_{B,I}$$

$$I_{RB} = I_{B,I} = \frac{V_{CC} - V_{BC,I(R.A)} - 2V_{BE(sat)}}{R_B}.$$

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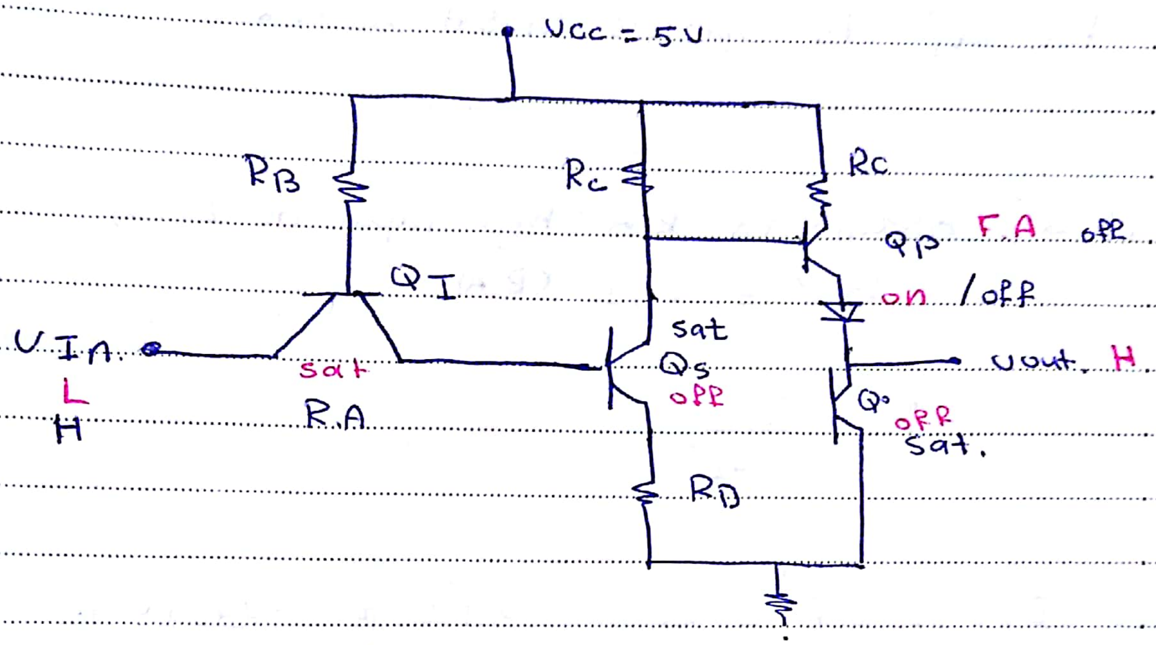
7.7 TTL power Dissipation :-



- I_{cc} (oH) :- (with no Load).

$$I_{RB}(oH) = \frac{V_{cc} - V_{BE,I}(sat) - V_{In}(Low)}{R_B}$$

$V_{CE}(sat)$ OR V_{In} (Low).

$I_{Rc}(oH) = I_{Bp}(F.A) = \approx 0.$

$I_{Rcp}(oH) = 0.$

- with Load $I_{Ep} = I_{E',I}$ (R.A). (v.samll).

* I_{cc} (oL) :-

$$I_{RB}(oL) = \frac{V_{cc} - V_{BC,I}(R.A) - 2V_{BE}(sat)}{R_B}$$

$$I_{Rc}(oL) = \frac{V_{CC} - V_{CE_3}(sat) - V_{BE_{1,2}}(sat)}{R_c}$$

$I_{Rcp} = 0.$

$$P_{cc}(avg) = \frac{I_{cc}(oH) + I_{cc}(oL)}{2} * V_{cc}$$

* Example 7.4. , $P_{cc}(avg) = 10.4$ mw.

– 7.9 Low power TTL (LTTL).

higher values of Resistors.
Lower values of current.
Lower values of power.
Fan-out decreases. (dis advantages)

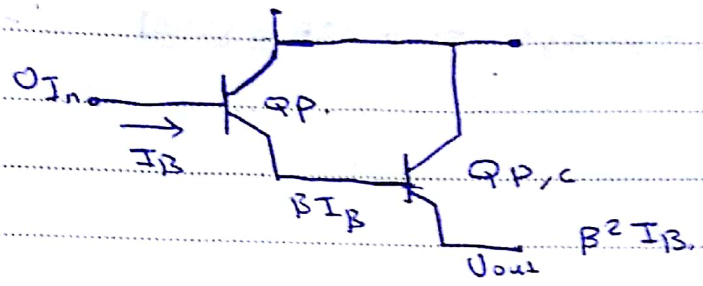
$\tau = Rc\uparrow$ (Time delay), speed ↓ (dis).
. design مسؤول عنه *

* Example 7.5, P = 919 μw.

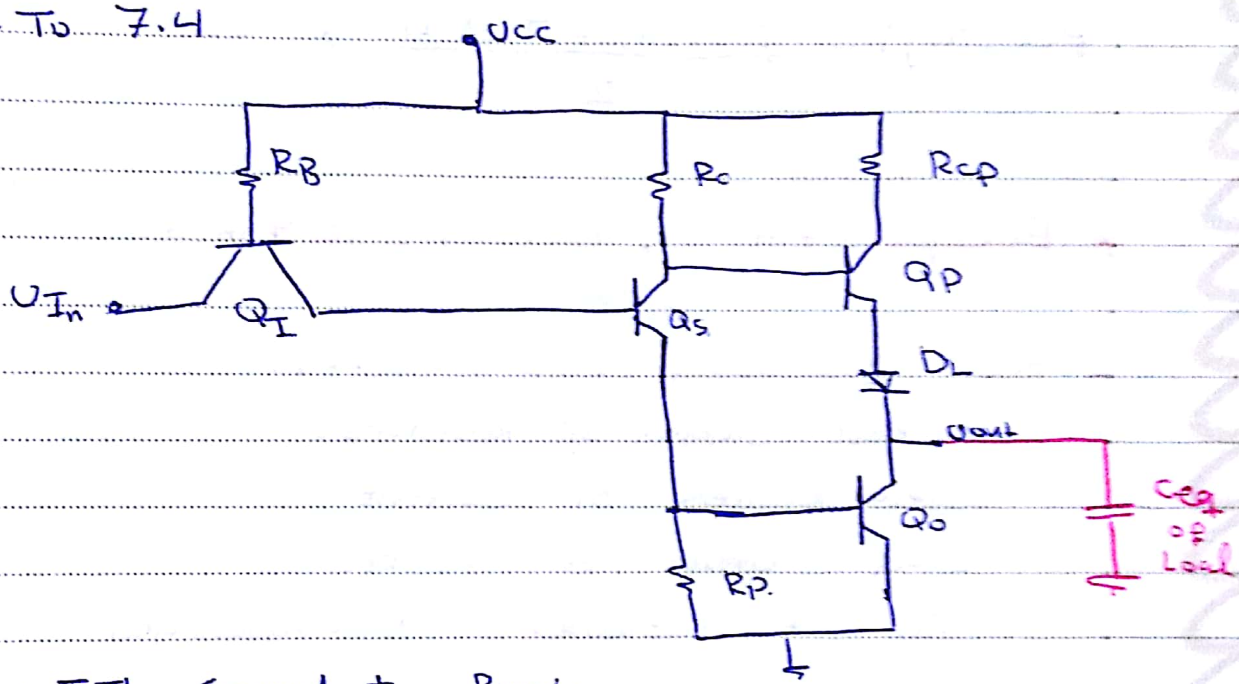
– 7.10 High speed TTL.

Less Resistance values.
higher Speed $\tau = Rc\downarrow$.
current ↑, Fan-out ↑, ✓.
power ↑ X.

Qp and DL are replaced with a Darlington pair



- Back To 7.4



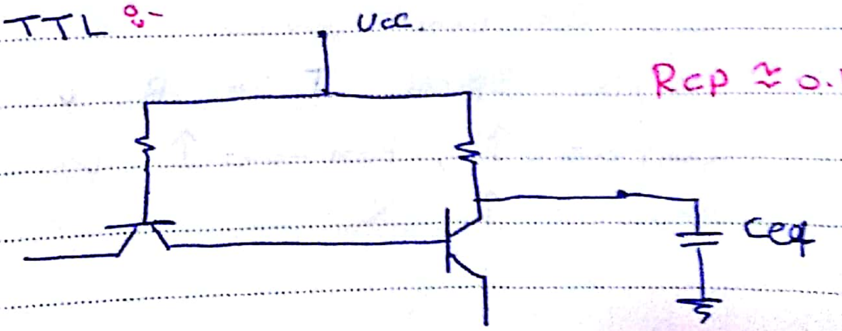
* Compare TTL Speed to Basic TTL speed.

$\tau = R_{cp} C_{eq}$.

$$I_{R_{cp}} = \frac{V_{cc} - V_{CE,P} - V_{DL(on)} - V_{CE(sat)}}{R_{cp}}$$

- Basic TTL :-

$R_{cp} \simeq 0.1 R_c$.



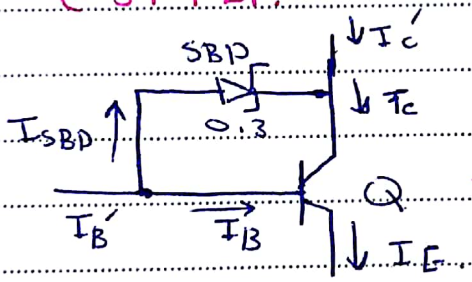
Scanned by CamScanner

$I_{Basic} = R_c$ ceq.

$I_{Rc} = \dfrac{V_{cc} - V_{CE(sat)}}{R_c}$.

$I_{Basic} > I_{TTL}$
$I_{Rc} < I_{RcP}$ } ⇒ TTL much Fast.

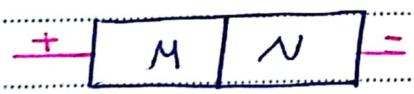
* Chapter 8 Schottky Transistor Transistor Logic (STTL).



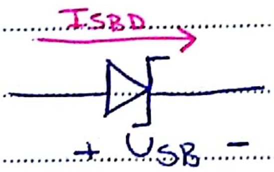
Sat بيمنع يدخل ×

⇒ QSBD.

- Schottky Diode (SBD):-



, P is replaced with metal (M).



$V_{SB}(on) = 0.3$.

* when Q Saturates, $V_{BC} = V_{BC(sat)}$.
If an SBD is connected between base and collector it will divert the input current and it will turn on to clamp V_{BC} at $V_{SBD}(on) = 0.3$

*


QSBD.

* regular Q saturates at V_{BC} (sat) = 0.5 V.
if SBD is connectd between Base and collector.
and current is applied SBD will turn on and
direct current from Q, preventing Q , form
Saturation $V_{BC} = V_{SBD} < V_{BC}$ (sat)

* operation modes :-

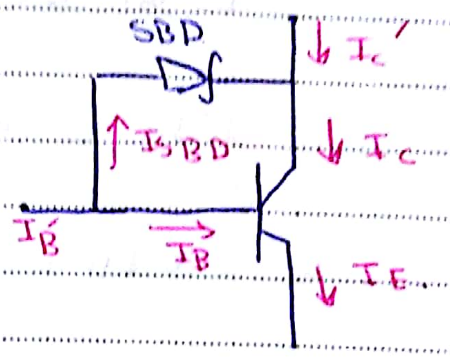
1. V_{BC} -ve , V_{BE} -ve.
QSBD off and current Zero (SBD off
, Q off).

2. FA mode.
V_{BE} +ve , V_{BC} -ve , QSBD in F.A mode
SBD off, Q F.A, V_{BE} (F.A) = 0.7, $I_C = \beta I_B$.
$I_E = I_B + I_C$.

3. Hard mode.
V_{BC} +ve , V_{BE} +ve.
SBD on , Q on.
V_{BC} (hard) = V_{SBD} = 0.3.
V_{BE} (sat) = 0.5 = V_{BE} (hard) − V_{SBD}

* $I_c = \beta I_B$

$I_{SBD} = I_c - I_c' = \beta I_B - I_c'$



4- Reverse Schottky (Rs).

V_{BC} +ve , SBD on.

$V_{BC} = V_{SBD} < V_{BC}(R.A)$.

(B-C) J ⟹ open.

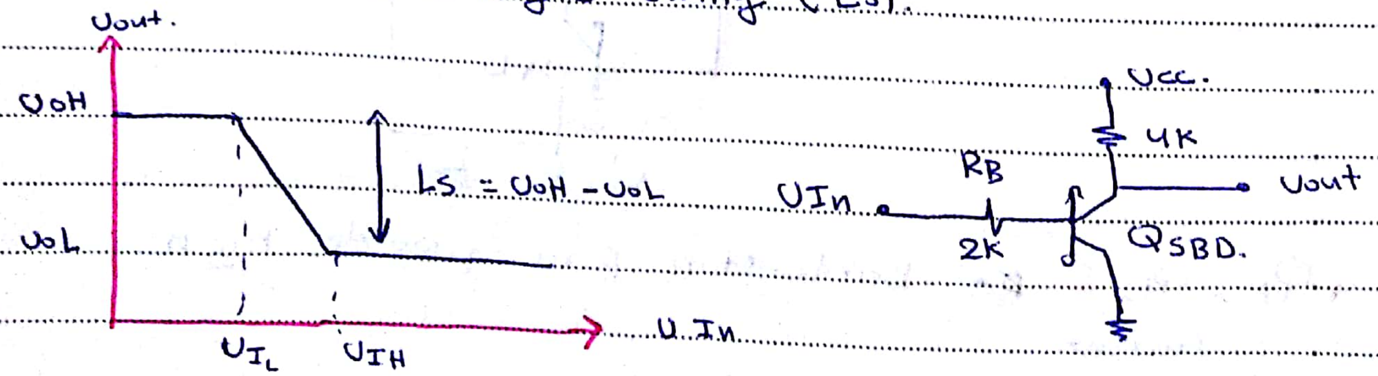
V_{BE} -ve , (B-E) junction open.

$I_B' = I_{SBD} = -I_c'$ (بس اتجاهه بالعكس).

$V_{BC}(Rs) = V_{SBD}$.

* Example 8.1

Find the Logic swing (Ls).



Subject: 7o

$V_{OH} = V_{CC} = 5.$

$V_{OL} = V_{CE}\,(\text{hard}) = 0.5.$

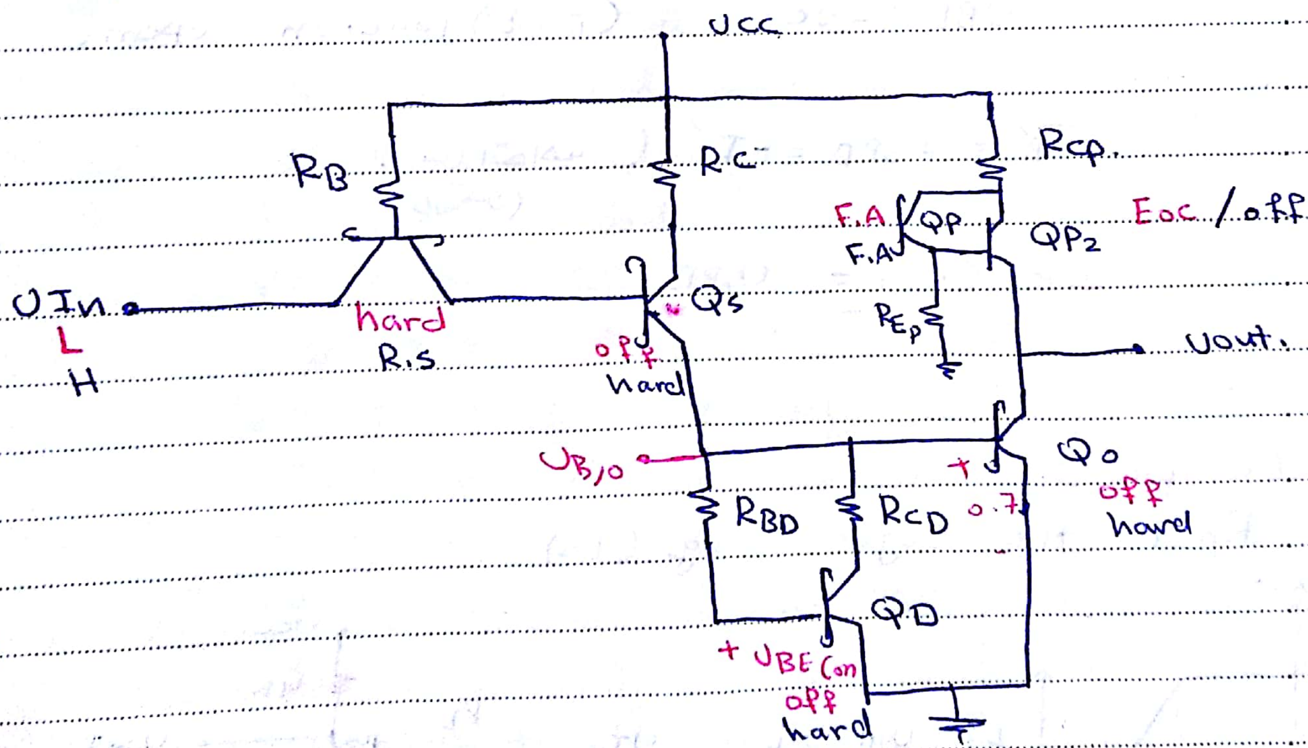
$L_S = 5 - 0.5 = 4.5.$

$V_{IL} = V_{BE}\,(F.A) = 0.7.$

$V_{IH} = I_B R_B + V_{BE}\,(\text{hard}).$

$$I_B = \frac{I_C}{\beta}$$

* 8.3 Schottky - Clamped TTL (STTL).



+ QP, QP2 :- Darlington pair provide high current.

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/ /

* R_{BD} / R_{CD} are Designed such that Q_o and Q_D turn on simultaneously also, Q_o, R_{BD}, R_D are conduction path for Q_S to ground. if Q_D is off, Q_S will be off too.
  Q_S will run only when Q_o, Q_D are on.

⇒ no Break point and transition width is narrower than in regular TTL.

- Q_D, R_{BD}, R_{CD} discharge path for Q_o.
  ⇒ high speed.
  STTL $\tau = 2ns$.
  regular TTL, $\tau = 10ns$.

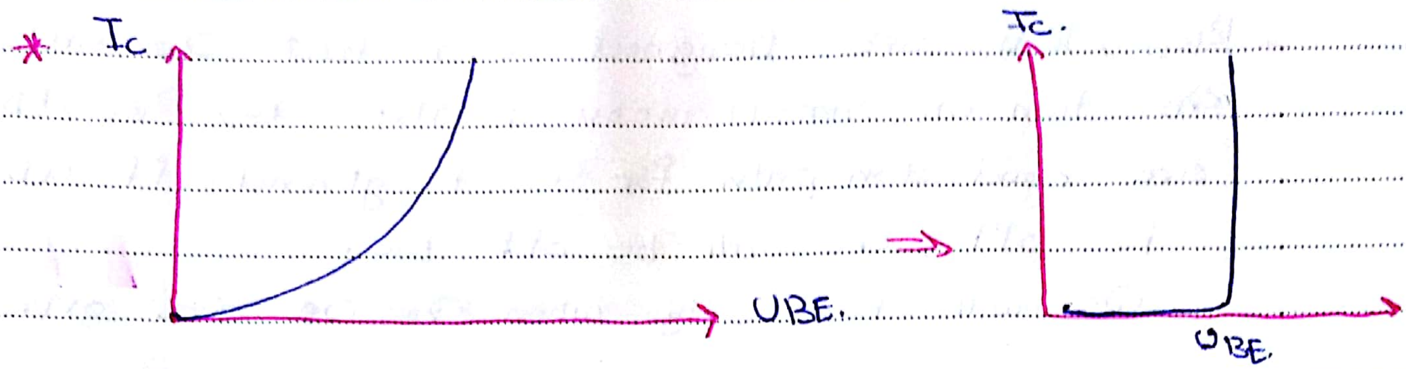
Q_{P_2} ⇒ $+ U_{CE,P} + U_{BE,P_2} - U_{CE,P_2} = 0$.

$U_{CE,P_2} = U_{CE,P} + U_{BE,P_2} > U_{CE(sat)}$.

does not saturate ⇒ no need for Q_{SBD}.

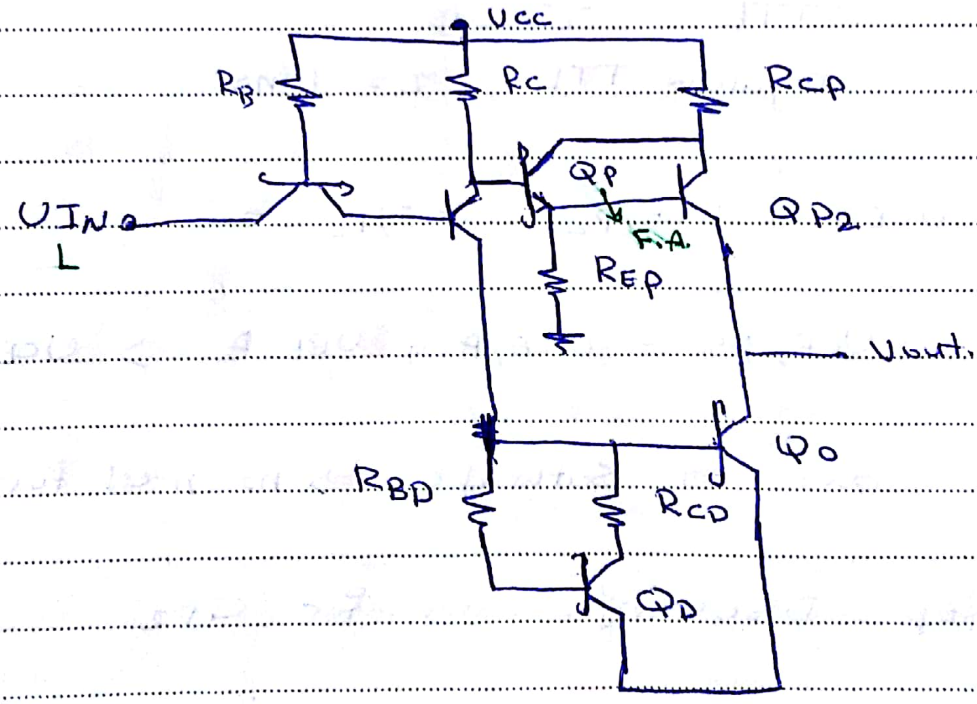
R_{EP} : Discharge path for Q_{P_2}.

* $R_{BD} > R_{CD}$, I_{BD} ignored when Q_o is on.



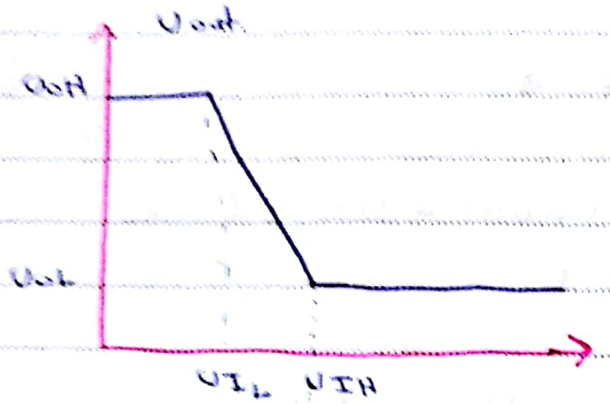
* QD does not follow piece wise analysis.
  ⇒ on when Qo on.

* Example 8.2 (STTL UTC)



$V_{out} = V_{cc} - I_{Rc} R_c - V_{BE} - V_{BE}$.

Subject: 7.3 13 / 3 / 2018.



– Input Low. Qs, Qo off.

* V_{OH} ⇒ $V_{IN} < 2V_{BE}(F.A) - V_{CE}(hard)$.
Qo, Qs off , Qp, Qp2 F.A.

$I_{Rc} = I_{Bp}(F.A) \approx 0$.

$V_{OH} = V_{CC} - 2V_{B}(F.A) = 3.6$.

$V_{Rc} > V_{Rcp}$ ⇒ $V_{Bc,p} - V_e$, Qp F.A

Qp2 also F.A.

* Input high. QS, Qo Hard $V_{Bp} = 1.3V$.
enough to turn Qp to F.A, but
Qp2 off.

VIL when Qo, Qs turn F.A
$V_{IL} = 2V_{BE}(F.A) - V_{CE}$ hard
$= 0.9$.

Subject: 7.4

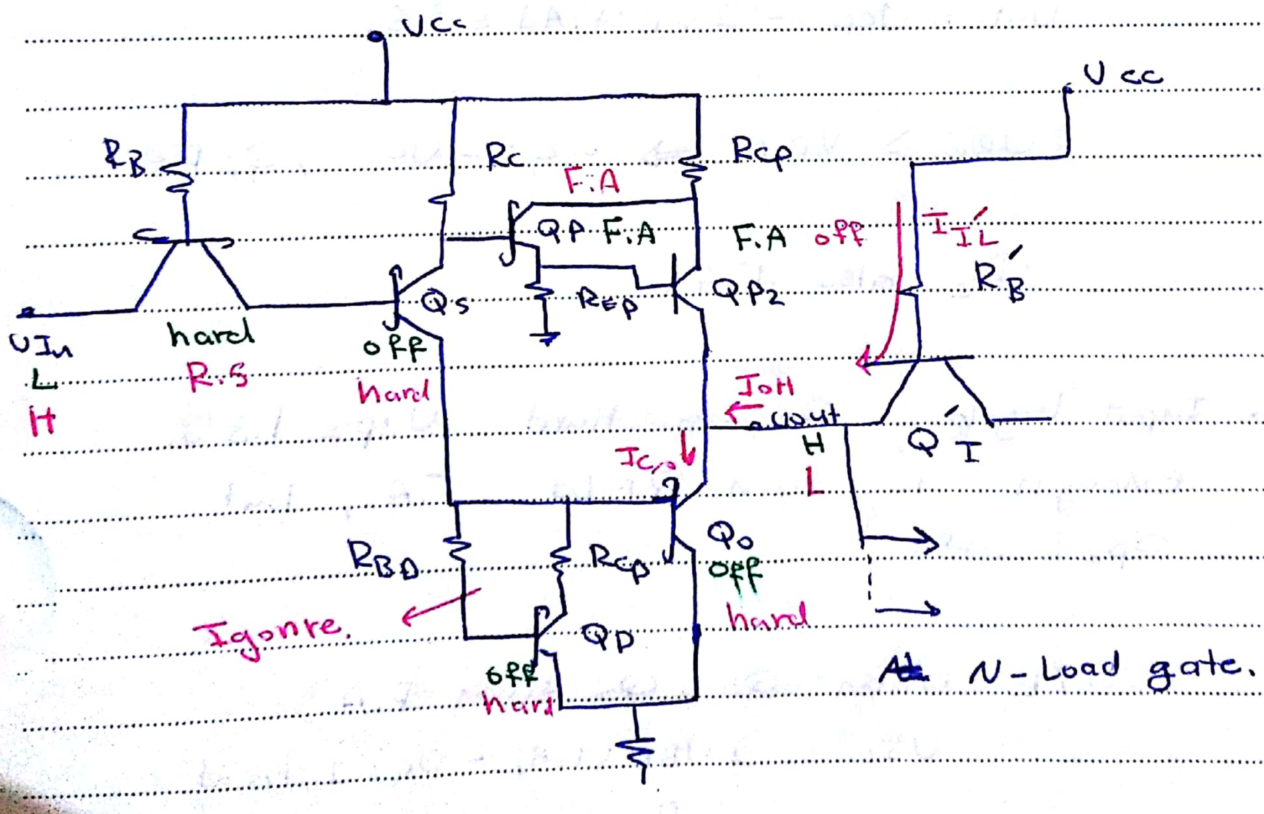
V_{IH} : Q_o, Q_s turn hard.

$V_{IH} = 2V_{BE}(hard) - V_{CE,I}(hard)$
$= 1.1\ V$

* $V_{OL} = V_{CE,o}(hard) = 0.5\ V$.

- $HNM = 3.6 - 1.1 = 2.5$.
- $LNM = 0.9 - 0.5 = 0.4$.

* 8.4 Fan-out.



* are performed when Driver o/p is Low so that Q_I' is hard and current flows.

$$N = \frac{I_{OL}}{I_{IL}'}$$

$$I_{IL}' = \frac{U_{CC}' - U_{BE,I}' (hard) - U_{CE,O} (hard)}{R_B'}$$

$$I_{OL} = I_{CO} = \beta_F I_{BO}$$

$$I_{BO} = I_{ES} - I_{CD}$$

$$I_{CD} = \frac{U_{BE,O} (Hard) - U_{CE,D} (hard)}{R_{CD}}$$

$$I_{ES} = I_{CS} + I_{BS}$$

(igonre $I_{Bp(F.A)}$) $$I_{CS} \approx I_{RC} = \frac{U_{CC} - U_{CE,S} (hard) - U_{BE,O} (hard)}{R_C}$$

$$I_{B,S} = I_{SBD} = I_{RB}$$

$$= \frac{U_{CC} - U_{BC} (R.S) - 2 U_{BE} (hard)}{R_B}$$

$$U_{BC} (R_S) = U_{SBD} = 0.3\ U$$

* Example 8.3 (Fan-out).

$N = 149.2 = 149.$

8.5 * power Dissipation :-

1. $I_{CC}(OH) = I_{RB}(OH) + I_{RC}(OH) + I_{RCP}(OH).$

$$I_{RB}(OH) = \frac{V_{CC} - V_{BE,I}(hard) - V_{In}(Low)}{R_B}$$

$I_{RC}(OH) = I_{BP}(F.A)$ Ignore $\approx 0.$

$$I_{RCP}(OH) = I_{E,P}(OH) = \frac{V_{CC} - V_{BE,P}(F.A)}{R_{EP}}$$

Q_{P2} conidered off (Load or no Load floated) ($I_{E,S}'(R.S) = 0$).

2. $I_{CC}(OL) =$

$$I_{RB}(OL) = \frac{V_{CC} - V_{BC}(R.S) - 2V_{BE}(hard)}{R_B}$$

$$I_{RC}(OL) = \frac{V_{CC} - V_{CE,S}(hard) - V_{BE,O}(hard)}{R_C}$$

$$I_{RCP}(OL) = I_{REP}(OL) = \frac{V_{CE,S}(ward) + V_{BE,O}(ward) - V_{BE,P(F...)}}{R_{EP}}$$

$$I_{CC}(OL) = I_{RCP}(OL) + I_{RC}(OL) + I_{RB}(OL) \; *$$

$$P_{avg} = \frac{I_{CC}(OL) + I_{CC}(OH)}{2} * V_{CC}.$$

- Example 8.4 ⇒ $P_{CC}(avg) = 20.05\ mW$.

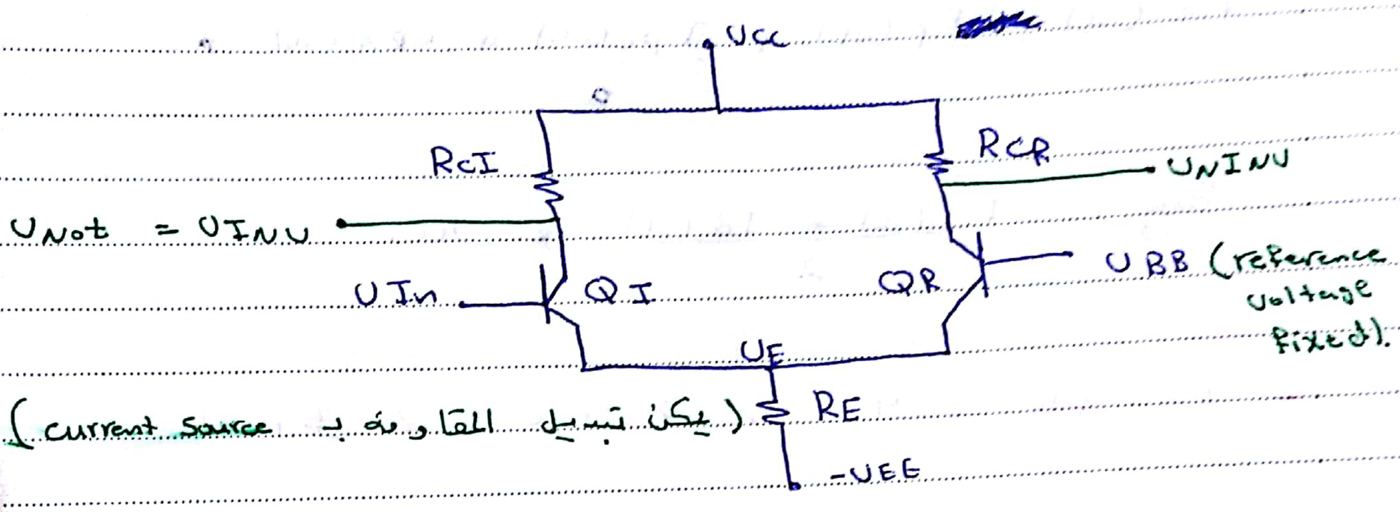
8.6 Low power STTL (LSTTL). مهم جداً

V.T.C, Fan-out, power Dissipation.

*

* Chapter 11 Emitter coupled Logic (ECL)

11.1 BJT current switch.



(يمكن تبديل المقاومة بـ current source)

- $I_{RE} = \frac{U_E + U_{EE}}{R_E}$

- $U_{INV} = U_{cc} - I_{c_I} R_{cI}$

- $U_{NINV} = U_{cc} - I_{cR} R_{cR}$.

- $U_E = U_{In} - U_{BE}$.

or

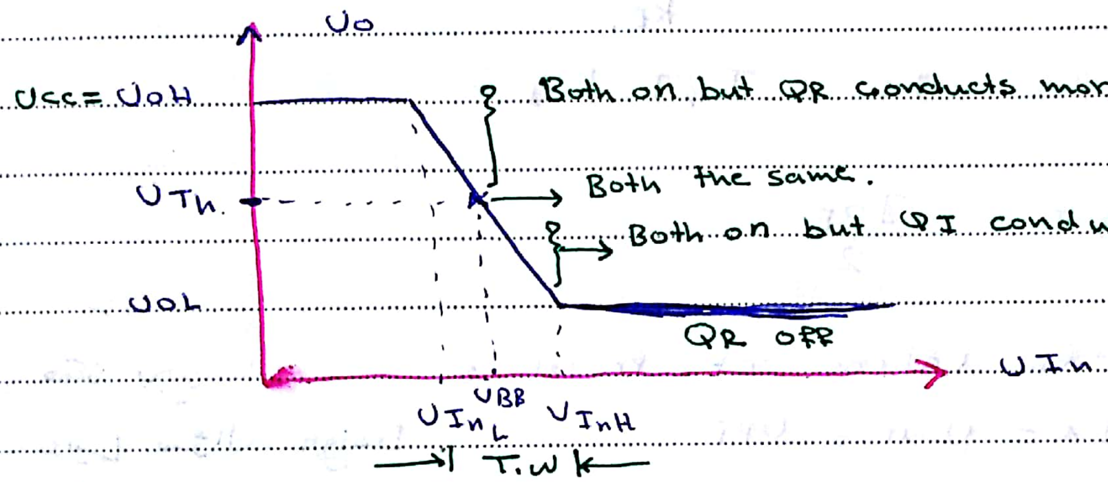
$U_E = U_{BB} - U_{BE}$, depends on which BJT is on.

* U_{BE} (F.A) = U_{BE} (ECL) = 0.75 V.

1_ if $V_{IN} < V_{BB}$, Q_I off, Q_R on.
V_{INV} high, V_{NINV} Low.

2_ if $V_{IN} > V_{BB}$, Q_I on, Q_R off
V_{INV} Low, V_{NINV} high.

11.2 EcL (current switch VTC).



لم فترة الانتقال من H إلى L.

* Consider V_{INV} for O/P.

1- V_{OH}

$V_{IN} < V_{BB}$.

Q_R on

$V_E = V_{BB} - V_{BE,R}$ (EcL).

$V_{BE,I} = V_{In} - V_E$

$= \underbrace{V_{IN} - V_{BB}}_{-ve} + V_{BE,R}$.

$V_{BE,I} < V_{BE}$ (EcL) $\Rightarrow$ Q_I off.

Subject: 80

$I_{C,I} = 0.$

$V_{out} = V_{OH} = V_{INV} = V_{CC}.$

* Threshold Voltage.

$V_{IN} = V_{BB}$, Q_I , $Q_R \rightarrow$ on

$$I_{RE} = \frac{V_{BB} - V_{BE,R}(ECL) + V_{EE}}{R_E} = 2I_{C,I}.$$

$V_{INV} = V_{CC} - I_{C,I} R_{CI}.$

$$I_{C,I} = \frac{I_{RE}}{2}.$$

- For certain values of resistors. — ممكن يجي

$V_{IN} = V_{out} = V_{BB}.$ — عليها سؤال Design.

* $T.W = 0.1 = V_{IH} - V_{IL}.$ — دائماً.

- $V_{InL} = V_{BB} - 0.05$
- $V_{InH} = V_{BB} + 0.05.$

* $V_{OL} \Rightarrow V_{IN} > V_{BB}.$

Q_I on

$V_E = V_{In} - V_{BE,I}(ECL).$

at $V_{IN} = V_{BB} + 0.05.$

* $V_{BE,R} = V_{BB} - V_E$

$= V_{BB} - V_{IN} + V_{BE,I}$

$V_{BE,R} = V_{BB} - V_{BB} - 0.05 + V_{BE,I}$

$V_{BE,R} < V_{BE}$ (ECL)

$\Rightarrow$ QR off.

– $I_{RE} = \dfrac{V_{IN} - V_{BE} + V_{EE}}{R_E} = I_{C,I}$

– $V_{INV} = V_{CC} - I_{C,I} R_{C,I}$

– $V_{IN} = V_S$, $V_{INV}(V_S)$: when QI saturats.

– QR does not saturats since V_{BB} is fixed.

* $I_{RE} = (V_S - V_{BE,I(sat)} + V_{EE}) / R_E \approx I_{C,I}$

– $V_{INV}(V_S) = V_{CC} - \dfrac{V_S - V_{BE,I(sat)} + V_{EE}}{R_E} R_{CI}$ .... eqn (1)

– $V_{INV} = V_S - V_{BC,I(sat)}$ .... eqn (2)

Solve 1 4 2 for V_S.

Subject: 82

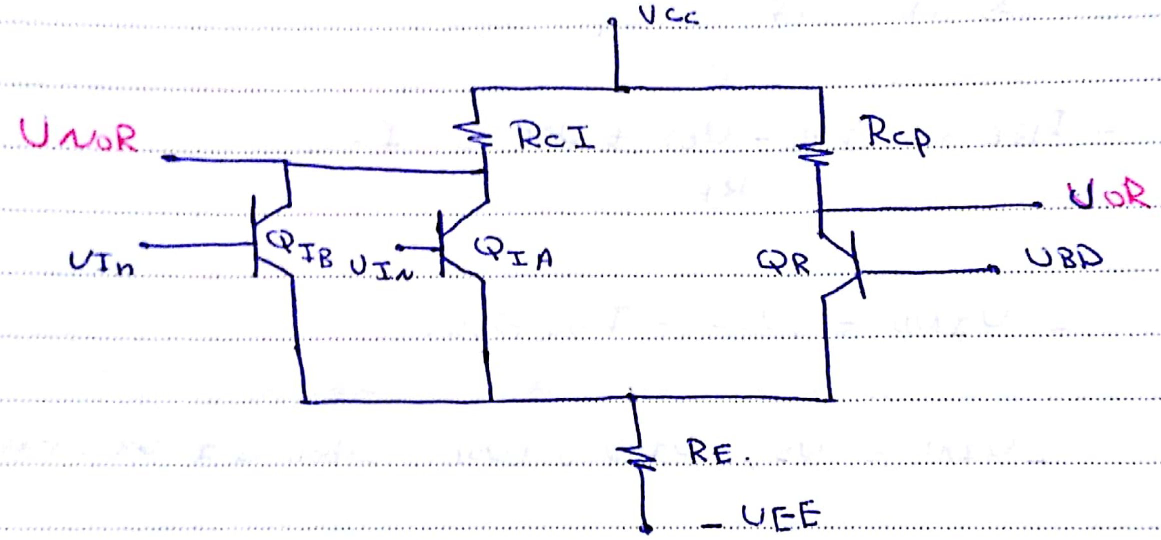
$$\star \quad V_S = \frac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E}\left[V_{BE}(sat) - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$$

Subject: 82   12 / 3 / 2018.

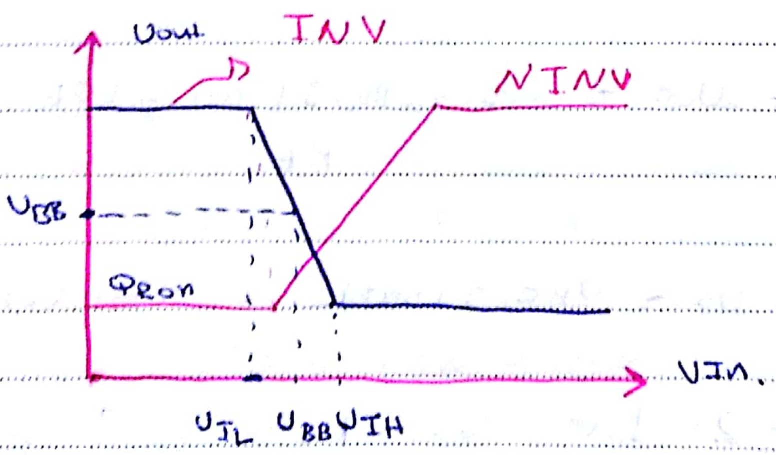
* $V_S = \dfrac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E}\left[V_{BE}(sat) - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$

* Example 11.1

- 11.4 Basic ECL, NOR, OR Gate.



- RcI < Rcp ⇒ , on يكونوا Trasastor حتى آخر.



Subject: 83

A	B	NOR	OR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

* Any input high QI on , QR off (corresponding).

$V_{NOR} = V_{CC} - I_{C,I} \; R_{C,I}$ --- Low

($I_{C,I} \rightarrow I_{R,E}$)

$V_{OR} \Rightarrow$ high.

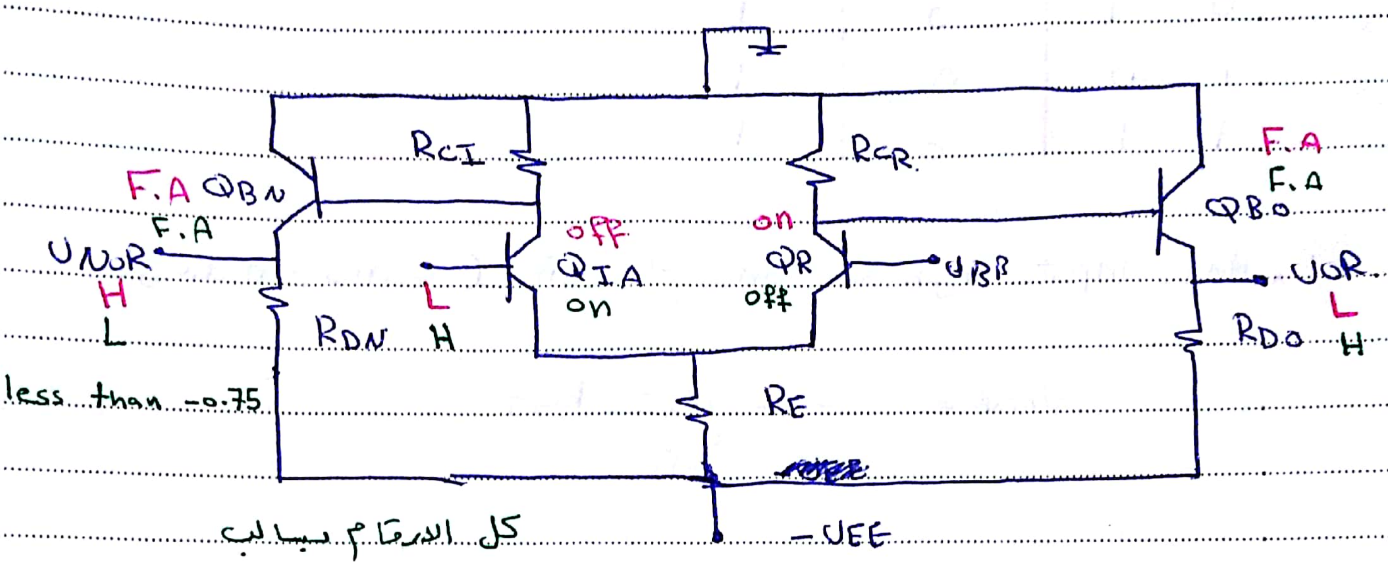
* All inputs Low , QI's off — $V_{NOR} \rightarrow$ high
  — $V_{OR} \rightarrow$ Low.

* Advantages :-

1- Low Sensitivity to noice, due to differential nature of the cct.
2- Vcc always provides cct with const current.

Subject: 8.4 / /

11.5 MECL (I) NOR/OR Gate with output (Buffer) :- مهمة للامتحان



الهدف منه رفع تيار ⟸ Fan-out ↑ ⟵ high speed ⟸ ما بنعرف احكم انه adv أو dis.

power ↑ ⟶ disadvantage ×

* QBN, QBO : Buffers (F.A)

- high output current → high Fan-out. ✓
  → high speed. (Fastest). ✓
  → high power dissipation ✗

* provides level Shifting between current Switch and UNOR and UOR.

For input and o/p to be compatible.

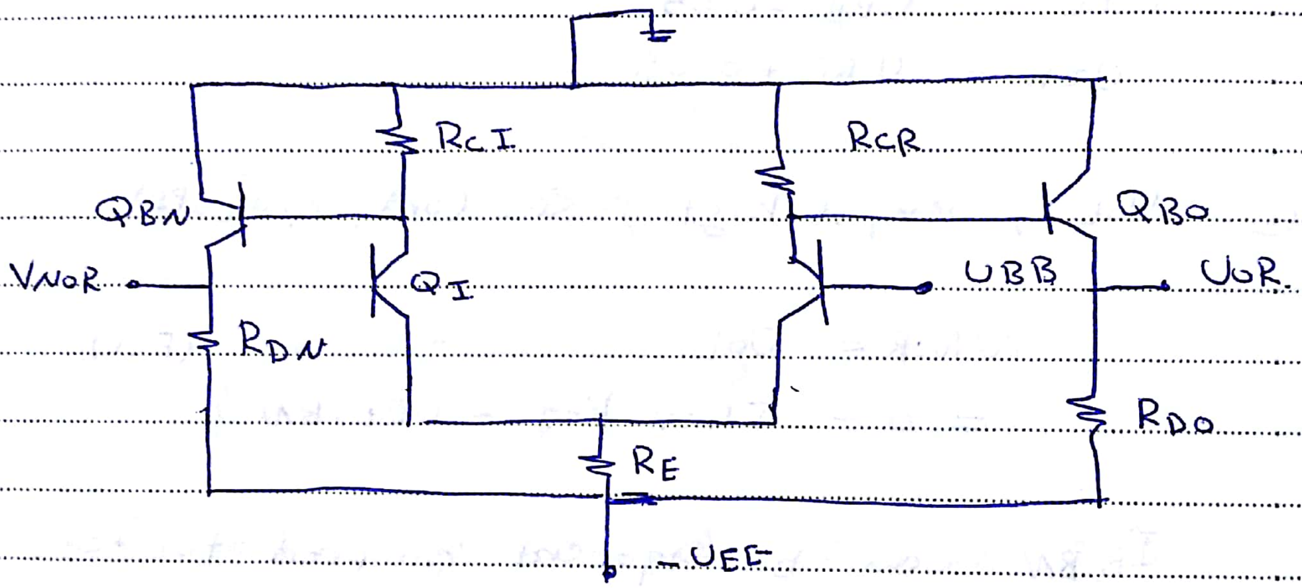
Subject: 8.5 20/3/2018.

R_{DN}, R_{DO} ⇒ pull - ~~up~~ down.

* disadvantage → high current spikes due to switching capability.

* For more than one input $R_{cI} < R_{cR}$

* 11.6 MEcL VTC.



* $\underline{V_{oH}}$ → input Low
QI off , QR on.

(EcL)

$V_{NoR} = V_{oH} = 0 - I_{B,BN} R_{c,I} - V_{BE,BN}$

Subject: 86

* $I_{B,BN} R_{CE} + V_{BE,BN} (ECL) + I_{E,BN} R_{DN} - V_{EE} = 0$

  ($I_{E,BN} \rightarrow I_{B,BN} (\beta_F + 1)$)

$$I_{B,BN} = \frac{V_{EE} - V_{BE}}{(R_{C,I} + R_{DN} (\beta_F + 1))}$$

② * V_{IL}, V_{IH} :-

$V_{IL} = V_{BB} - 0.05$

$V_{IH} = V_{BB} + 0.05$.

③ V_{OL}, input high, Q_I (on), Q_R (off).

$V_{NOR} = V_{OL}$ (ECL)

$= 0 - I_{RcI} R_{cI} - V_{BE,BN}$

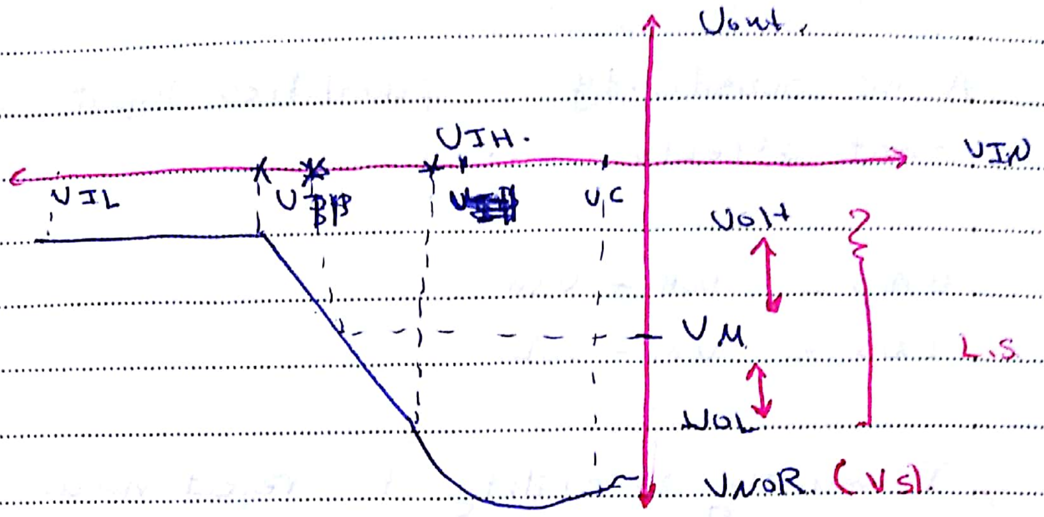
$I_{B,BN}$ can be iqonerd compred to I_{cI}.

$I_{RcI} \approx I_{c,I} \approx I_{E}$.

$$= \frac{V_{IH} - V_{BE,I} (ECL) + V_{EE}}{R_E}$$

$V_{IH} = V_{BB} + 0.05$.

% الكويز حطا Vcc بدي أحسب power منها وعالي من VEE



④ Vs and VNOR (Vs) when QI saturates.

$$V_{NOR} = -\left(\frac{+V_S - V_{BE,I(sat)} + V_{EE}}{R_E}\right) R_{CI} - V_{BE,BN(ECL)}$$

$$V_{NOR} = V_S - V_{BC,I(sat)} - V_{BE,BN}(ECL)$$

$$V_S = \frac{V_{BC(sat)} + \frac{R_{CI}}{R_E}\left[V_{BE(sat)} - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$$

Subject: 8.8

* Noise Sensitivity and Immunity.

– Noise Sensitivity :- quantifies input variations that affects output.

$$HNS = V_{OH} - V_m$$
$$LNS = V_m - V_{OL}.$$

* Immunity :- ability to reject noise $HNI = \frac{HNS}{Ls}$

$$HNI = \frac{V_{OH} - V_m}{Ls.}$$

$$LNI = \frac{LNS}{Ls} = \frac{V_m - V_{OL}}{Ls.}$$

– Example 11.2 $V_{BB} = -1.175.$

Immunity, Logic swing, noise margine.

$V_{OH} = -0.76$, $V_{IL} = -1.225$, $V_{IH} = -1.1225$

$V_{OL} = -1.55$, $V_S = -0.29$ V.

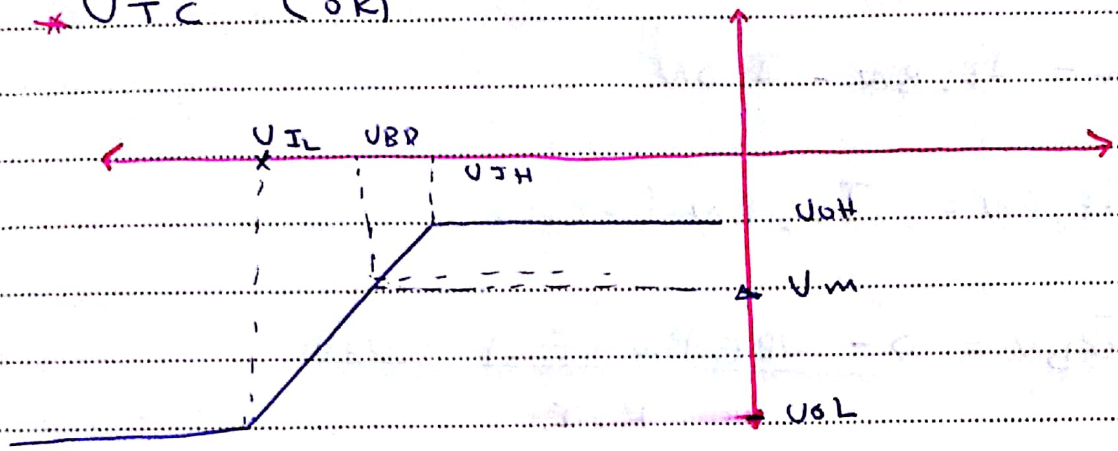
$V_{NOR} = -1.64$ V.

$$LS = -0.76 + 1.55 = 0.79.$$
$$HNm = -0.76 + 1.125 = 0.365.$$
$$LNm = -1.225 + 1.55 = 0.325.$$
$$HNI = \frac{-0.76 + 1.175}{0.79} = 0.53 \text{ V}.$$

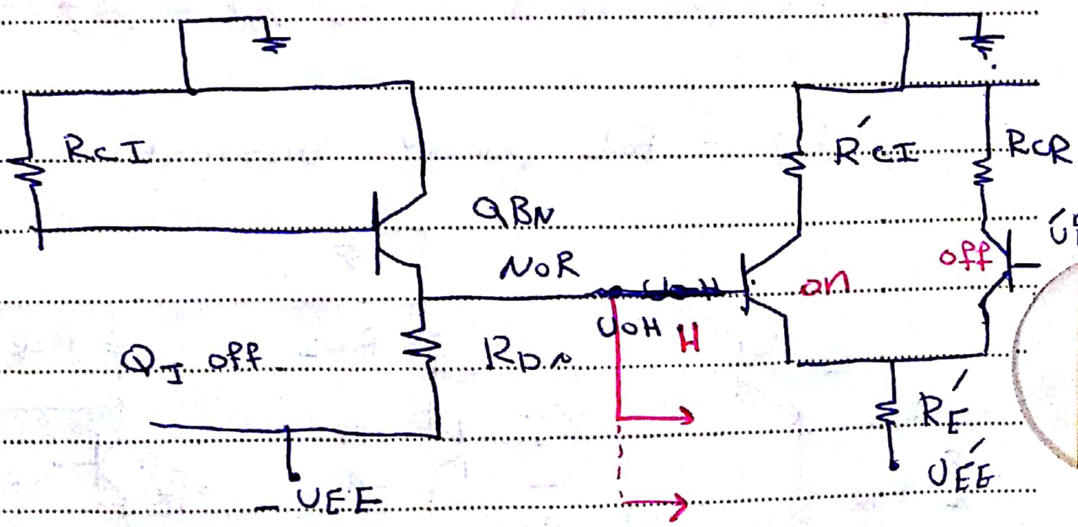
$$LNI = \frac{-1.175 + 1.55}{0.79} = 0.475\ V.$$

بالاترم تكون قسمة من 0.5.

* VTC (OR)



* 11.7 Fan-out MEcL(I) NoR.



$N = \frac{I_{OH}}{I_{IH}} \Rightarrow$ Load must be on.

$$I_{IH} = I_{B,BN} = \frac{I_{E,BN}}{\beta+1} = \frac{I_{RE}}{\beta+1}$$

$$I_{RE} = \frac{V_{OH} - V_{BE,I}\,(ECL) + V_{EE}}{R_E}$$

$$I_{OH} = I_{E,BN} - I_{RDN}$$

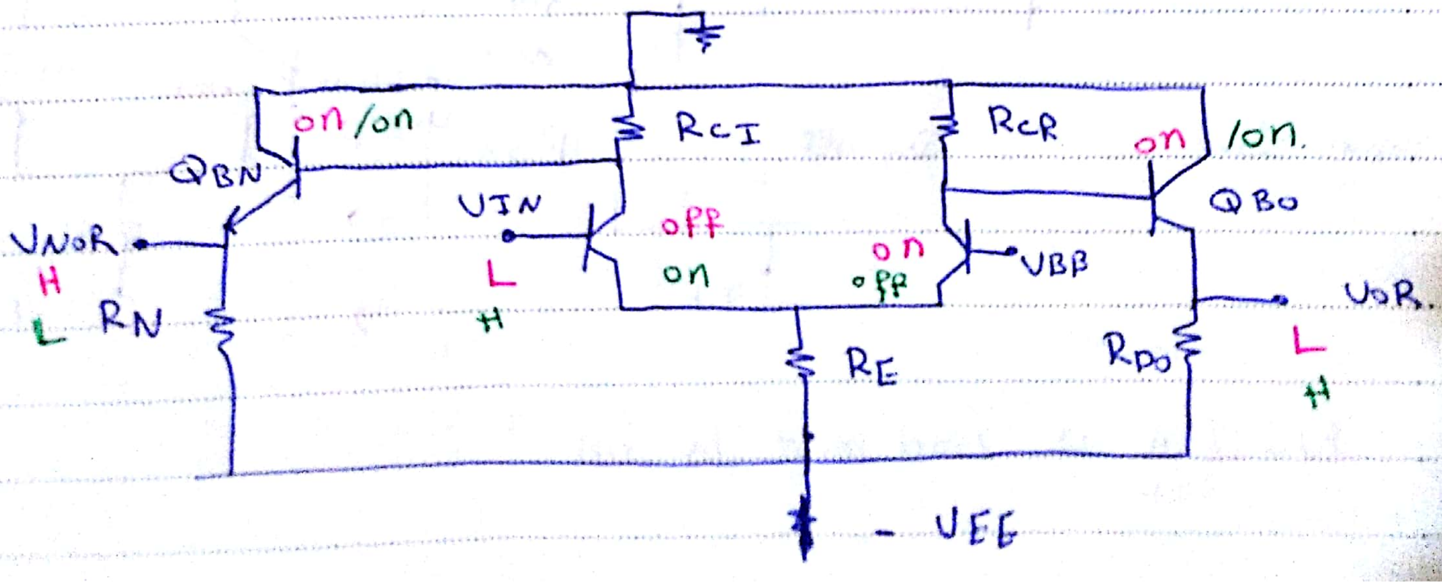
$$I_{E,BN} = I_{B,BN}\,(\beta_F+1)$$

$$I_{RBN} = \frac{0 - V_{BE,BN}\,(ECL) - V_{OH}}{R_{CI}}$$

$$I_{RDN} = \frac{V_{OH} + V_{EE}}{R_{DN}}$$

+ Example 11.3 ⇒ $N = 87.5 = 87$

* 11.8 :- ECL power Dissipation.



* I_{EE} (oH) input Low :-

1) $I_{RE}(oH) = \frac{V_{BB} - V_{BE,R} + V_{EE}}{R_E}$

2) $I_{RDN}(oH) = \frac{V_{oH} + V_{EE}}{R_{DN}}$

3) $I_{RDo}(oH) = \frac{V_{oL} + V_{EE}}{R_{Do}}$

$I_{EE} = \Sigma$ current (oH).

* I_{EE} (oL), input high :-

$I_{RE}(oL) = \frac{V_{IN} - V_{BE,I} + V_{EE}}{R_E}$ (V_{IN} → V_{oH})

$I_{RD_N}(oL) = \frac{V_{oL} + V_{EE}}{R_{DN}}$ (NOR)

$I_{RDo}(oL) = \frac{V_{oH} + V_{EE}}{R_{Do}}$ (OR)

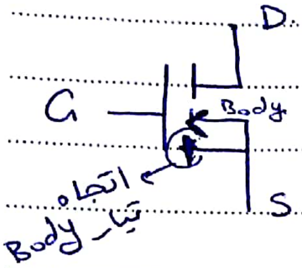
* Example :- $P_{avg_{EE}} = \frac{I_{EE}(oH) + I_{EE}(oL)}{2}$ V_{cc}

$= 35.6$ mW

Subject: 92

* Chapter 16 :- Metal oxide Semiconductor (FET) :-
MosFET.

- N-Mos , PMos



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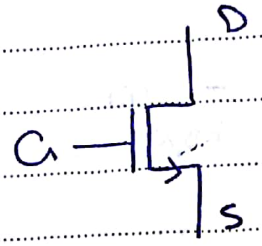


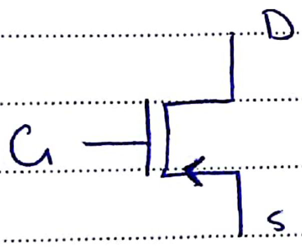
نفس اتجاه تيار
بالحالتين.

N- Mos

I_G = Zero.

وضع نفس الشكل من غير سهم.

* P- Mos :-



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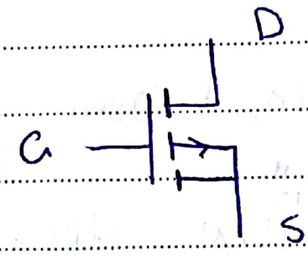

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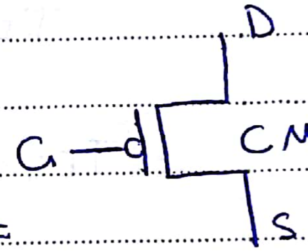
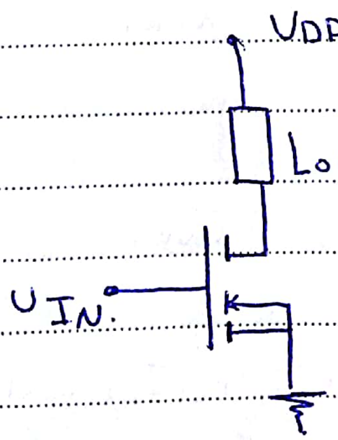


CMos.



Load ⇒ R (17), NMos (19), PMos (23,24).

* Enhamement :- V_{TN} +ve
V_{TP} -ve.

* 16.3. MosFET operation Modes (NMos)

* Cut off → $V_{GS} < V_{TN}$, NMos off.

  $I_D = 0$.

* linear mode.

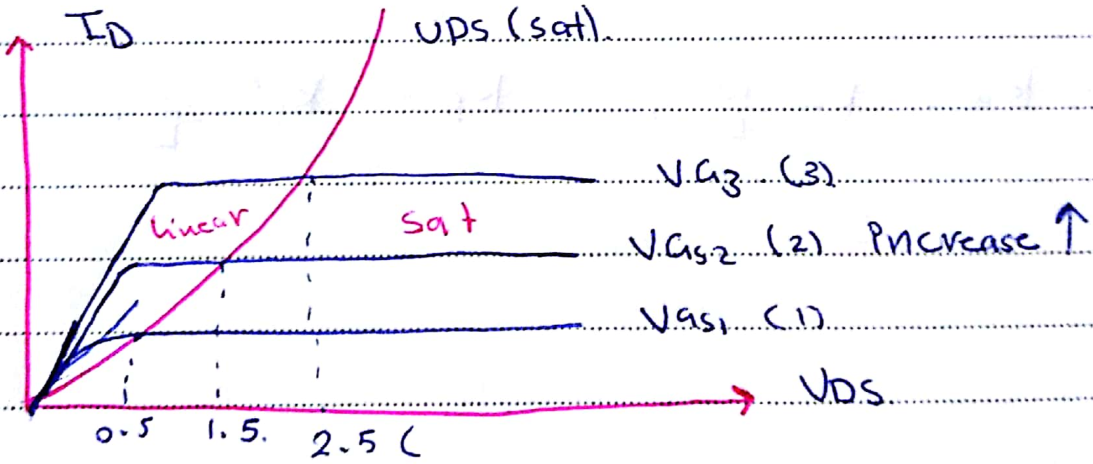
$V_{GS} \geq V_{TN}$, $V_{DS} < V_{DS(sat)}$.

$V_{DS(sat)} = V_{GS} - V_{TN}$.

$$I_{D(lin)} = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

↳ Trans conductance (mA/V²)

*



$V_{DS(sat)} = V_{GS} - V_{TN}$.

* Sat Mode. , $V_{GS} > V_{TN}$

$$I_{D(sat)} = \frac{K_n}{2} (V_{GS} - V_{TN})^2.$$

- $V_{DS} \geq V_{DS(sat)}$.

* 16.4 Mosfet Transconductance :-

$k_n = \underbrace{\mu_n C'_{ox}}_{k'_n} \frac{W}{L}$ → width and length of gate

area = WL.

$k_p = \underbrace{\mu_p C'_{ox}}_{k'_p} \frac{W}{L}$

μ :- mobility of electrons or holds.

C'_{ox} :- capacitance of oxide Layer per unit area

$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, ϵ_{ox} : permitlivity of oxide

t_{ox} :- thickness of oxide.

$\therefore k_n = k'_n \frac{W}{L}$, $k_p = k'_p \frac{W}{L}$.

2) $V_{SG} > -V_{Tp}$

$V_{SD} < V_{SD(sat)}$ linear.

$V_{SD(sat)} = V_{SG} + V_{Tp}$

$I_{Dp} = k_p \left[\left(V_{SG} + V_{Tp} \right) V_{SD} - \frac{V_{SD}^2}{2} \right]$

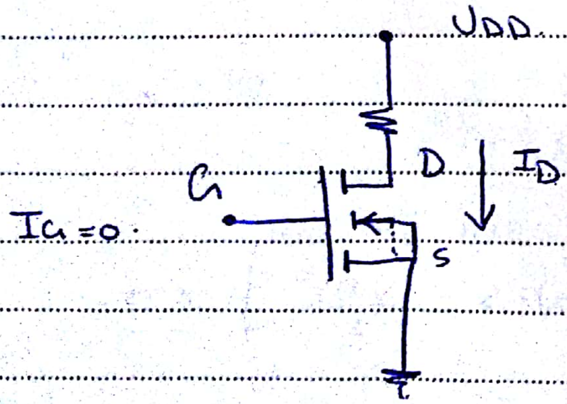
3) $V_{SG} > -V_{Tp}$

$V_{SD} \geq V_{SD(sat)}$.

$I_{Dp} = \frac{k_p}{2} \left(V_{SG} + V_{Tp} \right)^2$.

* Chapter 17 :- Introduction to Mos Digital cct.

General N Mos Inverter



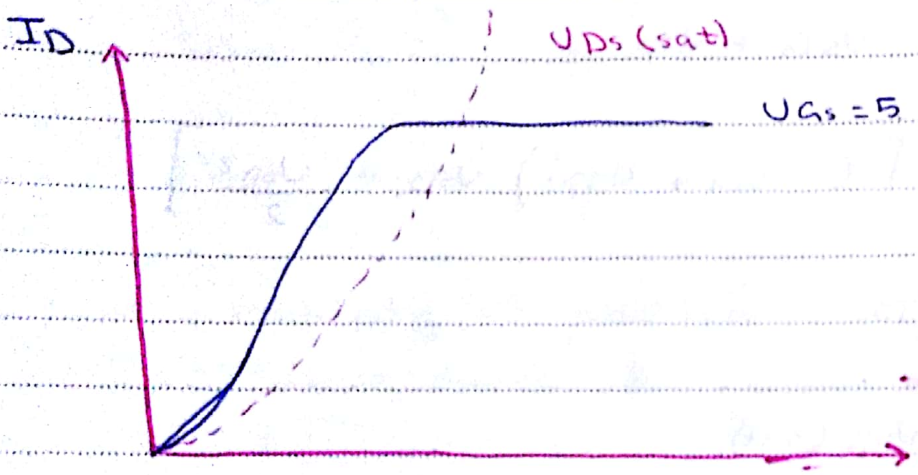
$V_{IN} = V_{GS}$

$V_{out} = V_{DS}$.

Subject: 96

- $V_{out} = V_{DD} - I_D R_L$

17.2 Zero-Drain Current Mosfet :-



$V_{DS(sat)} > 0$

$V_{GS} > V_{TN} \longrightarrow$ linear on.

$I_D \longrightarrow 0$

$V_{DS} \longrightarrow 0$, but in active mode.

* Mathematically :-

V_{GS} high $\longrightarrow$ Active mode

$$I_D = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right] = 0.$$

$$V_{DS} = 2 \underbrace{(V_{GS} - V_{TN})}_{V_{DS}} > V_{DS}$$

$V_{DS} > V_{DS(sat)}$. | $2 V_{DS(sat)} > V_{DS(sat)}$

Subject: 97

Example 17.1 , Find Resistance of D-S channel R_{DS}:-

$V_{GS} = 5$, $V_T = 1$, $k = 40 \mu A / V^2$

a) $V_{DS} = 3$,

$$I_D = k_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\frac{dI_D}{dV_{DS}} = R_{DS}^{-1}$$

$$\frac{dI_D}{dV_{DS}} = k_n (V_{GS} - V_{Tn} - V_{DS})$$

$$\frac{dV_{DS}}{dI_D} = \frac{1}{k_n (V_{GS} - V_{Tn} - V_{DS})}$$

$$R_{DS} = \frac{1}{40\mu (5-1-3)} = 25k\,\Omega$$

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}$$

b) $V_{DS} = 0$:

$$R_{DS} = \frac{1}{40\mu (5-1)} = 6.25 k\Omega$$

$V_{DS} \uparrow$, $R_{DS} \uparrow$, conductivity $\downarrow$

$V_{DS} \downarrow$, $R_{DS} \downarrow$, " $\uparrow$.

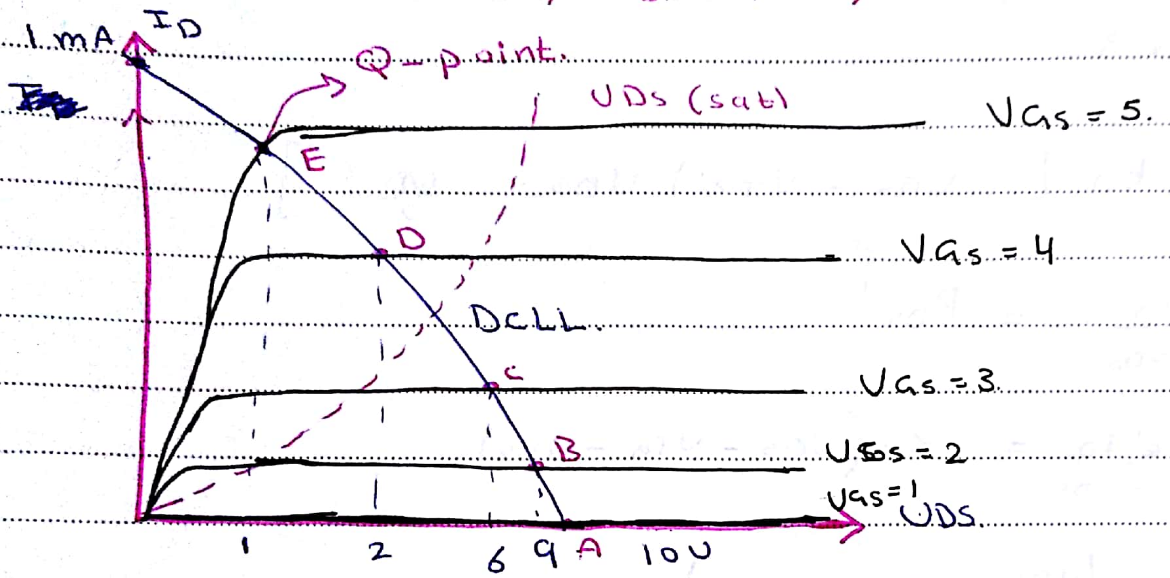
⟹ N Mos is used as a pull - down

P Mos is used as a pull - up.

Subject: 98 / /

* Example 17.2 :- Graphicall Determine VTC

$R_L = 10k\Omega$, $V_{DD} = 10V$, $V_{TN} = 1$, $K = 2mA/V^2$.



$V_{DD} = I_D R_L + V_{DS} \Rightarrow$ DCLL معادلة

↓ DC Load line.

$V_{DS} = V_{DD} - I_D R_L$.

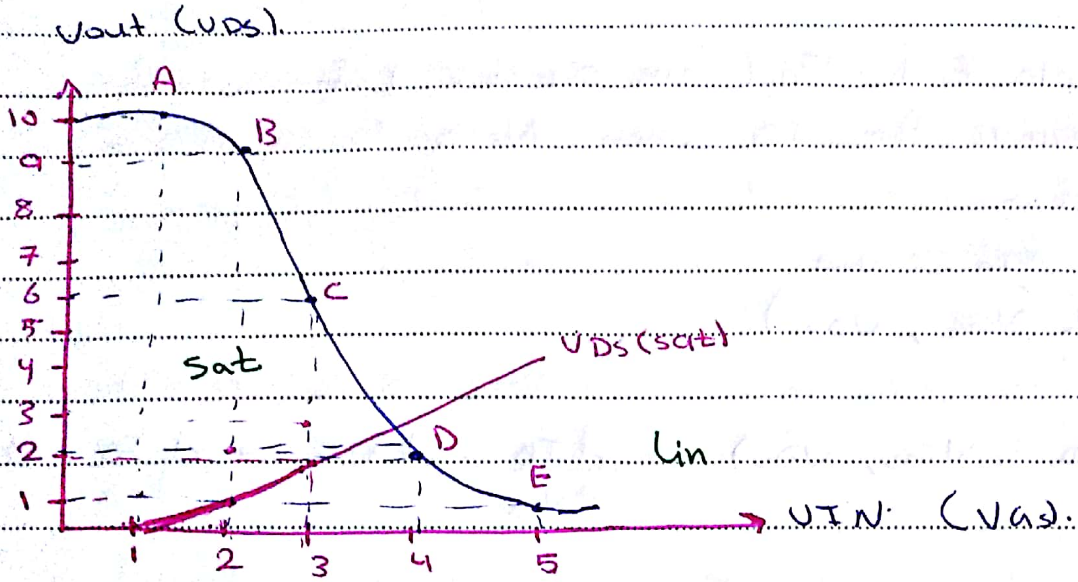
at $I_D = 0$, $V_{DS} = V_{DD} = 10V$

at $V_{GS} = 0$, $I_D = \frac{V_{DD}}{R_L} = 1mA$.

A, B, C, D, E $\Rightarrow$ Q-point.

E, D $\Rightarrow$ linear, C, B, A $\Rightarrow$ Sat.

Subject: 99 / /



$V_{DS}(sat) = V_{GS} - V_{TN}$

A, B, C : sat , $I_D = \frac{k_n}{2}(V_{GS} - V_{TN})^2$

$V_{GS} =$ 1, 2, 3 Volt

$V_{DS} = V_{DD} - I_D R$

C, D : linear. $V_{GS} =$ 4, 5

حذف وتعويض

ونطلع

$I_D = k_n\left[(V_{GS} - V_{TN}) - \frac{V_{DS}^2}{2}\right]$

$V_{DS} = V_{DD} - I_D R_L$

I_D, V_{DS}

	V_{GS}	I_D (mA)	V_{DS}
sat	A ← 1	0 →	10
sat	B ← 2	1 →	9
	C ← 3	4 →	6
linear	D ← 4	8 →	2
linear	E ← 5	9 →	1

Subject: 100 — 28/3/2018

* Example 7.4, Find the partial Differential equation for ID when NMos is in linear Mode.

$$I_D(\underbrace{V_{GS}}_{V_{In}}, \underbrace{V_{DS}}_{V_{out}})$$

$$dI_D(V_{GS}, V_{DS}) = \frac{dI_D}{dV_{GS}} \cdot dV_{GS} + \frac{dI_D}{dV_{DS}} \cdot dV_{DS}$$

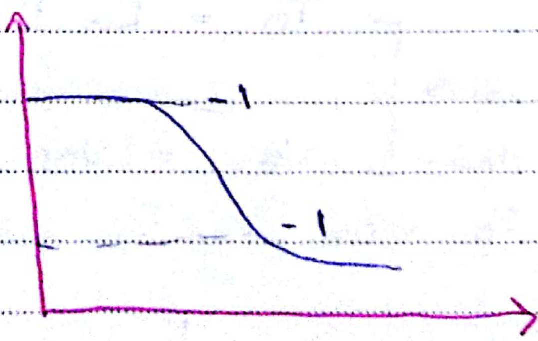
$$I_D = k_n \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\frac{dI_D}{dV_{GS}} = k_n V_{DS}$$

$$\frac{dI_D}{dV_{DS}} = k_n (V_{GS} - V_{Tn} - V_{DS})$$

$$dI_D = k_n \underbrace{V_{DS}}_{V_{out}} \underbrace{dV_{GS}}_{dV_{In}} + k_n \underbrace{(V_{GS} - V_{Tn} - V_{DS})}_{V_{In}} \underbrace{dV_{DS}}_{dV_{out}}$$

$$\frac{dV_{out}}{dV_{In}} = -1$$



* 17.6 Power Dissipation

* Static power Dissipation.

$$P_{DD}(avg) = V_{DD} \frac{I_{DD}(OH) + I_{DD}(OL)}{2}$$

* Dynamic power Dissipation :-
exicts also in BJT ccts, but ignored ($P_{dy} << P_{static}$) for Mos, P_{static} is also small and P_{dyn} can't be ignored.

* P_{dyn} : found when output switches between high and Low.

* MosFet ccts have the smallest power Dissipation.

- CMos have the Lasest power dissipation amongst all Logic cct.

- $P_{Dyn} = C_L \, \nu \, V_{DD}$
  ↳ switching freq., capacitance for Load

- $P_{Total} = P_{stat} + P_{dyn}$

* Example 17.5, $V_{DD} = 5$, $\nu = 0.5\ MHz$, $C_L = 10\ pF$
$I_{DD}(OH) = 5\mu$, $I_{DD}(OL) = 12\mu$.

$P_{Dyn} = 10p \times 0.5M \times 25 = 125\ \mu w$.

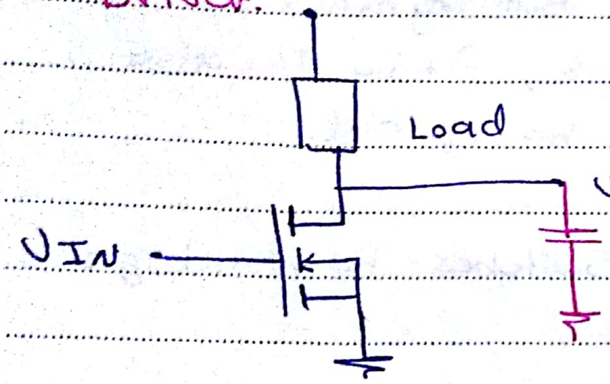
$P_{stat} = \frac{5\mu + 12\mu}{2} \times 5 = 262\ \mu w$.

$P_T = 125 + 262 = 387\ \mu w = 0.387\ mW$.

Subject: 102 / /

* 17.7 Fan – out.

Driver.



$C_{L,eq}$ (تأثر على سرعة من h و L)

– Fan-out : Max capacitance allowed at out of driver that can produce an acceptable Switing time.

① – charging
input $H \rightarrow L$, output $L \rightarrow H$
N lin → off , cap will charge.

$$I_{CL} = I_L = C_L \frac{d v_{out}}{dt}$$

② dis charging:
input $L \rightarrow H$, output $H \rightarrow L$
N off → lin , cap will dis charging.

$$* \; I_{CL} = I_D - I_L = C_L \frac{d v_{out}}{dt}$$

$$I_{CL} = C_L \frac{d v_{out}}{dt}.$$

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$$I_{CL} = C_L \frac{dv_{out}}{dt}$$

$$\int_{t_1}^{t_2} dt = \frac{C_L}{I_{CL}} \int_{v_1}^{v_2} dv_{out}$$

$$\Delta t = \frac{C_L}{I_{CL}} \Delta V$$

* Example 17.6, Find C_L, Max for $\Delta t = 1\,\mu s$ (max switching time).

$I_{CL\,charge} = 50\,\mu A$, $I_{CL\,Dicharg} = -20\,\mu A$

$V_{OH} = 5\,V$, $V_{OL} = 0.5$

$$C_L = I_{CL} \frac{\Delta t}{\Delta V} \rightarrow \text{Charging}$$

$$C_L = 50\mu \frac{1\mu}{5-0.5} = 11.1\,pF$$

② Discharging:

$$C_L = \frac{(-20\mu)\,(1\mu)}{(0.5-5)} = 4.44\,pF$$

① if you pick $C_L = 11.1\,pF$ find Δt for both cases.

$\Delta t_{ch} = 1\,\mu$, $\Delta t_{dis} = \frac{11.1\,pF}{-20}(-4.5) = 2.5\,\mu$

> 1

* لما تحقق شرط طلع Δt اكبر ا بجرب غيرها

* $C_L = 4.44\,pF$

$$\Delta t_{,ch} = \frac{4.44 * 4.5}{50\mu} = 0.4\,\mu s$$

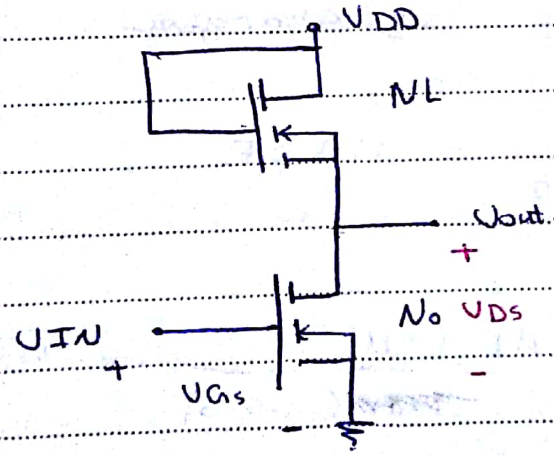
$\Delta t_{,dis} = 1\,\mu s.$

باخد CL الأقل حتى أجيب At أقل من 1 μ,

$\therefore C_L = 4.44\,pF$, is the correct answer, obvious since it was obtained from the smaller current.

* Chapter 19 Staturated Enhancement only Loaded NMOS Inverter.

+ 19.1 and 19.3 operation + VTC.



$V_{IN} = V_{GSO}$

$V_{out} = V_{DSO}$.

DL and GL are connected

$V_{GSL} = V_{DSL}$

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$V_{DSL}(sat) = V_{GSL} - V_{TL} = V_{DSL} - V_{TL}$

$V_{DSL} > V_{DSL}(sat)$

$\Rightarrow$ NL always saturating

① VIN Low, No off.

$V_{IN} < V_{To}$

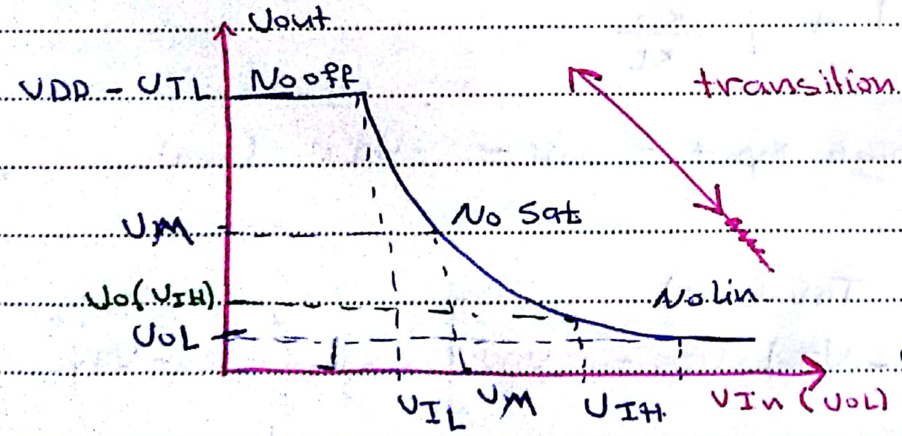
$V_{GS} < V_{To}$

$V_{out} = V_{DD} - V_{DSL}$

$I_{Do} = Zero = I_{DL}(sat) = \frac{K_L}{2}\left[V_{GSL} - V_{TL}\right]^2$

$V_{GSL} = V_{TL}$

$V_{out} = V_{OH} = V_{DD} - V_{TL}$



② VIL can't be formad at $\frac{dV_{out}}{dV_{In}} = -1$ due discontinuily $V_{IL} = V_{To}$.

② during transition both saturate.

$I_{DL}(sat) = I_{Do}(sat)$.

$$\frac{K_L}{2}\left(V_{GSL}-V_{TL}\right)^2=\frac{k_o}{2}\left(V_{GSo}-V_{To}\right)^2$$

$V_{GSL} = V_{DD} - V_{out}$ } --- (1)

$V_{GSo} = V_{IN}$.

$$V_{out} = -\sqrt{\frac{k_o}{K_L}}\; V_{IN} + V_{To}\sqrt{\frac{k_o}{K_L}} + V_{DD} - V_{TL} \quad \text{--- (2)}$$

the bigger $\sqrt{\frac{k_o}{K_L}}$, the steeper the VTC curve.

(3) mid point $V_{In} = V_{out} = V_M$. Both sat.
either (1) or (2)

$$V_M = \frac{V_{To}\sqrt{\frac{k_o}{K_L}} + V_{DD} - V_{TL}}{1+\sqrt{\frac{K_o}{K_L}}}$$

(4) V_{OL}, at high input $= V_{OH} = V_{IN}$ (V_{OL}).

I_{Do} (Lin) $= I_{DL}$ (sat).

$$k_o\left[\left(V_{GS_o}-V_{To}\right)V_{DS}-\frac{V_{DS}^2}{2}\right]=\frac{K_L}{2}\left(V_{GS}-V_{TL}\right)^2$$

$V_{GS} = V_{IN}\ (V_{OL}) = V_{DD} - V_{TL}$.

$V_{DSo} = V_o = V_{OL}$.

$V_{GSL} = V_{DD} - V_{out} = V_{DD} - V_{OL}$.

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$$V_{OL} = \frac{K_L (V_{DD} - V_{TL})^2}{2K_L (V_{DD} - V_{TL}) + 2K_o (V_{DD} - V_{TL})}$$

⑤ V_{IH} at $\frac{dV_{out}}{dV_{IN}} = -1$, No Lin

I_{DL} (sat) = I_{Do} (linear) — quadratic eq.

$d\,I_{DL}$ (sat) = $d\,I_{Do}$ (linear). ---- ③

$$I_{DL}(sat) = \frac{K_L}{2} (V_{DD} - V_{out})^2$$

$$I_{Do} = K_o \left[(V_{IN} - V_{To}) V_{out} - \frac{V_{out}^2}{2} \right] \quad ---- ④$$

③ : $\frac{dI_{DL}}{dV_{out}} * dV_{out} = \frac{dI_{Do}}{dV_{IN}} dV_{IN} + \frac{dI_{Do}}{dV_{out}} dV_{out}$

$$\frac{dV_{out}}{dV_{IN}} = \frac{\frac{dI_{Do}}{dV_{IN}}}{\frac{dI_{DL}}{dV_{out}} - \frac{dI_{Do}}{dV_{out}}} = -1.$$

$$\frac{dI_{Do}}{dV_{IN}} = K_o V_{out}$$

$$\frac{\partial I_{DL}}{\partial V_{out}} = -K_L (V_{DD} - V_{out})$$

$$\frac{\partial I_{Do}}{\partial V_{out}} = K_o (V_{IN} - V_{To} - V_{out})$$

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$$\frac{d V_{out}}{d V_{IN}} = \frac{k_o (V_{IH} - V_{To}) + k_L (V_{DD} - V_{TL})}{2 k_o + k_L}.$$

from quadratic equation → anothe relation

between

V_{out} V_{IN} ⇒ $V_{IH} = V_{To} + \dfrac{2 (V_{DD} - V_{TL})}{\sqrt{\frac{3 k_o}{k_L} + 1}}$

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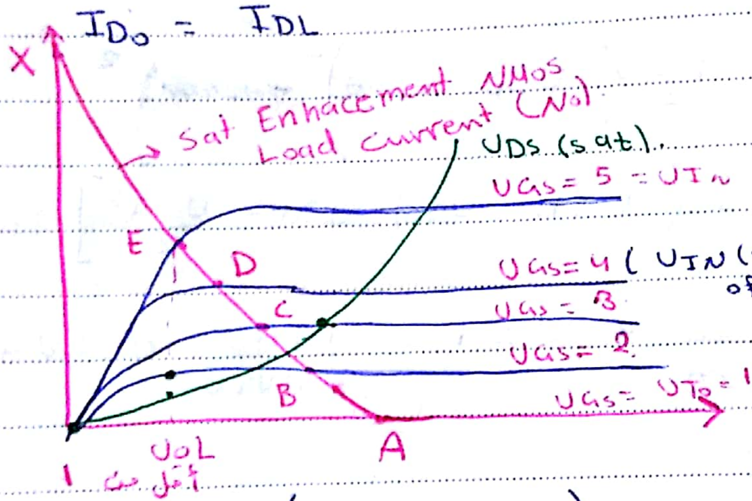
$$\frac{dV_{out}}{dV_{IN}} = \frac{K_o(V_{IH} - V_{To}) + K_L(V_{DD} - V_{TL})}{2K_o + K_L}$$

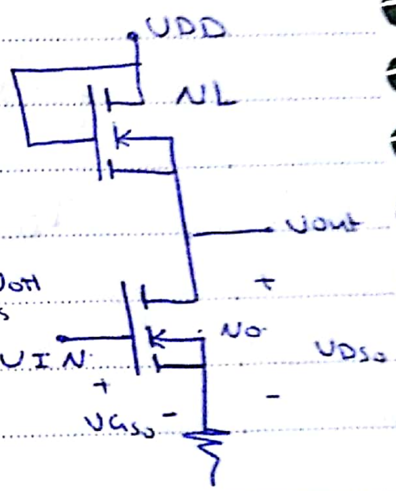
from quadratic equation → another relation between

V_{out} V_{IN} ⇒ $V_{IH} = V_{To} + \dfrac{2(V_{DD} - V_{TL})}{\sqrt{\frac{3K_o}{K_L} + 1}}$

- Example *

موجود داخل شكل ص ٣٧





(I-V char)

at X :- $V_{DSo} = 0$.

$$I_{DL} = I_{Do} = \frac{K_L}{2}(V_{GSL} - V_{TL})^2$$

$$V_{GSL} = V_{DSL} = V_{DD} - \cancel{V_{out}}^{\,0} = V_{DD}$$

$$I_{DL} = \frac{K_L}{2}(V_{DD} - V_{TL})^2.$$

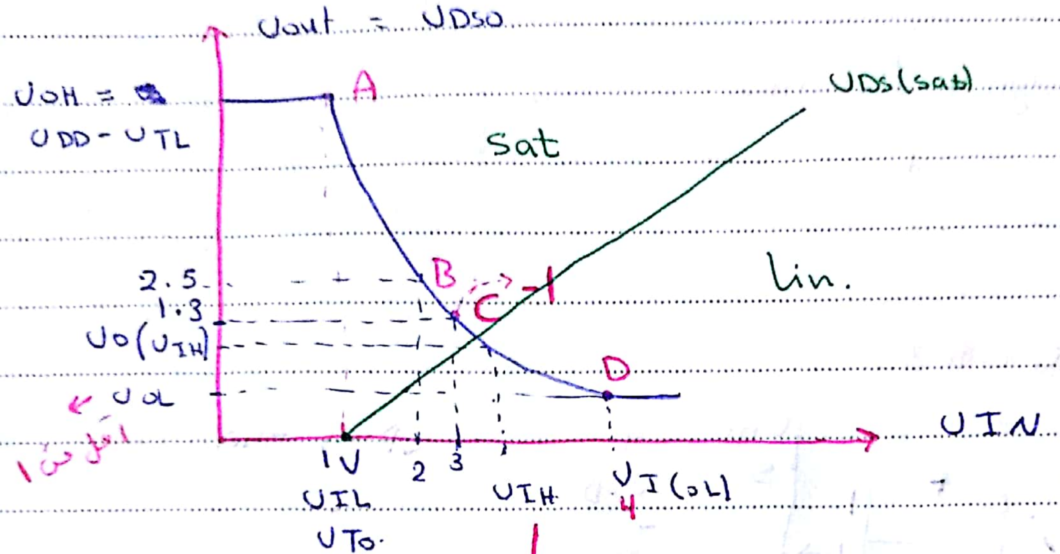
at A : $I_{Do} = 0 = \frac{K_L}{2}(V_{GSL} - V_{TL})^2$

$$V_{GSL} = V_{TL}.$$

$V_{out} = V_{DD} - V_{TL}$ (N_o off)

$V_{IL} = V_{To}$

* رسمة UTC



B, C لو تكون واحدة من
C, D او

* $V_{DS(sat)} = V_{GS} - V_T$

* 19.3 power Dissipation

1_ Static

$I_{DD}(oH) = 0$ ∴ , VIN Low , $N_o = 0$, $I_{Do}(off) = I_{D_L}(sat) = 0$

$I_{DD}(oL) = I_{DL}(sat) = I_{Do}(lin)$

$$= \frac{K_L}{2}(V_{GS} - V_{TL})^2 = K_D\left((V_{GSo} - V_{To})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$P_{DD}(avg) = \frac{I_{DD}(oL)}{2} V_{DD}$$ أقل power

Subject: ilo / /

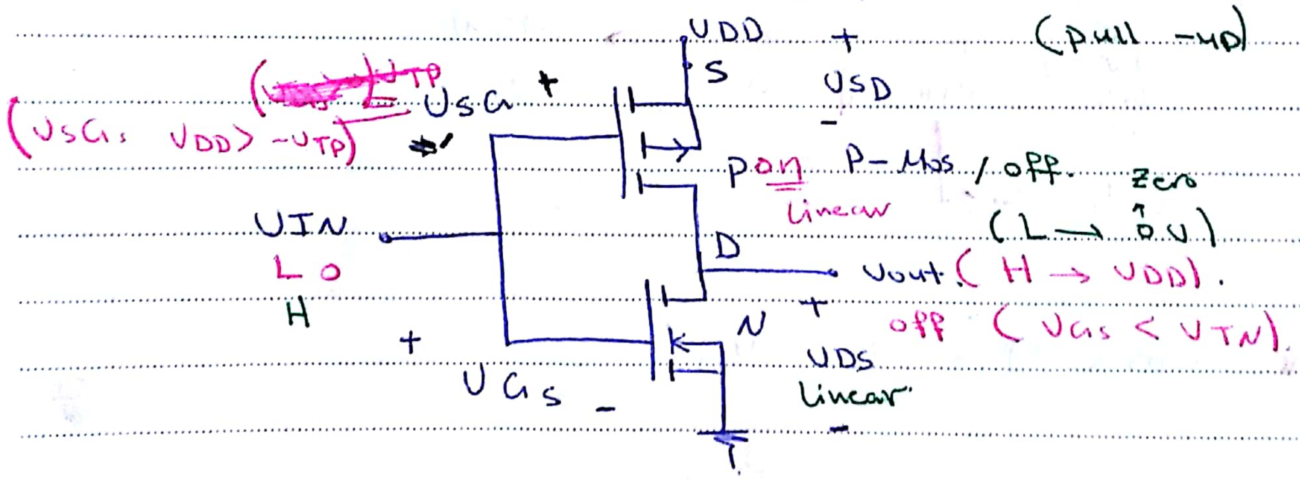
2- Dynamic.

$$P_{dyn} = C_L \nu' V_{DD}^2.$$

$$P_{tot} = P_{dyn} + P_{static}.$$

* Chapter 23

23.1 CMOS Inverter.



$V_{IN} = V_{GS}$

$V_{out} = V_{DS}.$

$V_{SD} = V_{DD} - V_{out}.$

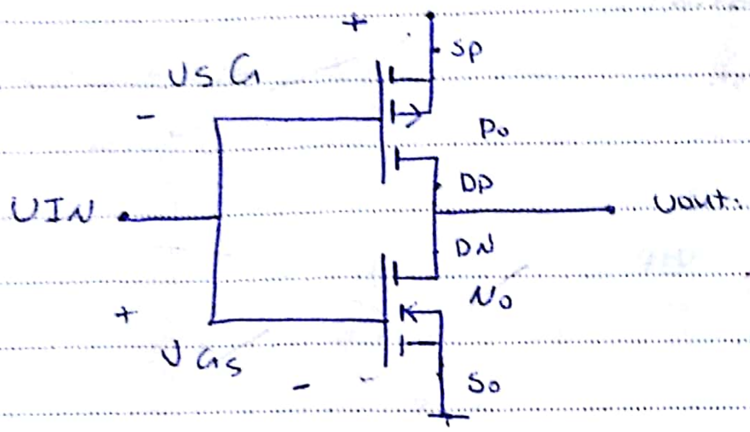
$V_{SG} = V_{DD} - V_{IN}.$

P-Mos ⇒ pull -up

N- Mos ⇒ pull - down.

Subject: 111

* 23.1 CMOS Inverter + 23.4 VTC



① VIN Low, $V_{IN} = 0$.

$V_{IN} < V_{TN}$

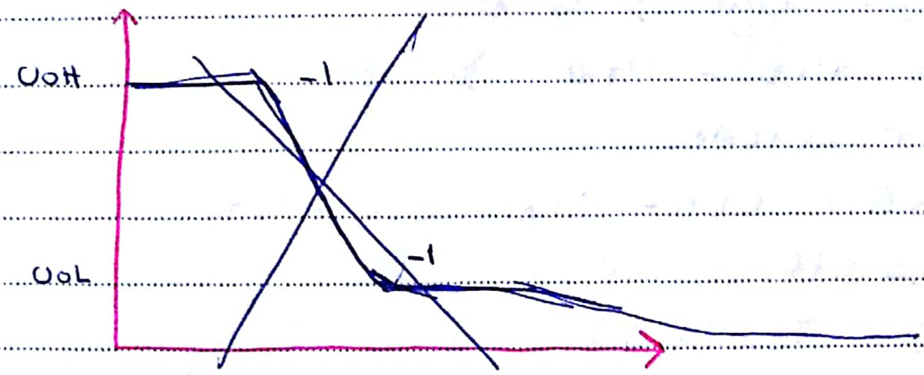
N → off, $I_{DN} = 0$.

$V_{SG} = V_{DD} > -V_{TP}$.

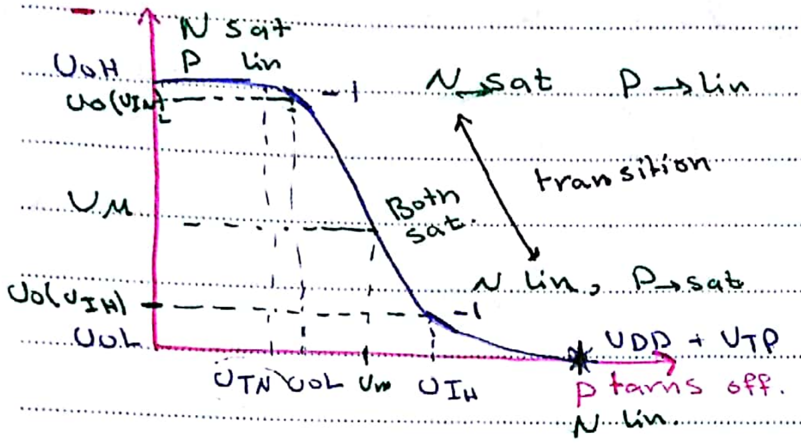
$V_{SD}(sat) = V_{SG} + V_{TP} = V_{DD} + V_{TP} > V_{SD}$

PMOS in linear region.

$I_{DN}(off) = I_{DP}(lin)$



S T A R S Notebook



x لا يكونوا sat(c) يكونه تيار أعلى ما يمكن.

$I_{DN}(off) = I_{DP}(lin)$

$$0 = k_p\left[(V_{SG} + V_{TP})\,V_{SD} - \frac{V_{SD}^2}{2}\right]$$

$V_{SD} = \text{Zero}.$

$V_{SD} = 2(V_{SG} + V_{TP}) > V_{TP}(sat)$ غلط لا باصفرها.

$V_{out} = V_{OH} = V_{DD}$

② V_{OL}, $V_{IN} = V_{DD}$.

high input.

$V_{IN} = V_{DD} = V_{GS} > V_{TN}$

$V_{DS}(sat) = V_{DD} - V_{TN} > V_{DS}$

⇒ linear mode.

$V_{SG} = V_{DD} - V_{IN} = 0 < -V_{TP}$

PMOS → off.

$I_{DP}(off) = I_{DN}(lin)$.

$$0 = k_n\left((V_{GS} - V_{TN})\,V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$V_{DS} = 0$.

$V_{out} = V_{OL} = V_{DS} = 0.$

* $V_{SG} < -V_{TP}.$

$V_{DD} - V_{IN} < -V_{TP}.$

$V_{IN} > V_{DD} + V_{TP}.$

(3) at $V_m = V_{IN} = V_{out}.$

Both sat.

$I_{DP}(sat) = I_{DN}(sat).$

$$\frac{k_p}{2}\left(V_{DD} - V_m + V_{TP}\right)^2 = \frac{k_n}{2}\left(V_m - V_{TN}\right)^2.$$

$$V_m = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\frac{k_n}{k_p}}}{1 + \sqrt{\frac{k_n}{k_p}}}$$

(4) at $\frac{dV_{out}}{dV_{IN}} = -1$, V_{IL}.

N-sat : $I_{DN}(sat) = \frac{k_n}{2}\left(V_{IN} - V_{TN}\right)^2.$

P-lin : $I_{DP} = k_p\left[(V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}\right]$

$d\,I_{DN}(V_{IN}) = d\,I_{DP}(V_{IN}, V_{out}).$

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{TP} + \frac{k_n}{k_p} V_{TN}}{1 + \frac{k_n}{k_p}}$$

* V_{out} from $I_{DN}(sat) = I_{Dp}(lin)$.

N (lin) $\Rightarrow I_D(lin) = k_n\left((V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right)$

P (sat) $\Rightarrow I_D(sat) = \frac{k_p}{2}(V_{SG} + V_{Tp})^2$

$\rightarrow V_{DS} = V_{out}$

$d I_{DN}(lin) = d I_{Dp}(sat)$.

$$V_{IH} = \frac{V_{DD} + V_{TP} + \frac{k_n}{k_p}(V_{TN} + 2V_{out})}{1 + \frac{k_n}{k_p}}$$

from quadratic equations find V_{out}.

* for symmetric VTC.

1 - $k_n = k_p$

$\mu_n C_{ox} \left(\frac{W}{L}\right)_N = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$ → gate.

$580 \left(\frac{W}{L}\right)_N = 230 \left(\frac{W_p}{L_p}\right)$.

$$\boxed{\frac{W_p}{L_p} = 2.5 \frac{W_N}{L_N}}$$

2- $V_m - V_{IL} = V_{IH} - V_m$

3- $V_m = V_{DD}/2$

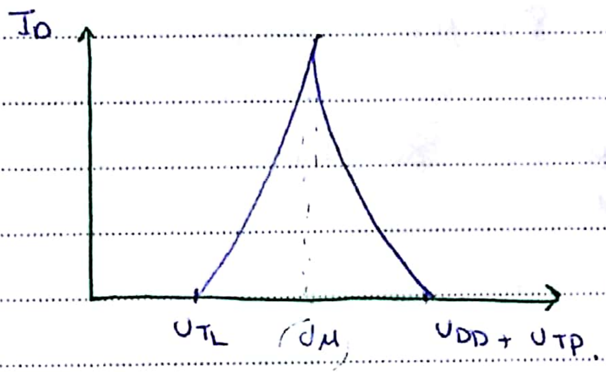
* $HNM = V_o(V_{IL}) - V_o(V_{IH})$

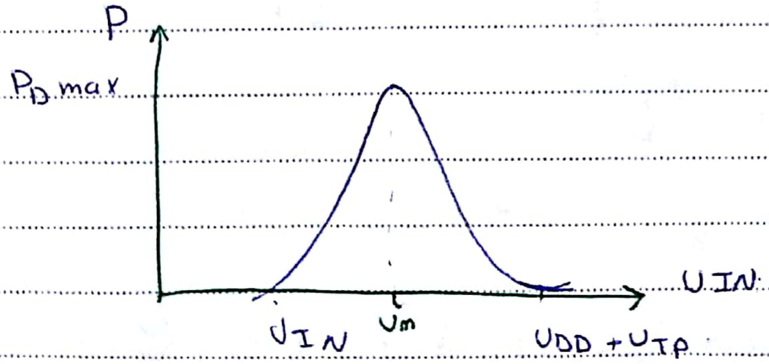
$LNM = V_{IL} - V_o(V_{IH})$

- 23.2 * Power Dissipation :-

$P_{static} = \text{Zero}$, $I_{DD}(OH) = 0$ (N-off), $I_{DD}(OL) = 0$ (P-off)

$P_{dynamic} = C \, \nu \, V_{DD}^2$





- Example

* Example 23.3, Design for Symmetry. $V_{DD} = 5$.

$k_n' = 40 \mu A/V^2$, $k_p' = 16 \mu A/V^2$, $V_{TN} = 1\,V$

$V_{TP} = -1$, $L_N = L_P = 2 \mu m$, $W_n = 4 \mu m$

$W_p = ?$, Check for symmetry. [$k_n = k_p$, $V_m = \frac{V_{DD}}{2}$

V_m — V_{IL} = V_{IH} — V_m

$$\frac{W_p}{L_p} = 2.5 \frac{W_n}{L_n}$$

$W_p = 2.5 * 4 \mu = 10 \mu m$

① $k_p = 16 \mu \times \frac{W_p}{L_p} = 80 \mu m$ ✓

$k_n = 40 \mu \times \frac{4 \mu}{2 \mu} = 80 \mu m$

$k_p = k_n$

② $$V_m = \frac{5 + (-1) + 1\sqrt{\frac{80}{80}}}{1 + \sqrt{\frac{80}{80}}} = 2.5$$

$V_m = \frac{V_{DD}}{2} = \frac{5}{2} = 2.5$.

③ $$V_{IL} = \frac{2 V_{out}(V_{IL}) - 5 + (-1) + \frac{80}{80}(1)}{1 + \frac{80}{80}}$$

$V_{IL} = V_o(V_{IL}) - 2.5$.

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$V_{out}(V_{IL}) = V_{IL} + 2.5$

$I_{DN}(sat) = I_{Dp}(lin)$

$$\frac{k_n}{2}\left((V_{IN_L} - V_{TN})\right)^2 = k_p\left((V_{DD} - V_{IN_L})V_{SD} - \frac{V_{SD}^2}{2}\right)$$

$V_{SD} = V_{DD} - V_{out}$

$V_{SD} = V_{DD} - V_{IL} - 2.5$

$$\frac{k_n}{2}\left(V_{IL} - V_{TN}\right)^2 = k_p\left((V_{DD} - V_{IL})(V_{DD} - V_{IL} - 2.5) - \frac{(V_{DD} - V_{IL} - 2.5)^2}{2}\right)$$

$V_{IL} = 2.125\,V$

$$\rightarrow V_{IH} = \frac{5 - 1 + \frac{80}{80}\left[1 + 2V_{out}(V_{IH})\right]}{1 + \frac{80}{80}}$$

$V_{out} = V_{IH} - 2.5$

$I_{D_N}(lin) = I_{Dp}(sat)$

$\downarrow$ $\quad\quad$ $\hookrightarrow V_{SG} = V_{DD} - V_{INH}$

$V_{GS} = V_{INH}$

$V_{DS} = V_{out} = V_{IH} - 2.5$

$V_{IH} = 2.875$

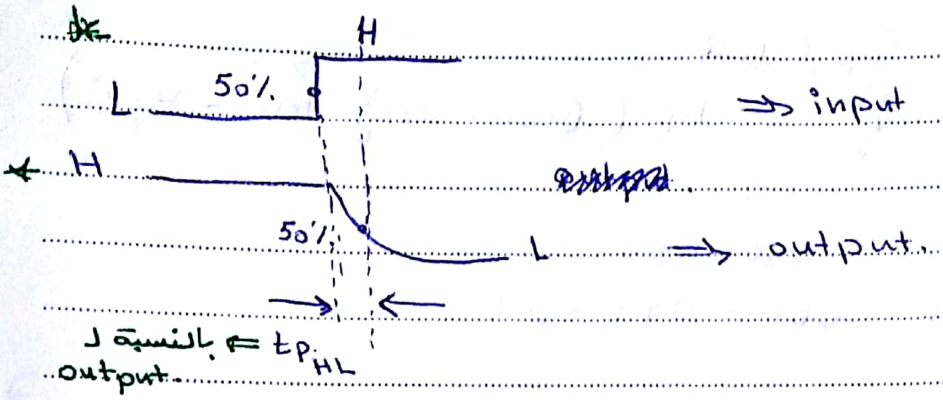
$V_m - V_{IL} = V_{IH} - V_m$

$2.5 - 2.125 = 2.875 - 2.5$

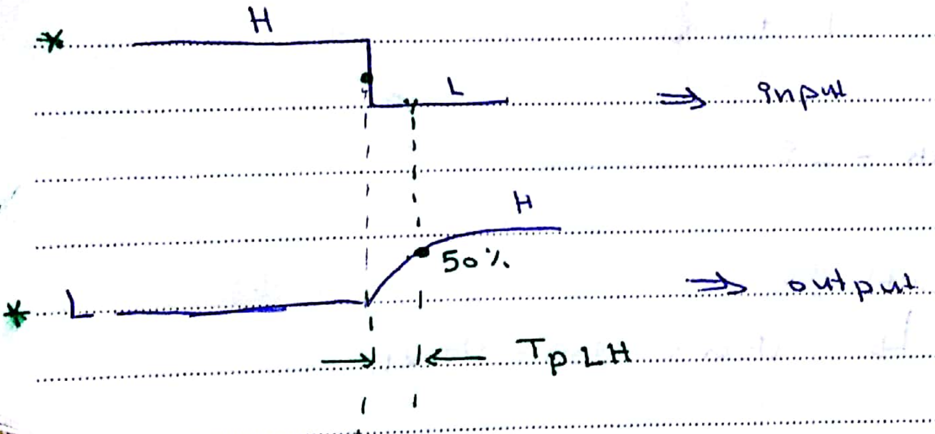
$0.375 = 0.375$ ✓

23.9 Fan-out (capacitance that a reasonable delay time).

Input. propagation delay.



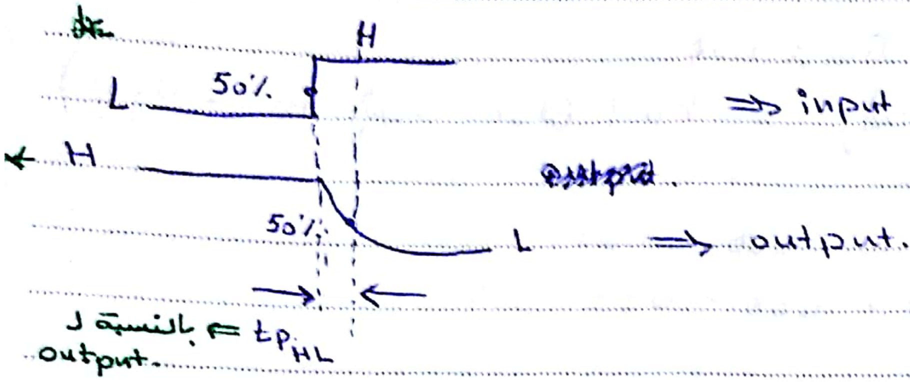
- tpHL = time delay between input increasing from Low to 50% of max, and output droping from max to 50% of max.



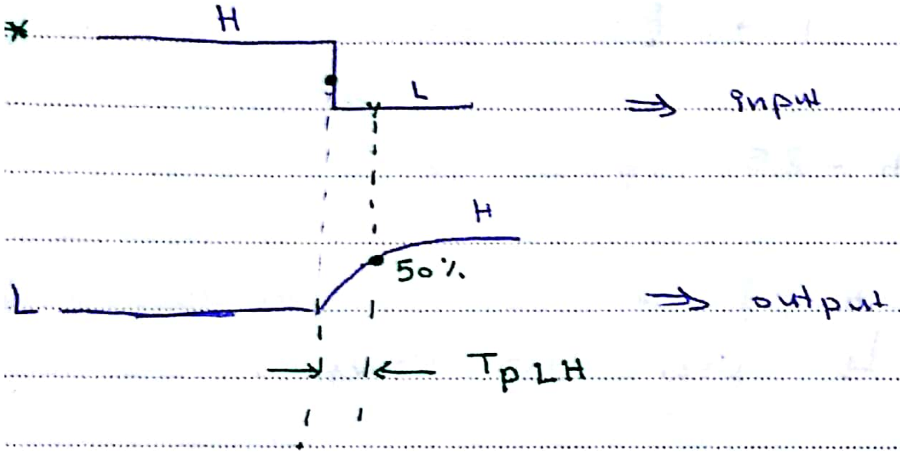
23.9 Fan-out (capacitance that a reasonable delay time).

propagation delay.

Input.



— tpHL = time delay, between input increasing from Low to 50% of max, and output droping from max to 50% of max.



$$t_{pHL} = \left[\frac{2V_{TN}}{K_n(V_{DD}-V_{TN})^2} + \frac{\ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)}{K_n(V_{DD}-V_{TN})}\right] C_L$$

$$= \left[\frac{2V_{TN}}{K_n(V_{DD}-V_{TN})^2} + \frac{1}{K_n(V_{DD}-V_{TN})} \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right] C_L$$

(1)

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$$t_{pLH} = \left[\frac{-2 V_{TP}}{k_p (V_{DD} + V_{TP})^2} + \frac{1}{k_p (V_{DD} + V_{TP})} \ln \left(\frac{1.5 V_{DD} + 2 V_{TP}}{0.5 V_{DD}} \right) \right] C_L$$

(2)

→ Find C_L, and $\frac{C_L}{K_n}$

* Fan - out if VTC symmetric.

- For a signal capacitance

$$C_{IN} = (W_n L_N + W_p L_p) C_{ox}$$ → ignor

in general for Load or driver.

Fan - out F : $F = \frac{C_L}{C_{IN}}$

لم يعلم

1- For symmetry $\frac{W_p}{L_p} = 2.5 \frac{W_n}{L_N}$ → $L_N = L_p$.

$$C_{IN} = (W_N L_N + 2.5 W_N L_N) C_{ox}$$
$$= 3.5 W_n L_N C_{ox}$$

2- $k_p = W_n = \frac{W_n}{L_N} \mu_n C_{ox}$

$$\frac{C_L}{K_n} = \frac{F C_{IN}}{\frac{W_n}{L_N} \mu_n C_{ox}} = \frac{F (3.5 W_n L_N C_{ox})}{\frac{W_n}{L_N} \mu_n C_{ox}}$$

Subject: 120

$$\frac{C_L}{k_n} = \frac{3.5\, L_N^2\, F\, C_{ox}'}{\mu_n\, C_{ox}'} \quad \text{---- from eqn (1)}$$

$$= \frac{3.5\, L_N^2\, F}{\mu_n}$$

$$F = \frac{C_L}{k_n}\,\frac{\mu_n}{3.5\, L_N^2}$$

$$F = \frac{\mu_n}{3.5\, L_N^2\left[\frac{2\,V_{TN}}{(V_{DD} - V_{TN})^2} + \frac{1}{V_{DD} - V_{TN}}\ln\left[\frac{1.5\,V_{DD} - 2\,V_{TN}}{0.5\,V_{DD}}\right]\right]}$$

لسه ليس للحفظ

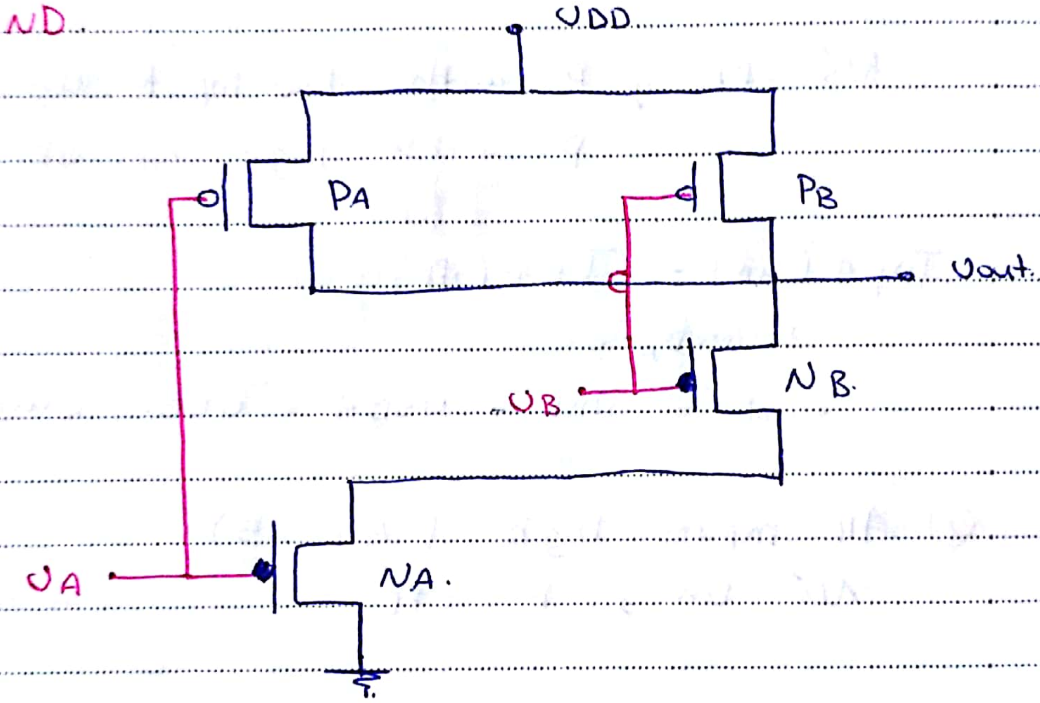
- Example 23.10 (read)

Subject: 121 Final.

* Chapter 24 CMos Gate.

24.2,3,4 NAND, NoR, AND, oR Gates.

* NAND.



A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

(1) Any input Low, N are off, P lin.

1.a A Low, B Low ($V_{IN} = 0$).

2 I_{Dp} (Lin) = I_{DN} (off) = 0.

↓ $V_{SD} = 0$.

$V_{out} = V_{DD} - V_{DS} = V_{DD}$ (high).

- Any input Low
A Low , B high (or vice vera).

N's off , P with Low input lin.
P with high " off .

$I_{DPA}(lin) = I_{DN}(off) = 0$.
↘ $V_{SDA} = 0$.
$V_{out} = V_{DD} - V_{SDA} = V_{DD}$. (high).

② All inputs high ($V_{IN} = 5$).
N's lin , P off.

$I_{DN}(lin) = I_{DP}(off) = 0$.
$V_{DS} = 0$. , $V_{out} = V_{DS} = 0$ (Low)

* For Symmetry :-
For a single input inverter $\frac{W_P}{L_P} = 2.5\, W_n/L_n$.

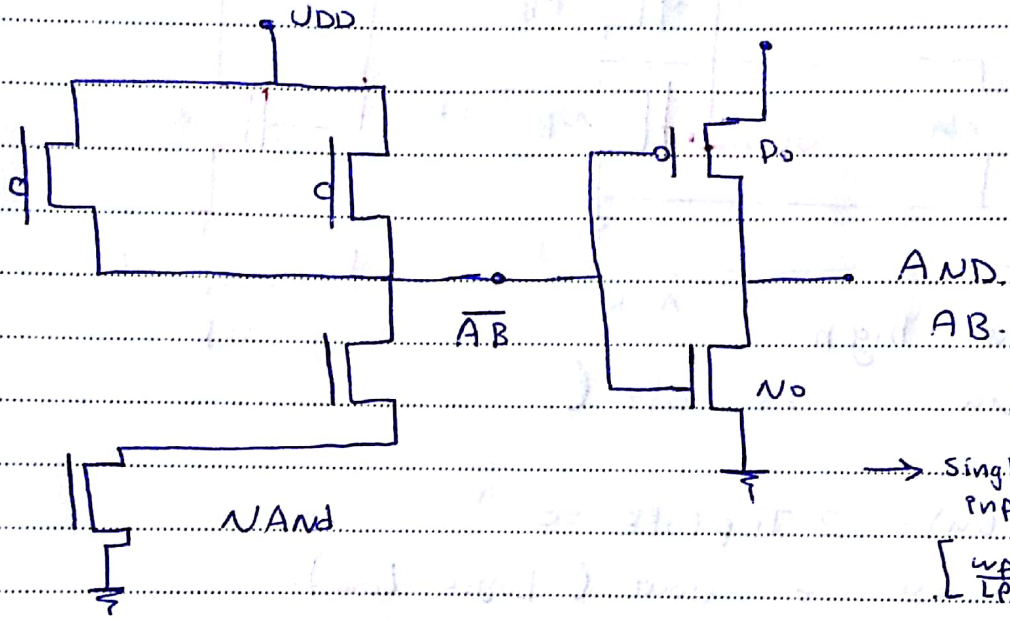
For a two input $= \frac{2W_P}{L_P} = 2.5\, W_n/L_n$.

$I_{DP} = I_{DN}$ تم اثباتها سابقاً

* In General: For an i-input NAND Gate.

$$i \frac{W_P}{L_P} = 2.5 \frac{W_n}{L_N}$$

* AND Gate.

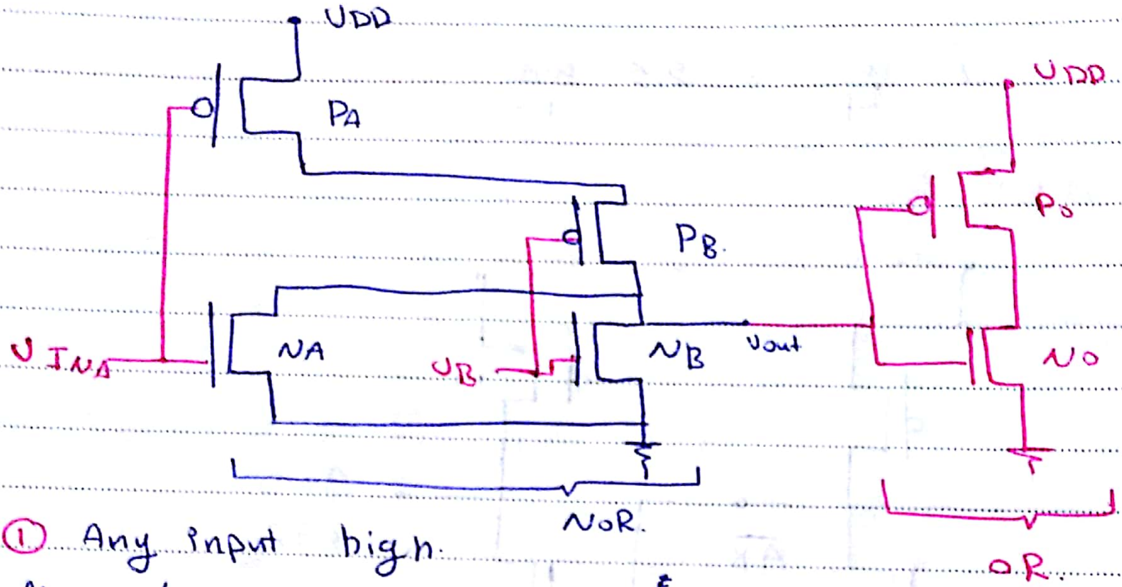


→ Single input ⇐ inverter هاد

بطبق قانون $\left[\frac{W_P}{L_P} = 2.5 W_n L_n\right]$

- add an inverter at the output of the NAND Gate.

– OR Gate :- + NoR Gate.



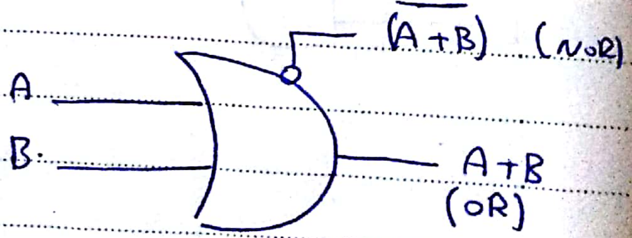
① Any input high.
Corresponding N's lin, P's off.

$I_{DN}(lin) = 2\, I_{DP}(off) = 0$.

$V_{DS} = 0 = V_{out}$ (Logic Low).

② All input Low.
N's off, ~~corresponding~~ P is lin.
$I_{DN}(off) = I_{DP}(lin) \Rightarrow V_{SD} = 0$.
$V_{out} = V_{DD}$ (Logic high).

A	B	NoR
0	0	1
0	1	0
1	0	0
1	1	0



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/ 2/

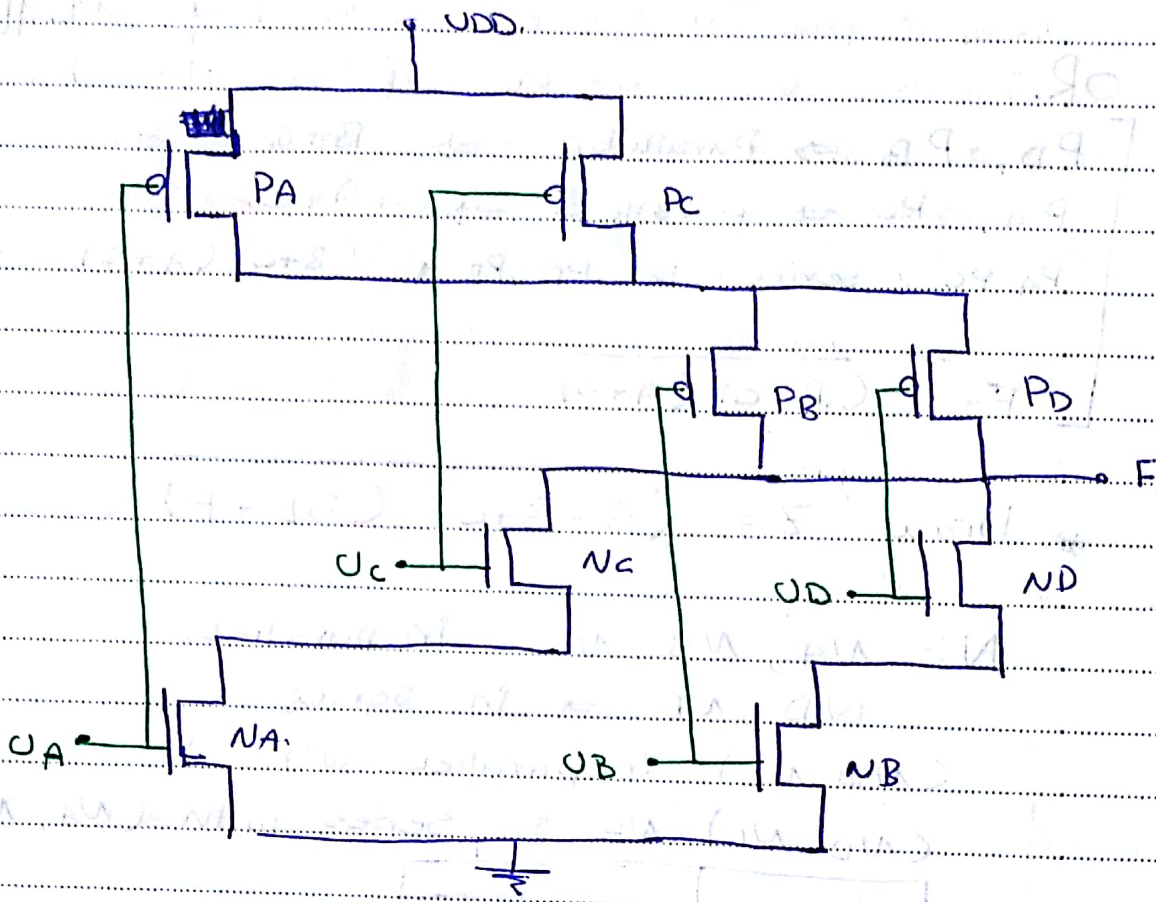
* For Symmetry

$$\frac{W_P}{L_P} = \left(2.5 \frac{W_N}{L_N}\right) * 2$$ (For two-input).

For i-input $\rightarrow$ $\frac{W_P}{L_P} = i \left[2.5 \frac{W_N}{L_N}\right]$.

S T A R S

* 24.5 AND-OR - Inverter Logic Function (AoI).



Enough to look at Pull down (or pull-up) cct. * N's in series → ANDing.
* P's in parallel → ORing.

- (For PMOS the opposite).
ND, NB in series → BD
NC, NA " " → CA
ND, NB is in parallel with (NC, NA)
= BD + CA

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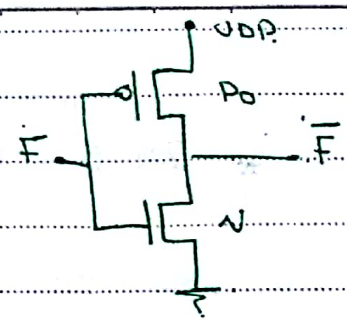
$F = \overline{BD + CA}$, $\overline{F} = BD + CA$



OR.

$P_D, P_B \Rightarrow$ Parallel. $\Rightarrow$ $B+C$

$P_A, P_C \Rightarrow$ parallel $\Rightarrow$ $A+C$

$P_A\ P_C$ series in $P_D, P_B \rightarrow$ $(B+C)(A+C)$.

$F = \overline{(B+C)(A+C)}$

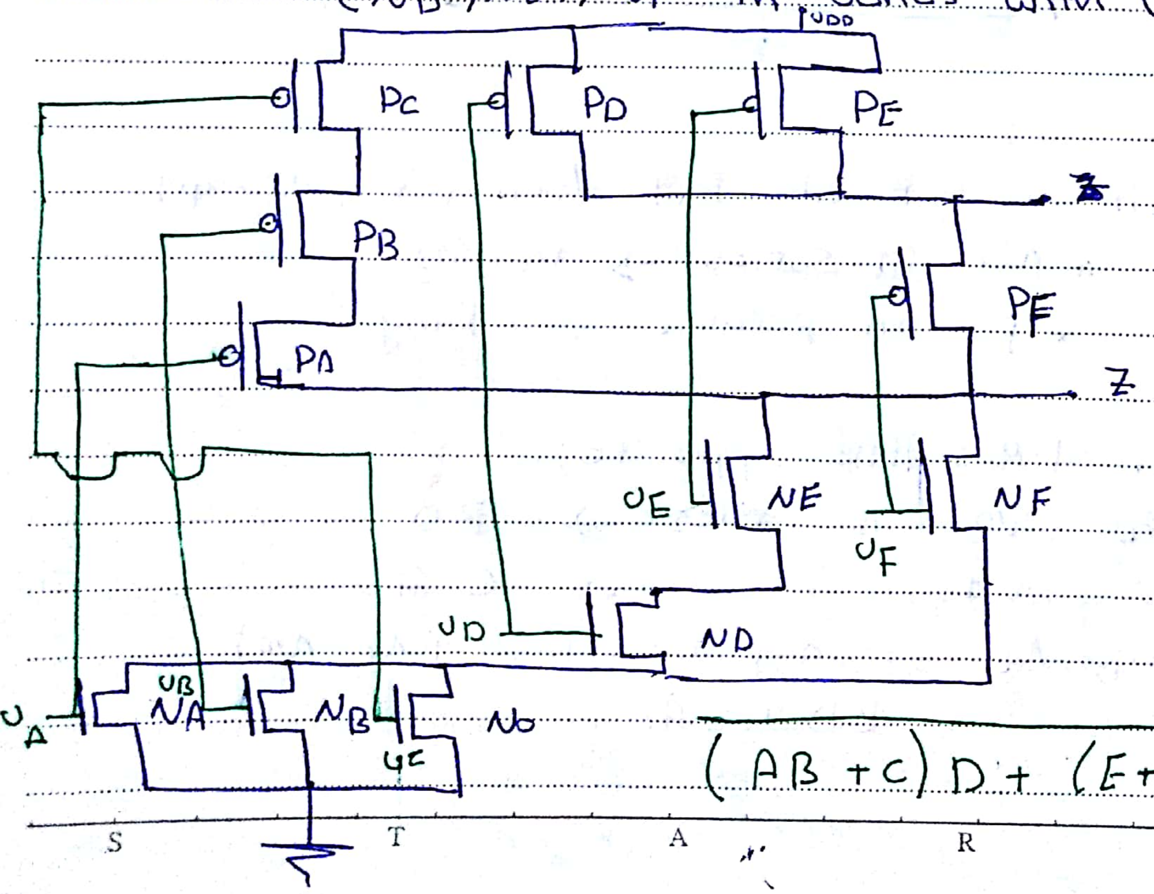
* Draw $Z = \overline{(A+B+C)(DE+F)}$

N :- NA, NB, NC in parallel.

ND, NE $\Rightarrow$ in series.

(ND, NE) in parallel with F.

(ND, NE), NF in Series with (NA, NB, NC).



$\overline{(AB+C)D + (E+F)(G+H)}$

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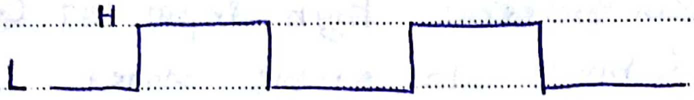
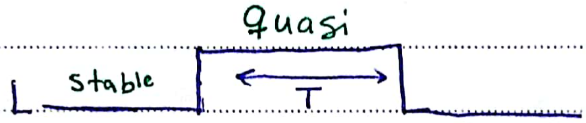
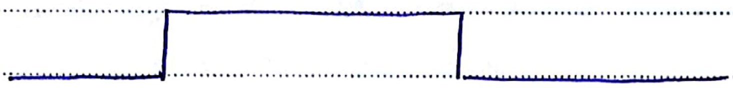
* Multivibrators (Neamen) ch 15

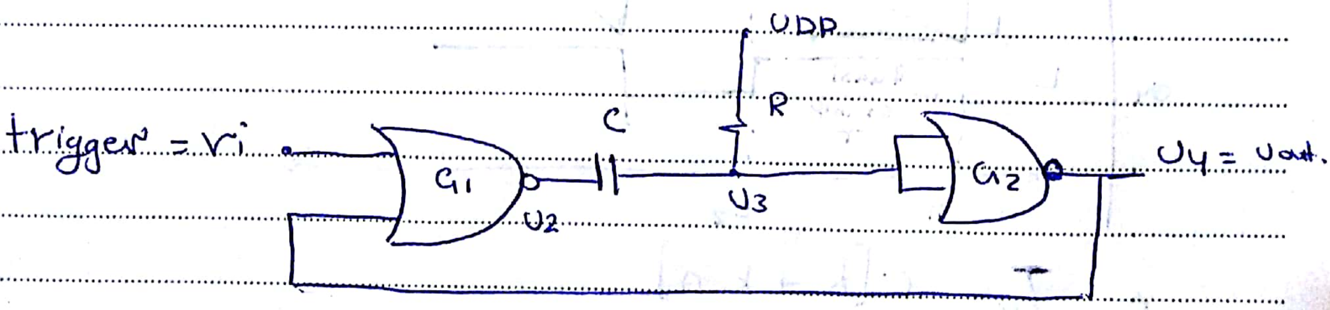
1. Astable :- trigged one with no stable state
2. Mono stable :- Has one stable state and moves to
3. ~~Bistable~~ the other state (quasi - stable) when trigged and remains in the quasi-stable state For a predetermined time.







3. Bistable (flip - flop), Two stable States, switches between them only when trigged.



① t < to.

Inital state vc = 0 , v2 at Logic High vy high
vy (out) Low , v2 still high
vout Low (stable state).

2 _ $t_0 < t < t_1$

Apply trigger at (at t_0) , V_2 Low , $U_C = 0$

$U_3 = 0$, U_4 high , (output quasi)

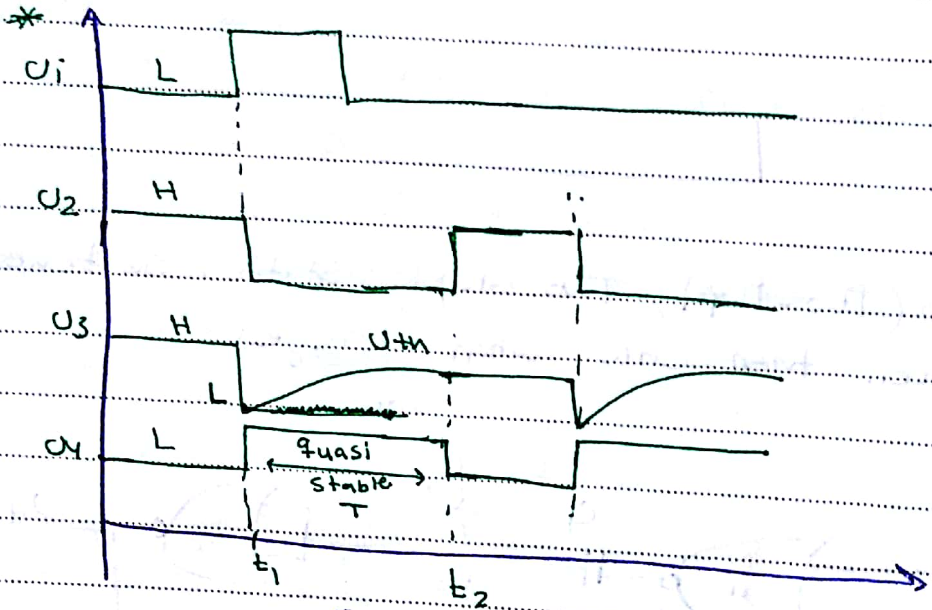
But capacitor starts charging through R

(U_C and U_3 increases ~~until~~ keeps inc until

$U_3 = U_{Th}$, considered high input at G_2)

⟹ U_4 Low (back to stable state)

and U_2 back to high also U_3 at high.



$T = C[R + R_{on}]$

↳ Resistance of gates and very small

$T = t_2 - t_1 = C(R + R_{on}) \ln\left(\frac{R}{R + R_{on}} \cdot \frac{U_{DD}}{U_{DD} - U_{th}}\right)$

قيمة الحل

* if $R >> R_{on}$, $U_{Th} = \frac{1}{2} U_{DD}$

$$T = RC \ln 2 = 0.7\, RC$$

$$U_C = U_i + (U_t - U_i)\left(1 - e^{-t/RC}\right)$$

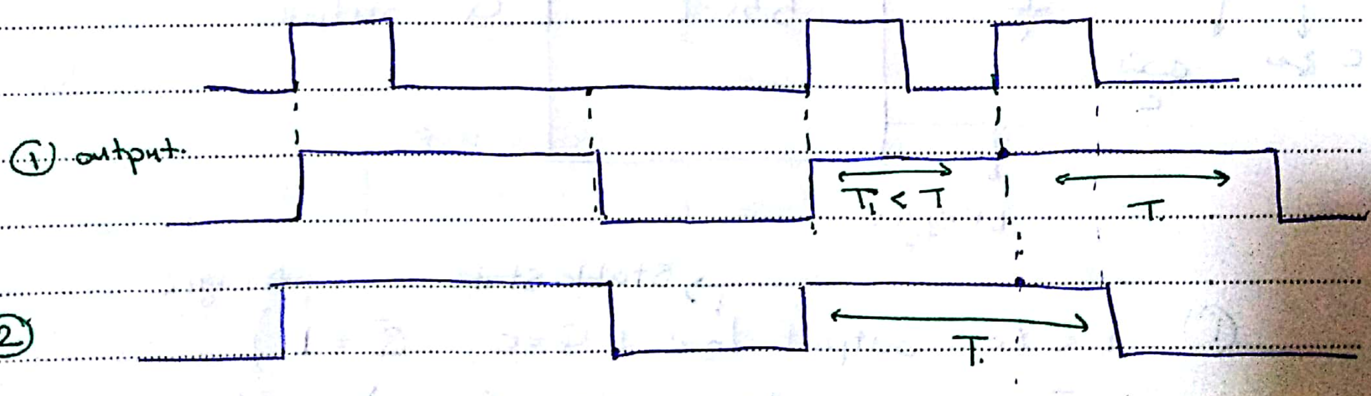
(U_C → U_{th}, $U_i = 0$, t → T; U_t ↳ target voltage U_{DD})

* Two types of mono stable Response :-

① Retriggable, ② no retriggable.

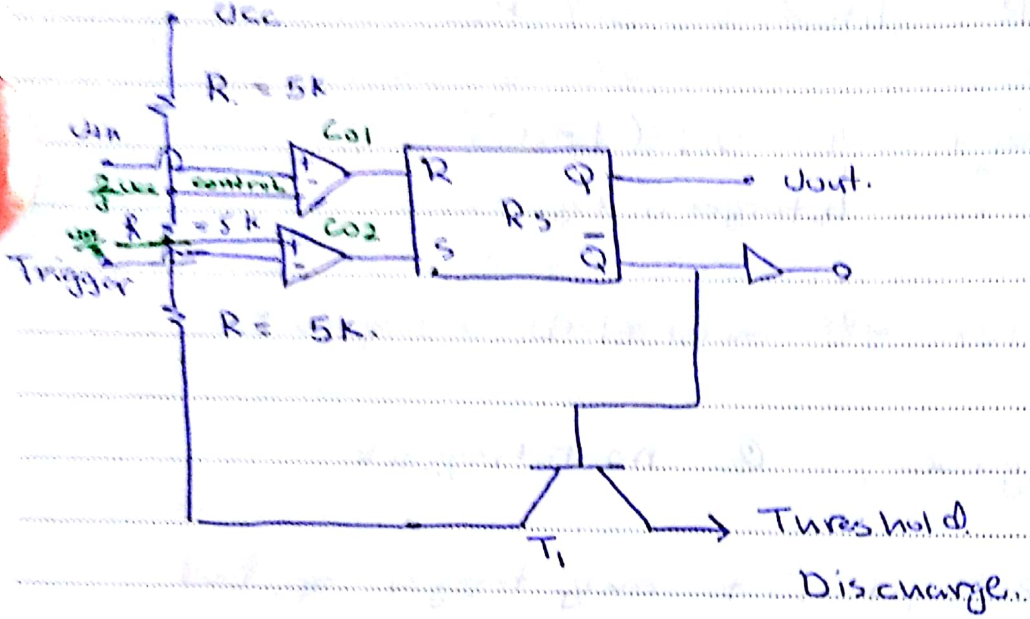
* Retriggable :- responds to any trigger applied even if in quasistable state.

* No retriggable :- does not respond to a new trigger if in quasistable state.

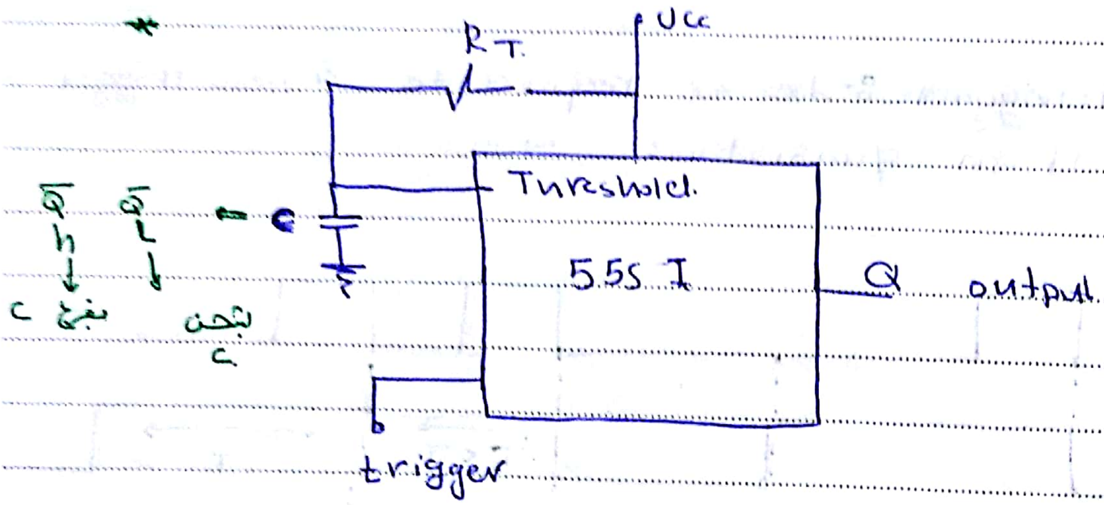


* 555 Ic timer:-

Mono stable Multivibrator



*



① $t < t_o$ output Low ($Q = 0$, $\bar{Q} = 1$), → Stable state → Logic

T_1 on, discharge C_T → $V_C = 0$

② Trigger is applied at $t = t_1$

$v_i < \frac{Vcc}{3}$, out of Co_2 is high

$(S = 1)$, $Q = 1$, $\bar{Q} = 0$. (T_1 = off).

Vout = high (quasi-stable)

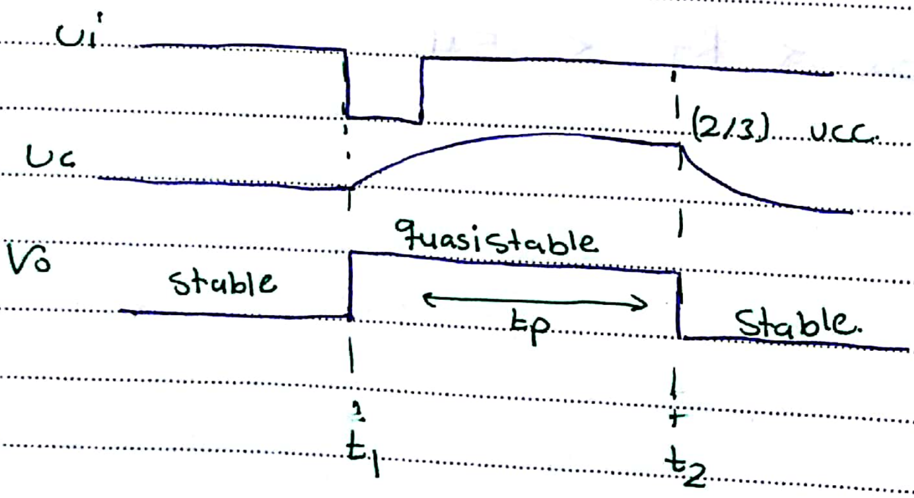
$T_1 \Rightarrow$ off (capacitor charges through R_T ~~capacitor charges~~ ~~[illegible]~~

③ cap charges until $Vc = \frac{2}{3} Vcc = V_{th}$

$\Rightarrow$ Co_1 is on and Reset flip flop.

$Q = 0$ (out put back to stable state)

$\bar{Q} = 1$ (T_1, on, cap dis charges again).



ex* $V_{cc} = 5$, $V_{th} = \frac{2}{3} * 5 = 3.33\,V$

$V_c = V_F + (V_i - V_F)\, e^{-t/RC}$

$3.3 = 5 + (0 - 5)\, e^{-t_p / R_T C_T}$

$t_p = 1.1\, R_T C_T$

* Example 8- Find min and maxium values of R_T if $350n < I_T < 10\,mA$

$I_{T\,max} = \frac{V_{RT\,max}}{R_{T\,min}} = \frac{5 - 0}{R_{T\,min}} = 10m$

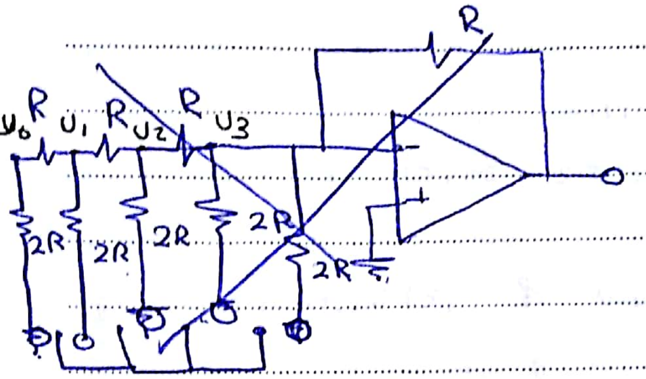
$R_{T\,min} = 500\,\Omega$

$R_{T\,max} = \frac{V_{RT\,min}}{I_{T\,min}} = \frac{5 - 3.3}{350n} = 5\,M\Omega$

$500 < R_T < 5M$

Subject: .... Sec 9 / /

* Digital to analog converter
  R/2R Ladder Conv.



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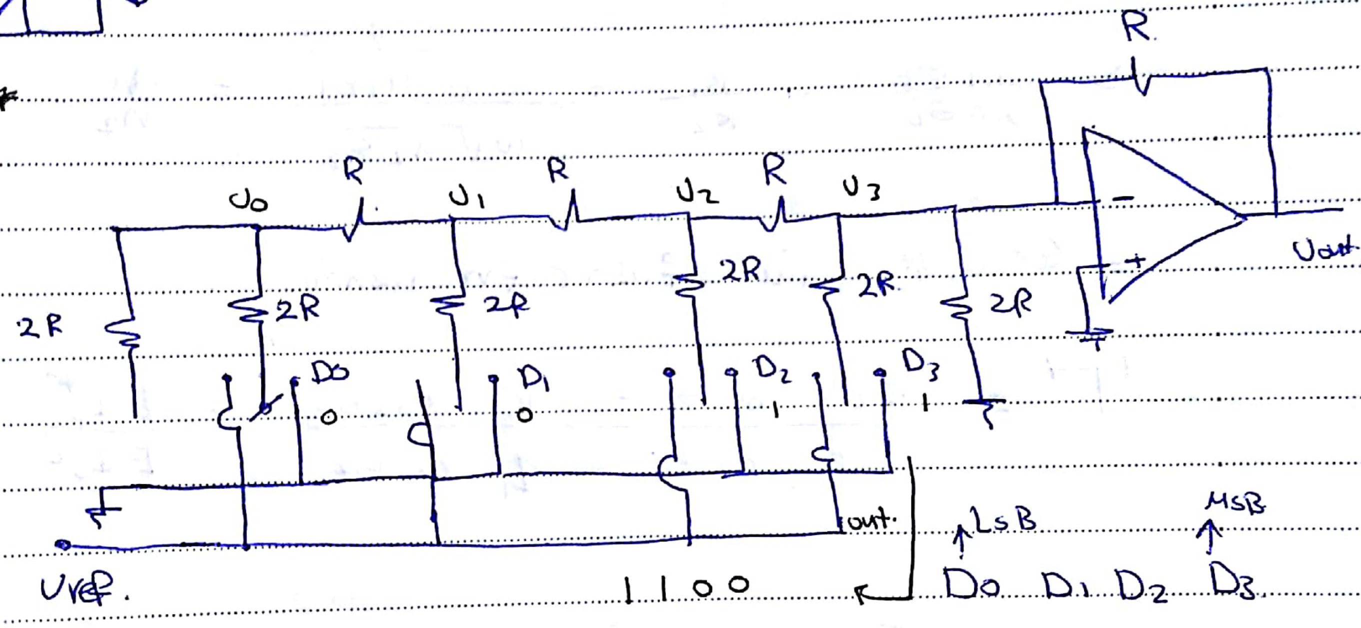

_For a certain node

* if Digital input to the left of that node is at Logic 0 (Grd), then said node sees an equivalent Resistance of 2R.

N: Number of bits

كل ما دقة عدد الابيتة تزيد R و 2R ،

Subject: /   /

$$V_{out} = \frac{V_{ref}}{2}\left(D_{N-1} + \frac{D_{N-2}}{2} + \cdots + \frac{D_1}{2^{N-2}} + \frac{D_0}{2^{N-1}}\right)$$

→ $N = 4$, $\overset{D_0 D_1 D_2 D_3}{0\,0\,1\,1}$

$$V_{out} = \frac{V_{ref}}{2}\left(\frac{D_3}{2^0} + \frac{D_2}{2^1} + \frac{D_1}{2^2} + \frac{D_0}{2^3}\right)$$

* بيحوطو مكان D_3 ← قيمتها 1

— if digital input is given in decimal.

$$V_{out} = \frac{n}{2^N} V_{ref}.$$ (مهمة).

— Example. Find V_{out} for inputs with each bit at Logic 1 one at a time. , $V_{ref} = 5$.

D_3	D_2	D_1	D_0	V_{out}
1	0	0	0.	$V_{out} = \frac{V_{ref}}{2}(1) = 2.5V$
0	1	0	0	$V_{out} = \frac{V_{ref}}{2}\left(\frac{1}{2}\right) = 1.25$
0	0	1	0	$= \frac{V_{ref}}{2}\left[\frac{1}{4}\right] = 0.625$
0	0	0	1	$= \frac{5}{2}\left[\frac{1}{8}\right] = 0.312.$

لازم نحسبهم في 5 إلي هو V_{ref} ، عند أنو 1111

$$V_{out} = \frac{5}{2}\left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right] = 4.68V$$

→ D_3 D_2 D_1 D_0
1 1 1 1

لما لانه 0000 ما أخذناها. لسا حنطلع أقل من 5.

Subject:......................

The sum of these voltage is 4.681 < 5, because we have $2^N = 2^4 = 16$ Level, but we only cannot $(2^4-1) = 15$.

Level $\frac{5}{16} = 0.315$ V.

$\frac{V_{ref}}{n} = \frac{5}{16} = 0.315$

n → number of Levels

$\frac{5}{16} \times 15 = 4.68$ V.

$\uparrow 5 = \frac{16}{15} \times 4.68 \uparrow$

achieve an output of 5 V increase. Vref.

$V_{ref} = \frac{16}{15} \times 5 = 5.33$ V.

- in general, for a max output

$V_{ref} = \frac{\text{\# of level}}{\text{\# of cocuts}} \times V_{o\,max}$.

* Resolution:- Least detected increment in input voltage that can be masured by the D/A convert

$Res = \frac{V_{ref}}{2^N - 1}$,

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Subject: / /

accuracy = $\frac{Res.}{Vref} = \frac{1}{2^N - 1}$

* Example: Design a 6-bit R/2R Ladder DA. if $R_F = R$.

1- Find the analog output to (10 1010)

$(101010)_2 \Rightarrow (42)_{10}$

$V_{out} = \frac{n}{2^N} V_{ref} = \frac{42 * 5}{64} =$

$= 3.28.$

b- $V_{out} = 2.2V$, find digital input.

$n = \frac{V_{out}}{V_{ref}} \times 2^N = \left(\frac{2.2}{5}\right) \times 64 = (28)_{10}$

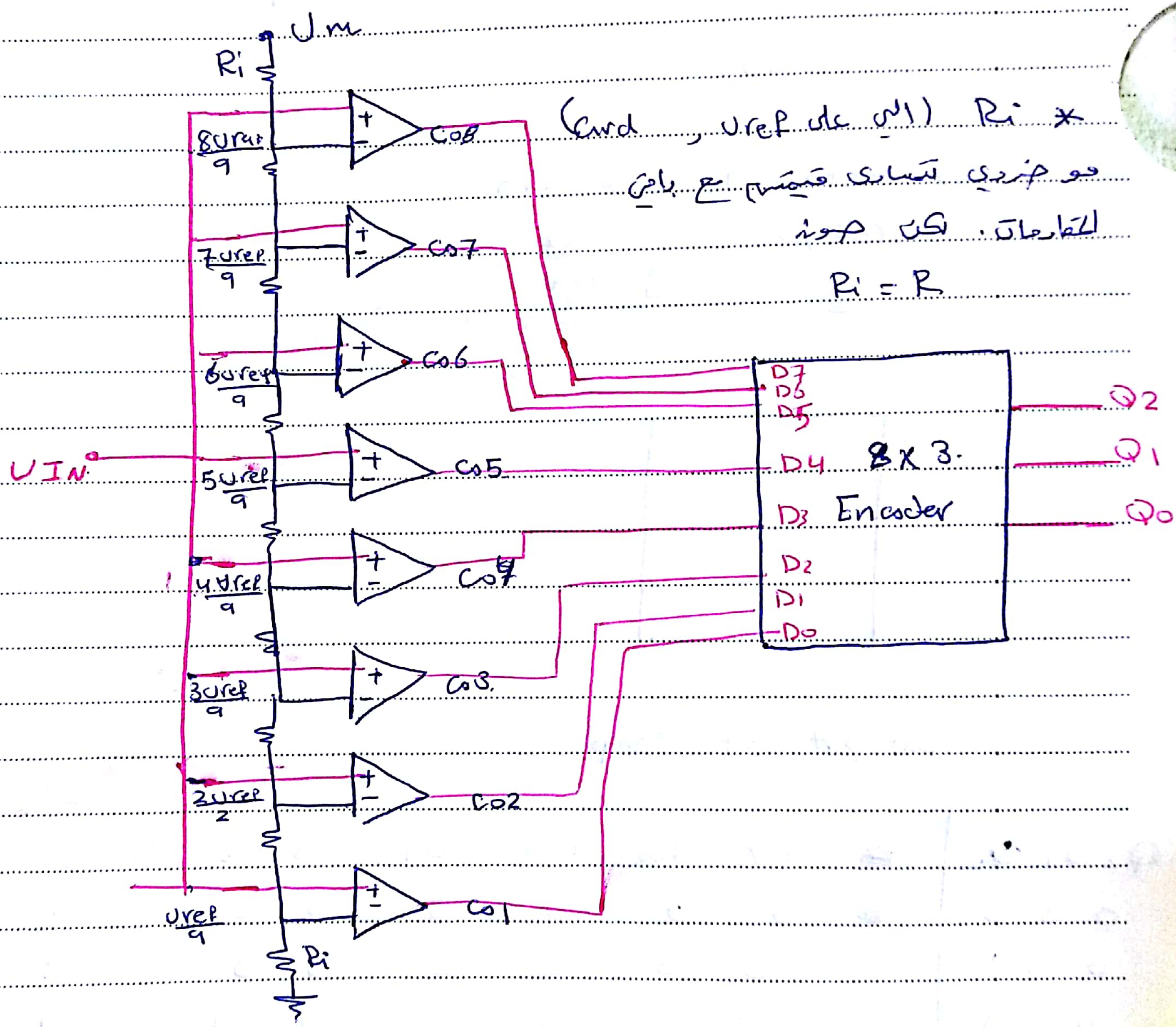
$(28)_{10} = 011100.$

* Analog to Digital Converter

Binary-Encoded A/D conv

* Ri (اللي على Vref , Gnd) هو جزئي تساوي قيمتهم مع باقي المقاومات. لكن هو ز

$R_i = R$



$V_{IN} > \frac{V_{ref}}{9}$, $V_{IN} < \frac{2V_{ref}}{9}$

only Co1 has high output rest Low o/p.

Subject: ....

0000 0000 1.

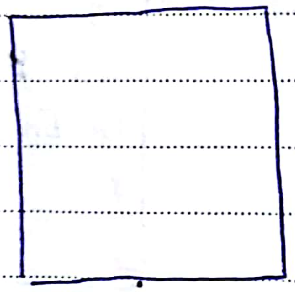
if $V_{IN} > \frac{2V_{ref}}{9}$, $V_{IN} < \frac{3V_{ref}}{9}$

0000 0011

* Comparato numbew = m.

$V_{ref}/m = \frac{m \; V_{ref}}{\boxed{N}+1}$

1 عدد ← (m) ; N → # of bit



out put of Comp.

$Q_2 Q_1 Q_0$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0 0 0	0	0	0	0	0	0	0	1
0 0 1	0	0	0	0	0	0	1	1
0 1 0	0	0	0	0	0	1	1	1
0 1 1	0	0	0	0	1	1	1	1
1 0 0	0	0	0	1	1	1	1	1
1 0 1	0	0	1	1	1	1	1	1
1 1 0	0	1	1	1	1	1	1	1
1 1 1	1	1	1	1	1	1	1	1

Subject: .... / /

Ex :- $\frac{3V_{ref}}{R} = 3$ $\frac{2V_{ref}}{R} = 2$

$V_{in} = 2.5$

high ⇐ on ⟵ C_{o1} , C_{o2} يعني

0 0 0 0 0 0 0 1 1

output 0 1 0.

* $Q_0 = D_1 + D_3 + D_5 + D_7$
$Q_1 = D_2 + D_3 + D_6 + D_7$
$Q_2 = D_4 + D_5 + D_6 + D_7$

اذا تغير رسمة تغير معادلات

Ex :- m = 5

$Q_0 = 0$ ($D_5 + D_7$ قيمة Bit يتجاهل).

$Q_1 = 0$

$Q_2 = 1$.

⇒ 1 0 0.

* $Res = \frac{V_{ref}}{N+1}$, $Acc = \frac{Res}{V_{ref}}$

* Example:- find the range of analog
a) inputs that correspon to binary number (000 11 111)

$V_{in, min} \geq V_{ref, 5} = \frac{5 V_{ref}}{9}$
$= 2.78.$

$V_{in, max} < V_{ref, 6} = \frac{6 V_{ref}}{9} = 3.33$ V.

Subject:...................... / /

b) find the resolution = $\frac{5}{9}$ = 0.56 V   حلك

c) find binary o/p if VIN = 1 V.

$V_{IN} = 1V > \frac{m\ V_{ref}}{N+1}$

$V_{IN} = 1 < \frac{V_{ref}}{9}(m+1)$.

$V_{IN} = 1 > \frac{m\ 5}{9}$ $\Rightarrow m < 1.8$

$1 < \frac{(m+1)\ 5}{9}$ > 0.8.

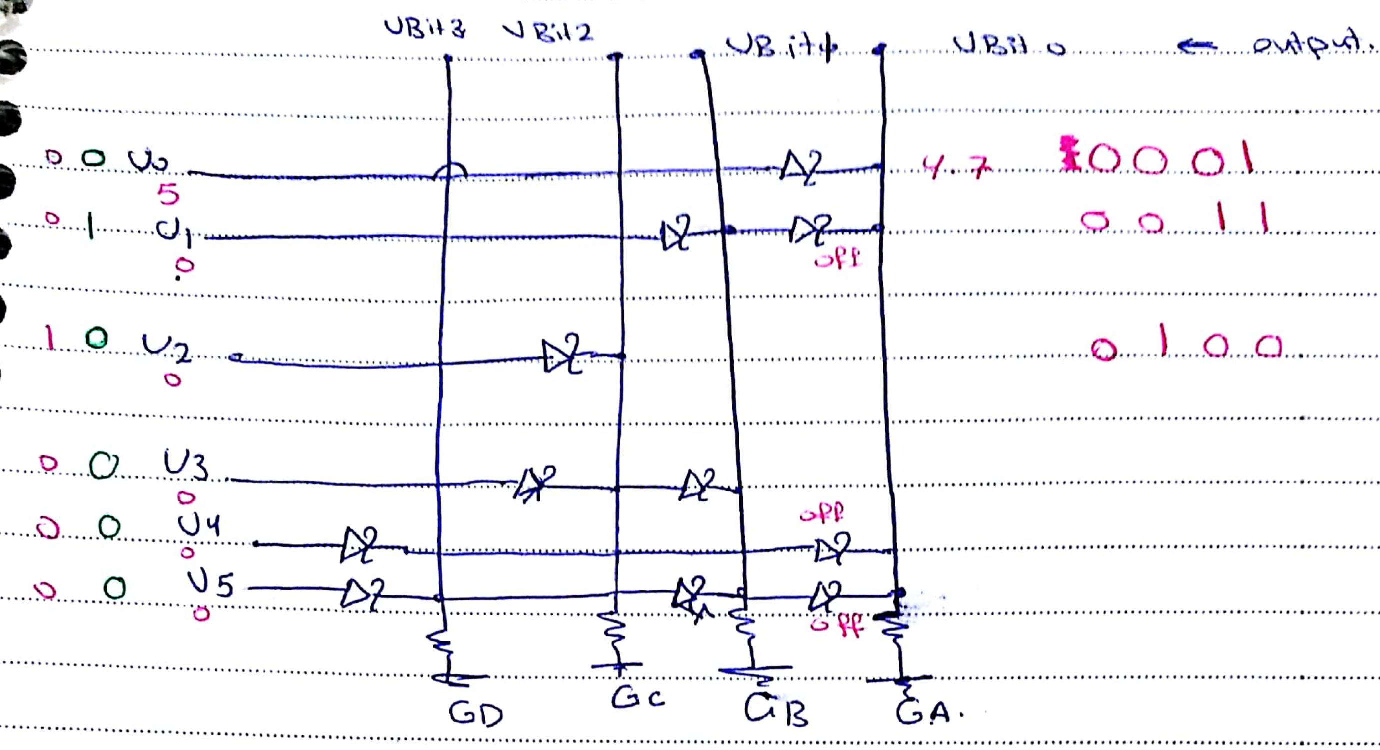
$\therefore m = 1$ $\Rightarrow$ only o/p at C_{o1} is high, others are Low.

0000 0001.

Encoded o/p $\Rightarrow$ 0 0 0.

* Chapter 32.1, 32.2 Diode and BJT (Read-only memory) RoM. (oR Gates)

Subject:........................ / /



GA :- UBit0 = U0 + U1 + U4 + U5.

if U0 = 1 and Rest 0.

UBit0 = 1

GB. ← UBit1 = 0

UBit2 = 0

UBit3 = 0.

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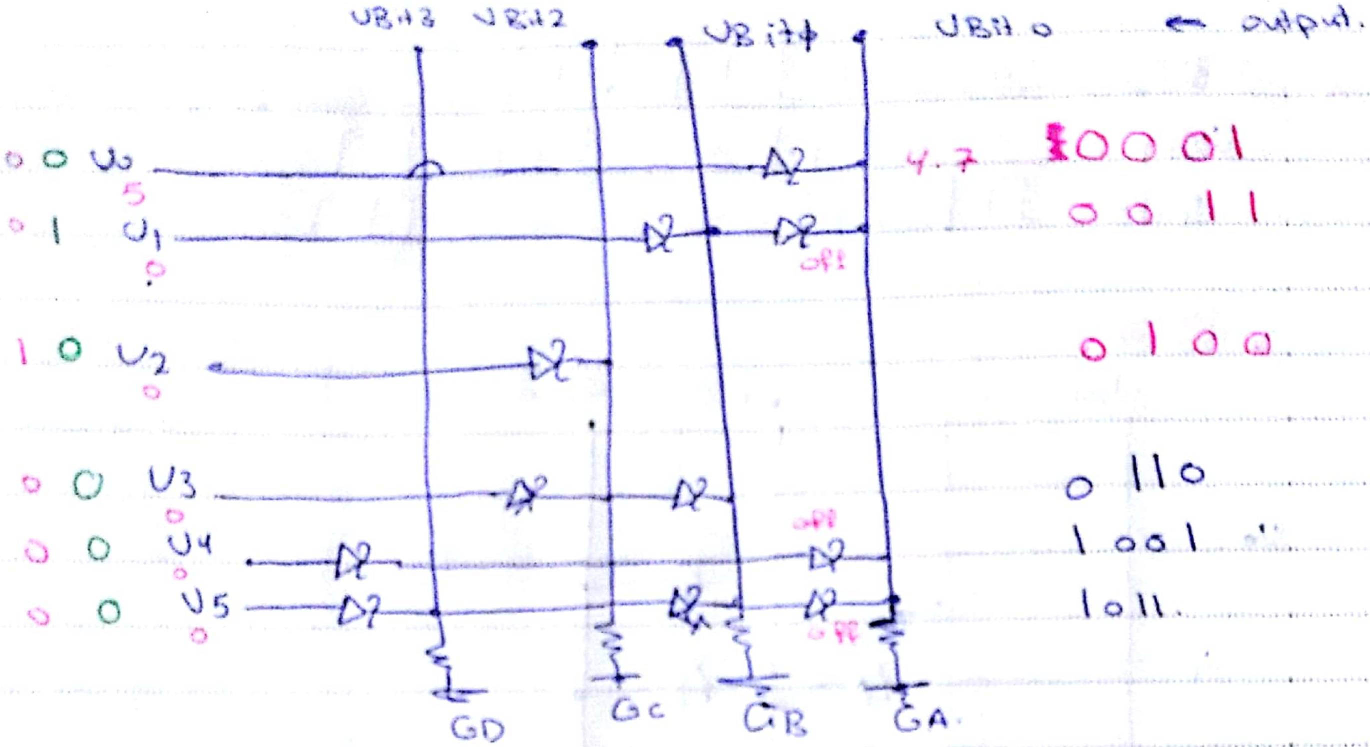


GA :- $UBit_0 = U_0 + U_1 + U_4 + U_5$.

if $U_0 = 1$ and Rest 0.

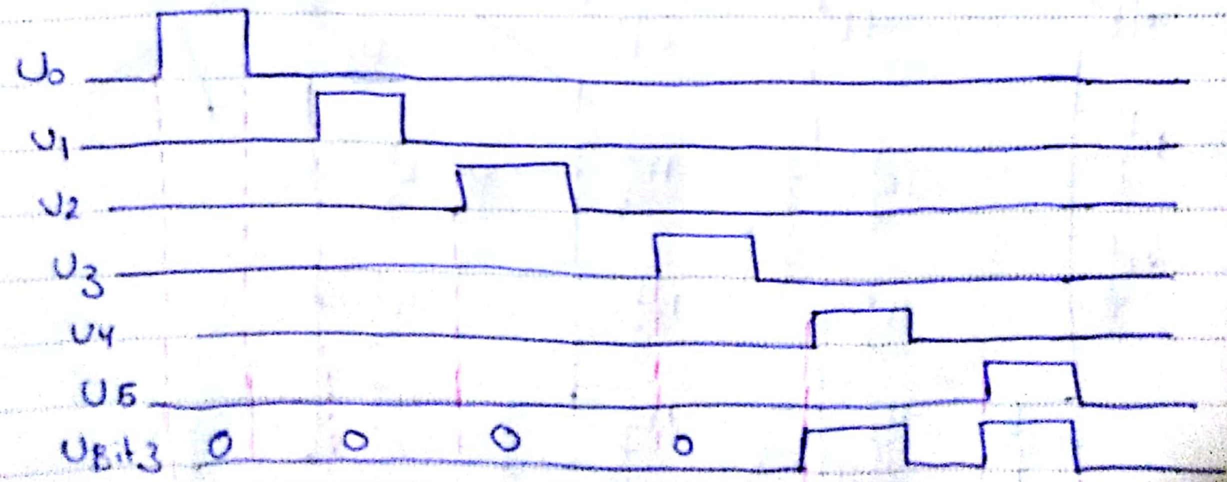
$UBit_0 = 1$

GB ← $UBit_1 = 0$

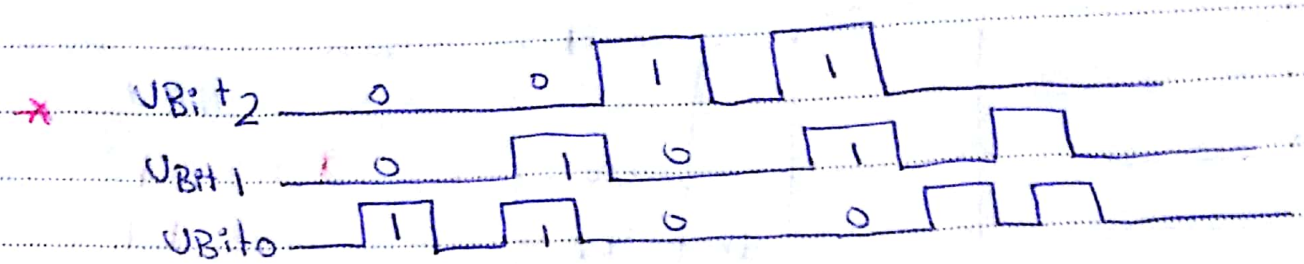
$UBit_2 = 0$

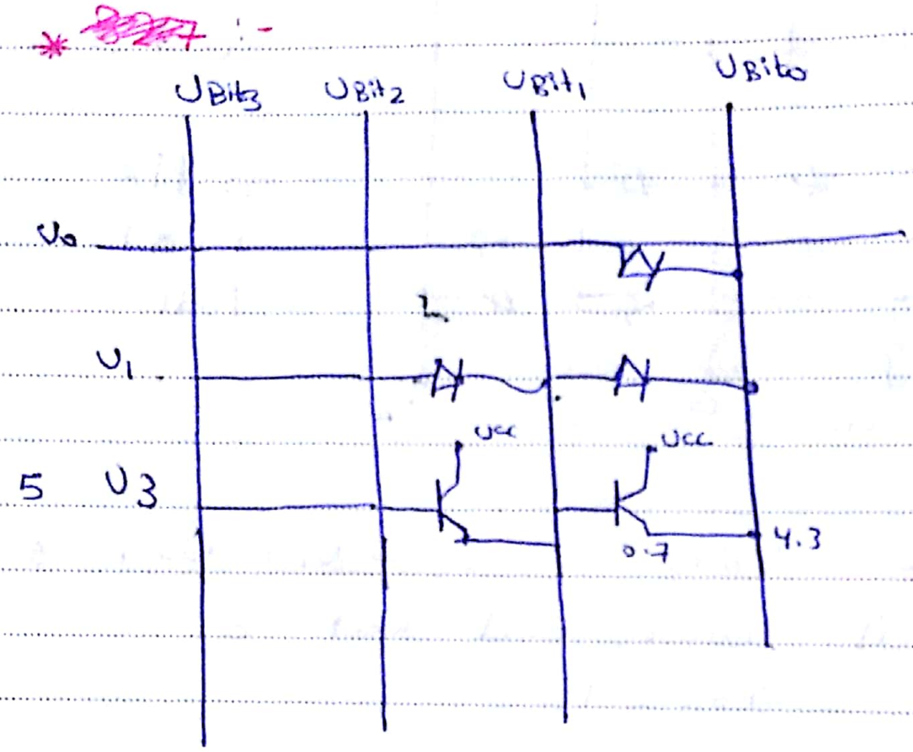
$UBit_3 = 0$.

* ممكن يجي السؤال كله دايود، واشتغل على مابدي ياه.

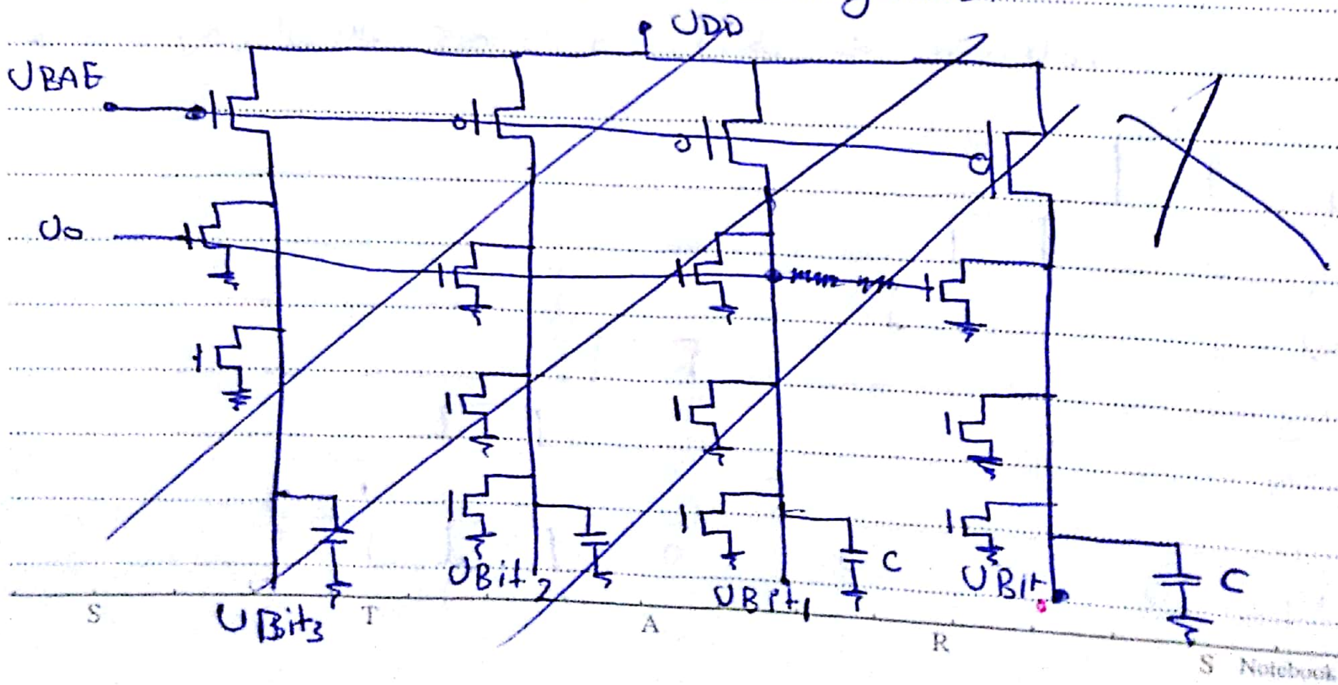


Subject: 143





* 32.7 CMos (REAl) only MEM.



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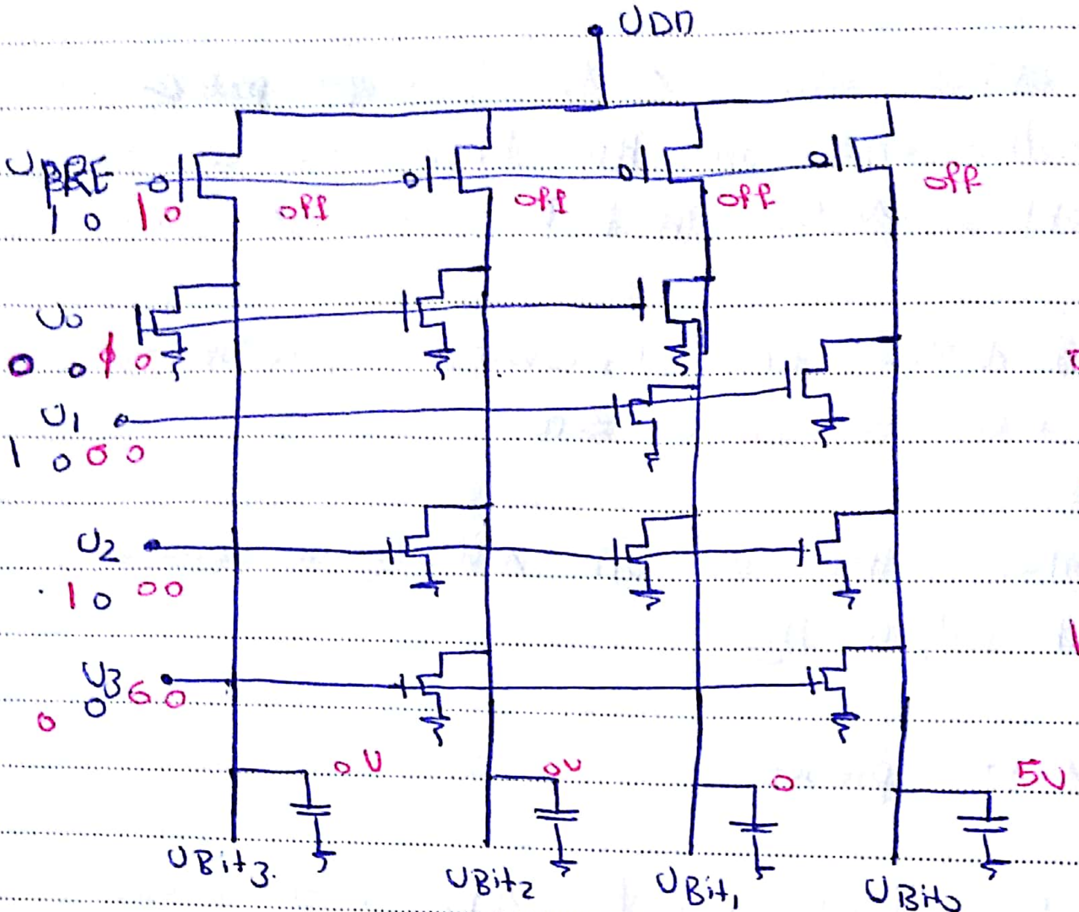
Subject: 144



(NOR Gate).

① VPRE = 0 V = 0 Logic.

V0 - V3 = 0 V = 0 Logic.

PMOS all lin ⇒ VSD = 0V.

NMOS all off Vout = VBit = VDD

output at Logic high

Capacitor Charge to VDD.

② read data when V0 is high (VPRE at Logic high) and all other input at Logic 0.

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PMos off. all NMos except ~~[illegible]~~ ~~off~~ the ones in the first line are all off, NMos in first are all on.

on NMos will discharge capacitor to 0 V ⇒ Logic Zero.

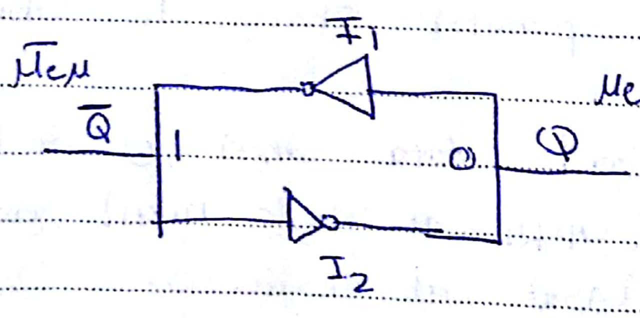
* Gates with no on NMos will remain at output high.

3) Next preset

4) V_1 high (and V_{PRE}) Rest Zeros.

* Chapter 33.1 & 2 Random Access Memory RAM

33.1 and 33.2 Static RAM (all with transmission gates MosFET SRAM



S T A R S Notebook

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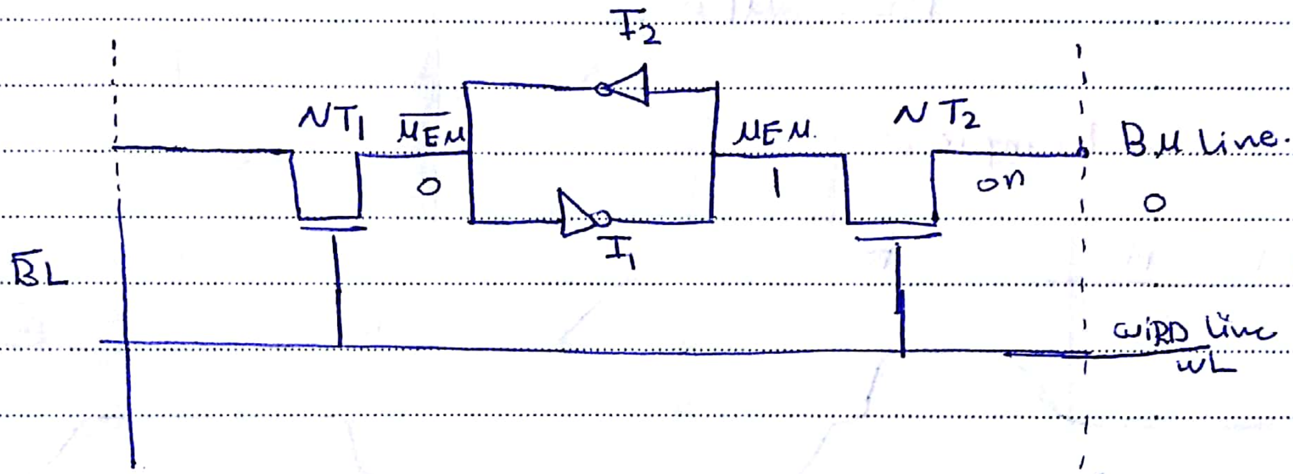
* RAM: Data can be read in a sequence independent of the order it was originally written.

* SRAM :- Maintains storage of data as Long as power is applied to semiconductor cct.



* NT_1 & NT_2, Transmission Gate, when WL high NT are on and conduct when WL Low NT's off and don't conduct (Store) يخزن

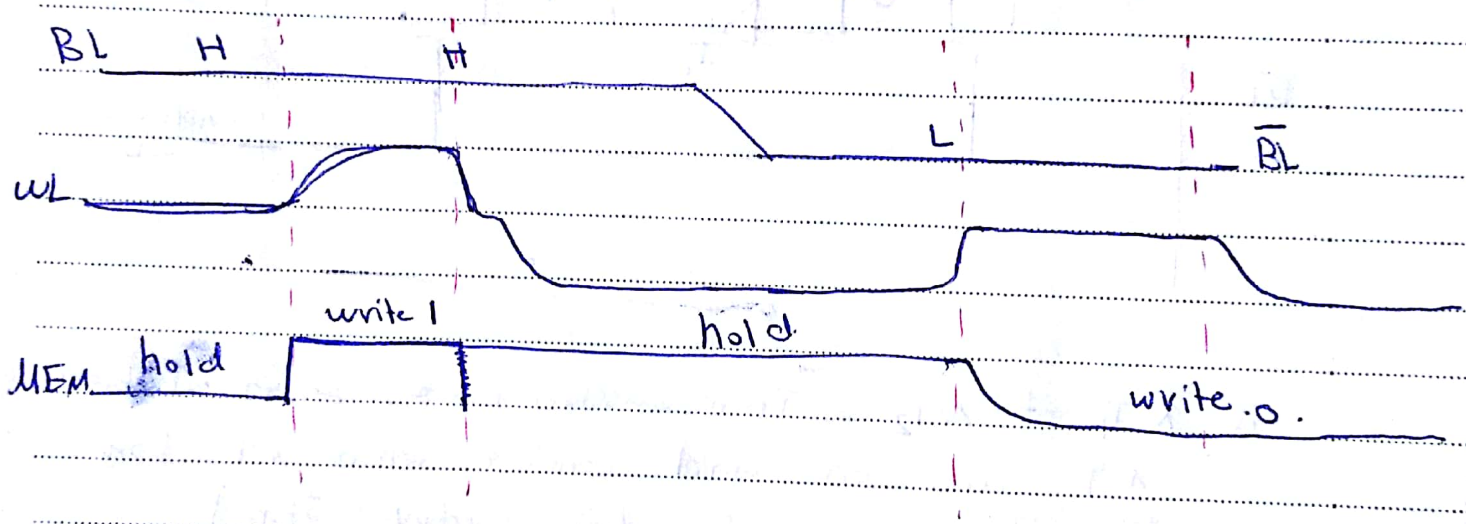
on → (Read & write)
off → (store) يخزن

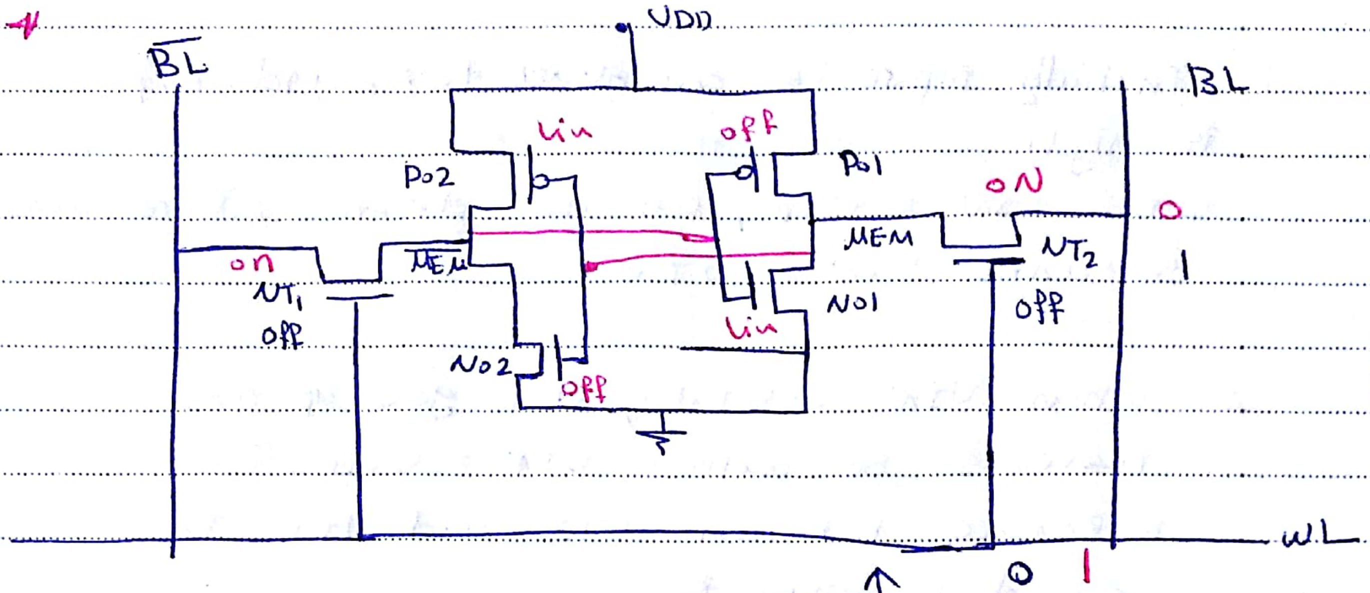
1- Store → $WL = 0$. NTs off data in cell remains the same $MEM = 1$

2- write → $WL = 1$, NTs on. $MEM = BL$, $\overline{MEM} = \overline{BL}$

3- read → $WL = 1$, NT's on. BL read memory, $BL = MEM$, $\overline{BL} = \overline{MEM}$.

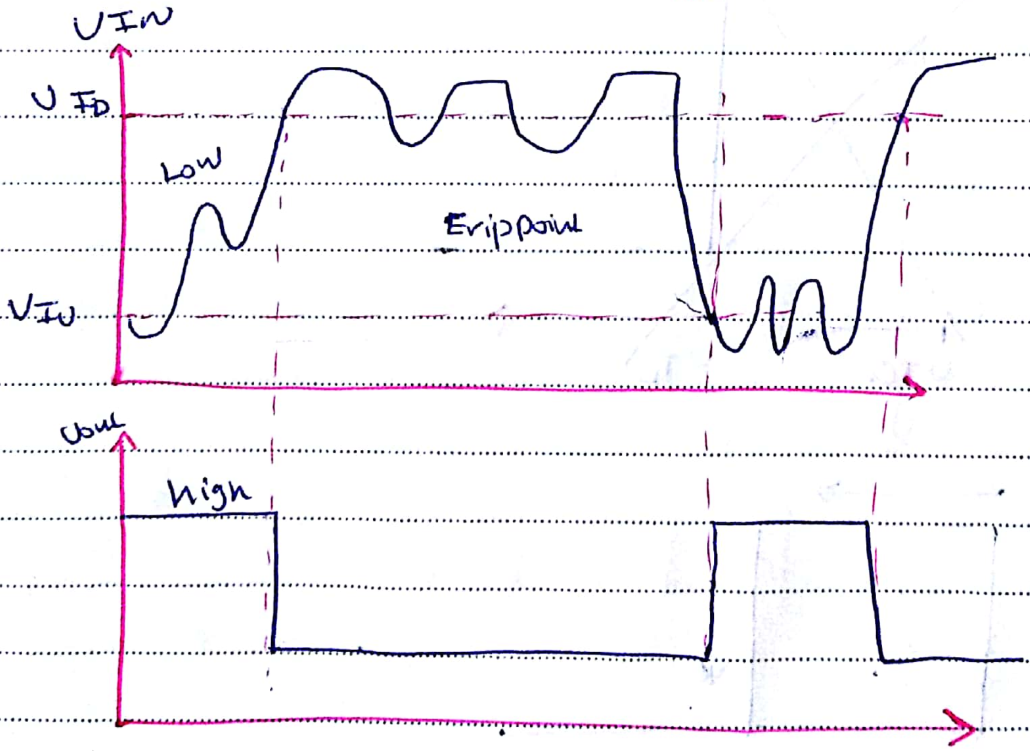
- Example :-





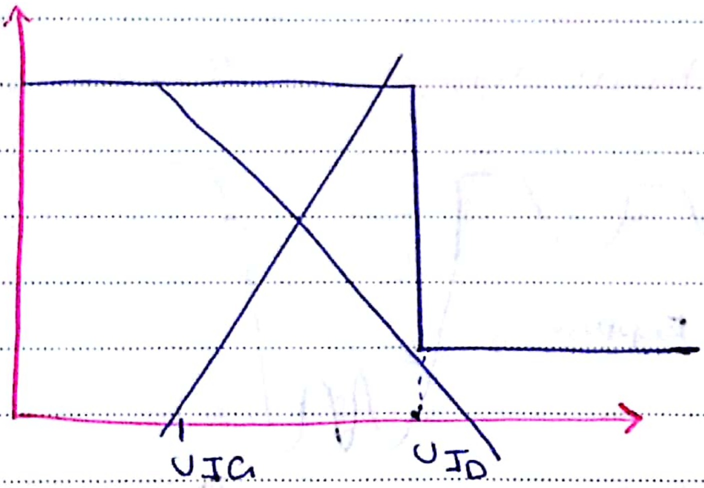
* CMOS Static RAM cell

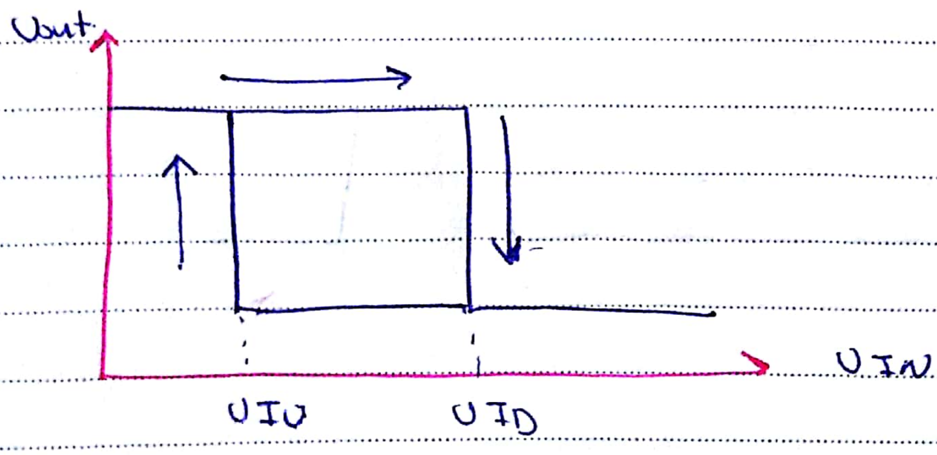
10.6 Schmitt trigger



1- Initially input is considered Low, and o/p is high
when VIN = VID, out goes drown and remains so until VIN = VIU.

2- When VIN = VIN, Vout goes up and remains so until VIN = VID.
Difference between VID and VIU is called (hysteresis)
ST removes noise or reform signal

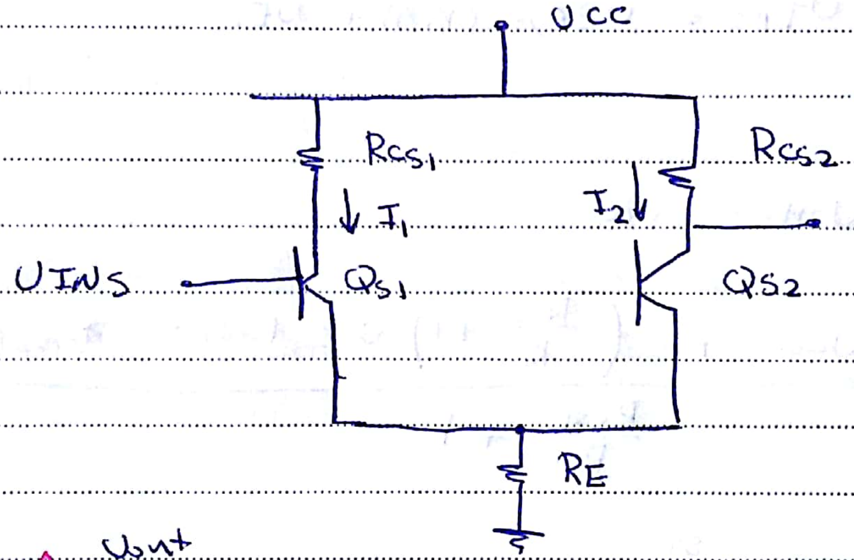




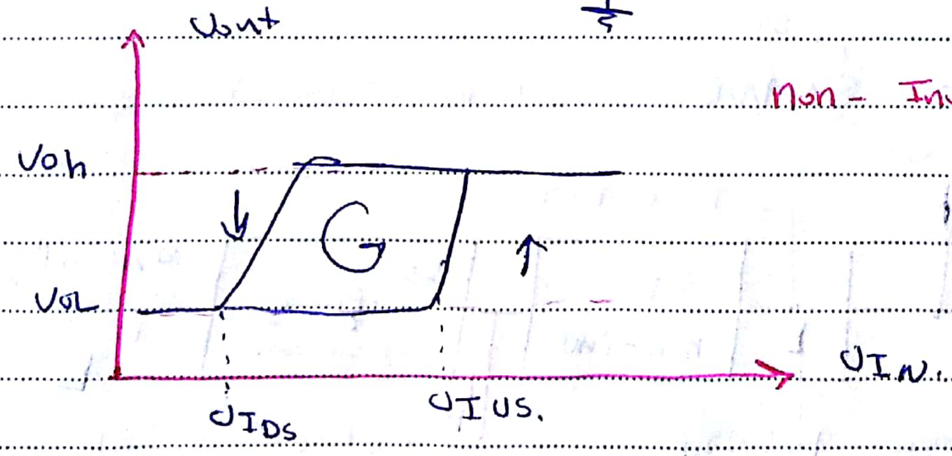
* Initial o/p high
① until VID, voltage Low.
② remains Low until input goes to VIN
⇒ output goes up.

* Emitter coupled Schmitter Trigger

Non-Inverting



Non-Inverting ST



1) + V_{OLS}

$$V_{OL} = V_{CE_2}(sat) + V_E$$

$$V_E = \frac{\frac{V_{CC} - V_{BC}(sat)}{R_{CS1}} + \frac{V_{CC} - V_{CE}(sat)}{R_{CS2}}}{\frac{1}{R_{CS1}} + \frac{1}{R_{CS2}} + \frac{1}{R_E}}$$

ليست للحفظ!!

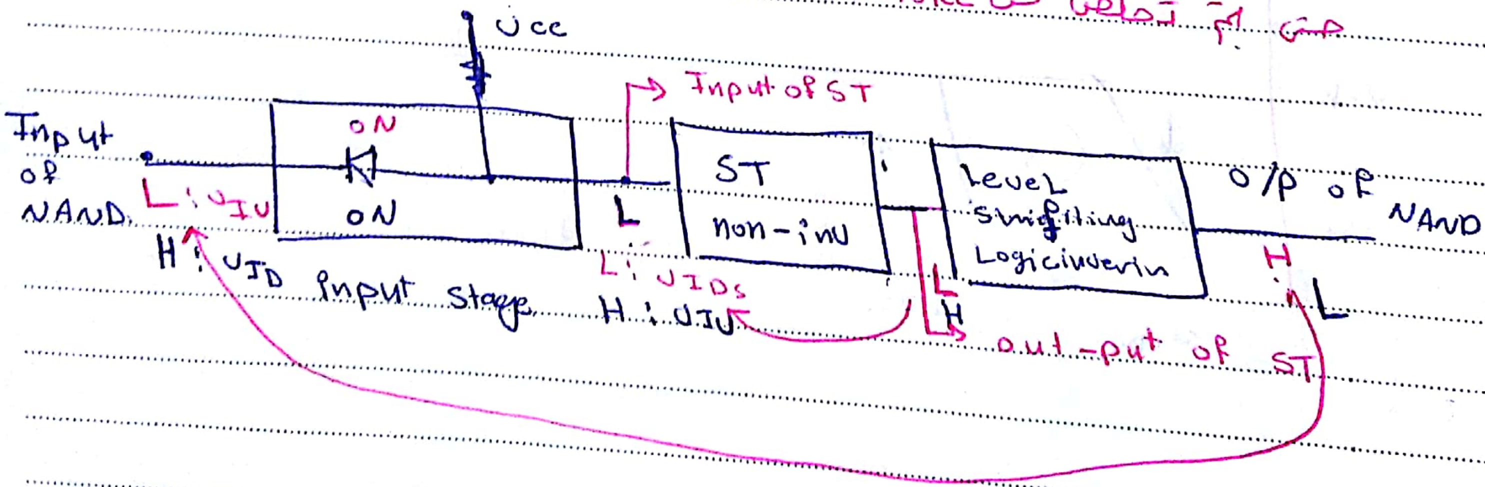
2) − V_{INS} ⇒ $V_{IUS} = V_{BE,S}(F.A) + V_E$.

3) − V_{OHS} ⇒ $V_{OHS} = V_{CC}$

4) V_{IDS} ⇒ $$V_{IDS} = \frac{V_{CC} + \left(\frac{R_{CS}}{R_E} + 1\right) V_{BE,S1}(sat) - V_{BE,S2}(F.A)}{\frac{R_{CS1}}{R_E} + 1}$$

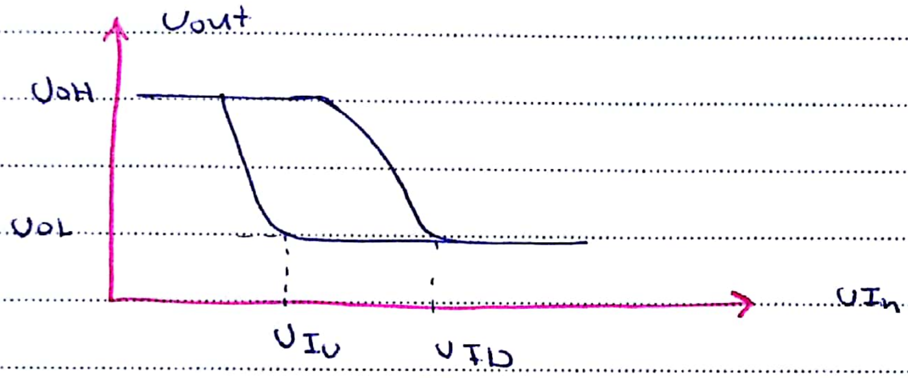
* Figure 10.10 SNAND (→ ST)

أهم حاجة من noise.



* VTC of SNAND 8

* $V_{IU} = V_{ID} - V_{D(on)}$
* $V_{ID} = V_{IUS} - V_{D(on)}$.
* $V_{OH} = V_{CC} - V_{BE(F.A)} - V_{D(on)}$.
* $V_{OL} = V_{CE(sat)}$



* hysteresis:- output high - to - Low and Low to high, transition occurs at different input