Chapter 1 Power Electronic Systems

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Power Electronic Systems

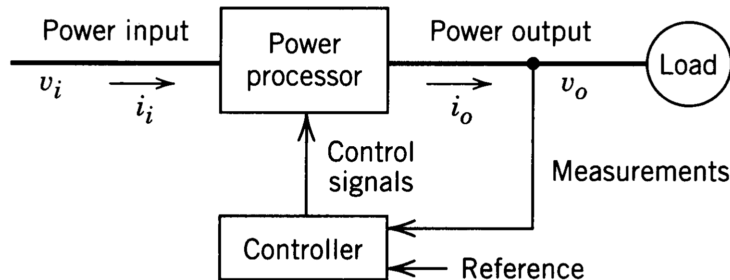

Figure 1-1 Block diagram of a power electronic system.

- Block diagram
- Role of Power Electronics
- Reasons for growth

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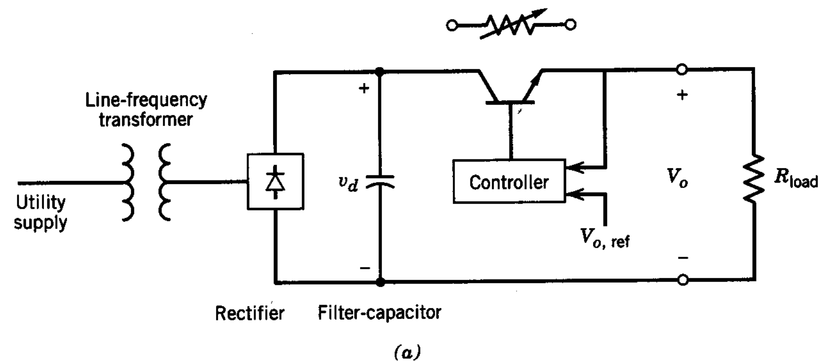
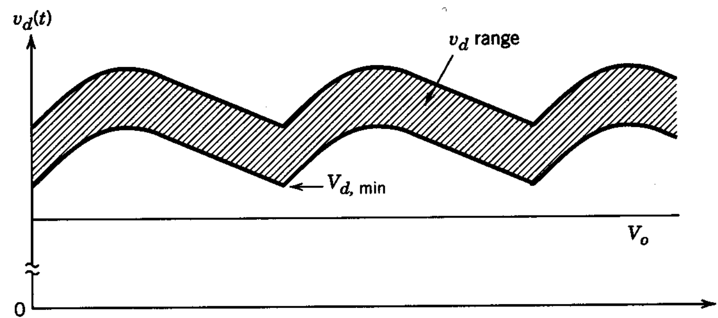
Linear Power Supply





- Series transistor as an adjustable resistor
- Low Efficiency
- Heavy and bulky

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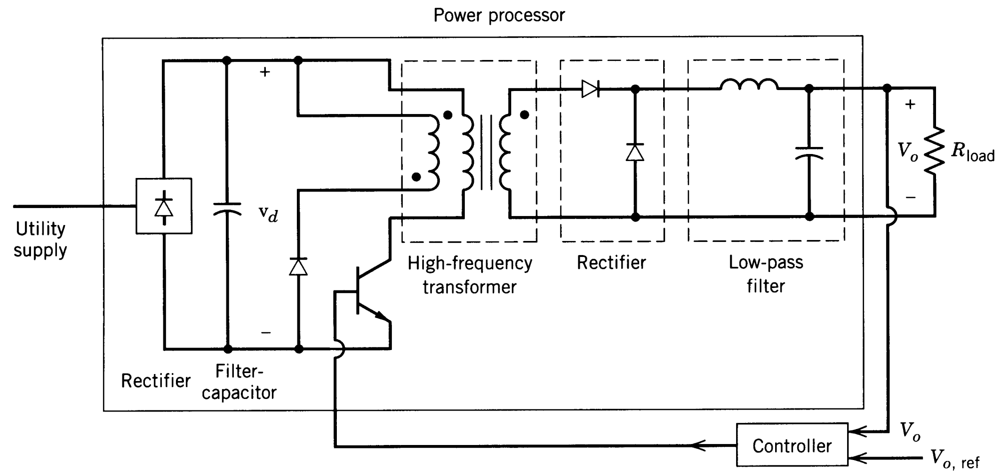
Switch-Mode Power Supply



- Transistor as a switch
- High Efficiency
- High-Frequency Transformer

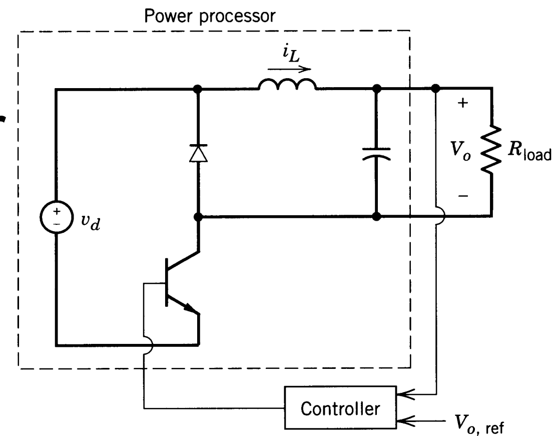


Figure 1-3 Switch-mode dc power supply.

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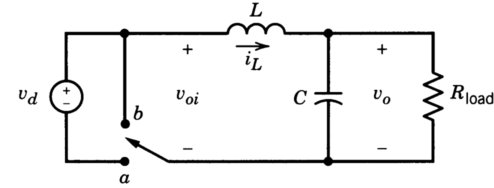
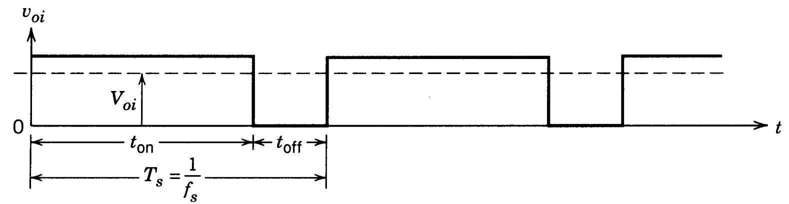
Basic Principle of Switch-Mode Synthesis



(a)



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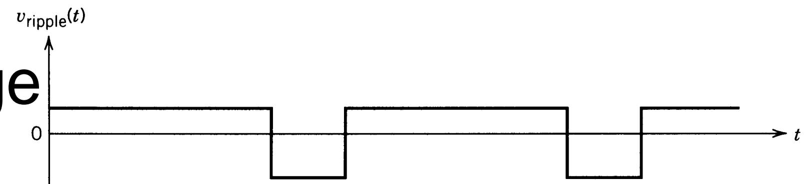

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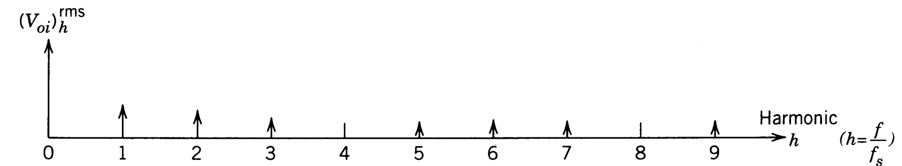

(d)

Figure 1-4 Equivalent circuit, waveforms, and frequency spectrum of the supply in Fig. 1-3.

- Constant switching frequency
- pulse width controls the average
- L-C filters the ripple

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Application in Adjustable Speed Drives

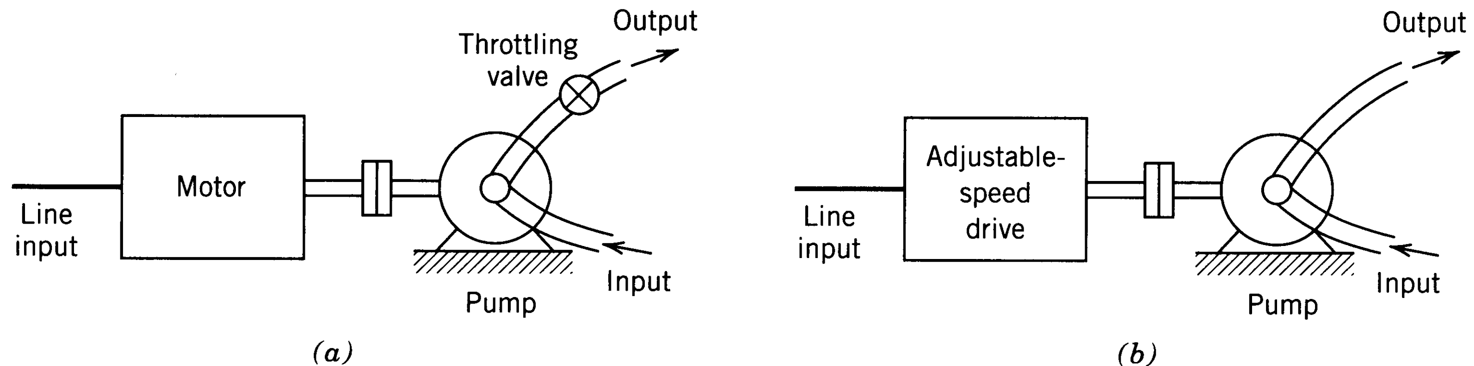

Figure 1-5 Energy conservation: (*a*) conventional drive, (*b*) adjustable-speed drive.

- Conventional drive wastes energy across the throttling valve to adjust flow rate
- Using power electronics, motor-pump speed is adjusted efficiently to deliver the required flow rate

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Scope and Applications

TABLE 1-1 Power Electronic Applications

(a) *Residential*
- Refrigeration and freezers
- Space heating
- Air conditioning
- Cooking
- Lighting
- Electronics (personal computers, other entertainment equipment)

(b) *Commercial*
- Heating, ventilating, and air conditioning
- Central refrigeration
- Lighting
- Computers and office equipment
- Uninterruptible power supplies (UPSs)
- Elevators

(c) *Industrial*
- Pumps
- Compressors
- Blowers and fans
- Machine tools (robots)
- Arc furnaces, induction furnaces
- Lighting
- Industrial lasers
- Induction heating
- Welding

(d) *Transportation*
- Traction control of electric vehicles
- Battery chargers for electric vehicles
- Electric locomotives
- Street cars, trolley buses
- Subways
- Automotive electronics including engine controls

(e) *Utility systems*
- High-voltage dc transmission (HVDC)
- Static var compensation (SVC)
- Supplemental energy sources (wind, photovoltaic), fuel cells
- Energy storage systems
- Induced-draft fans and boiler feedwater pumps

(f) *Aerospace*
- Space shuttle power supply systems
- Satellite power systems
- Aircraft power systems

(g) *Telecommunications*
- Battery chargers
- Power supplies (dc and UPS)

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Power Processor as a Combination of Converters

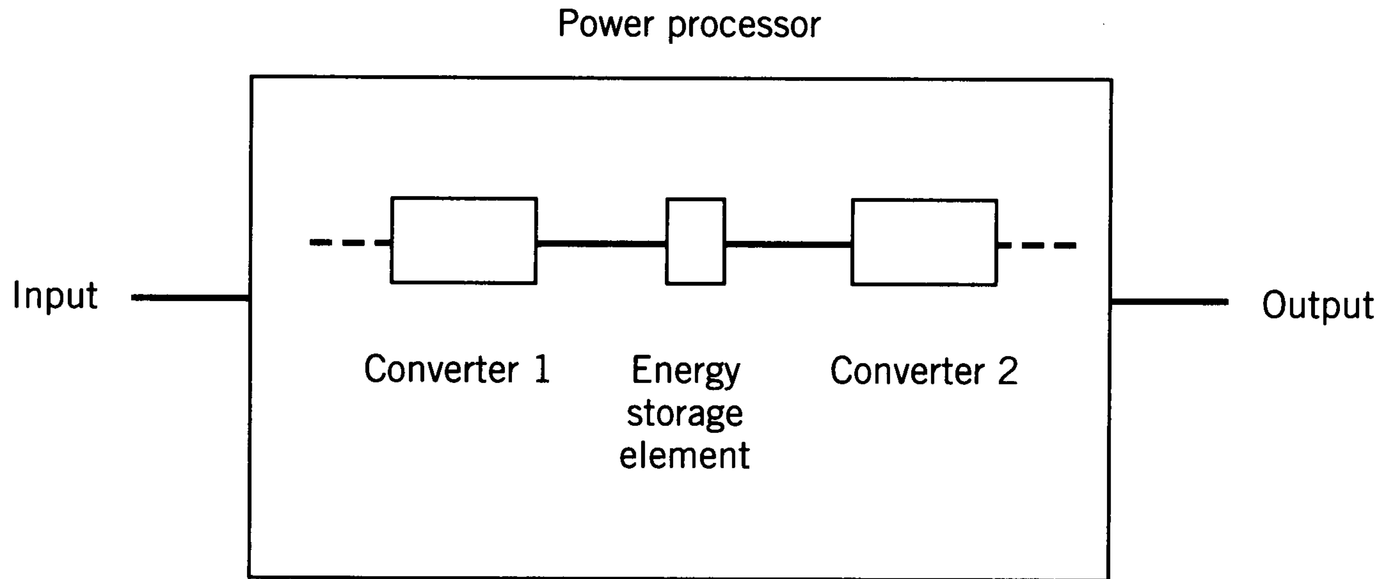

Figure 1-6 Power processor block diagram.

- Most practical topologies require an energy storage element, which also decouples the input and the output side converters

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Power Flow through Converters

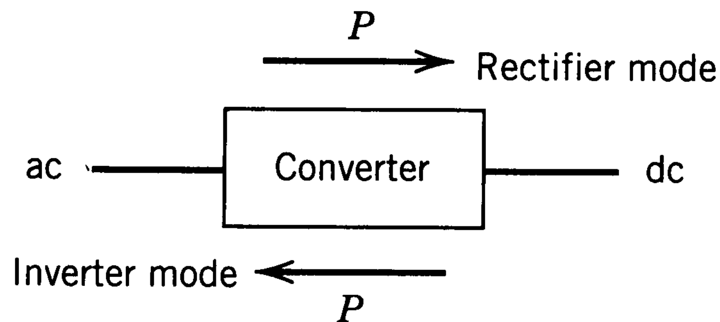

Figure 1-7 ac-to-dc converters.

- Converter is a general term
- An ac/dc converter is shown here
- Rectifier Mode of operation when power from ac to dc
- Inverter Mode of operation when power from ac to dc

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AC Motor Drive

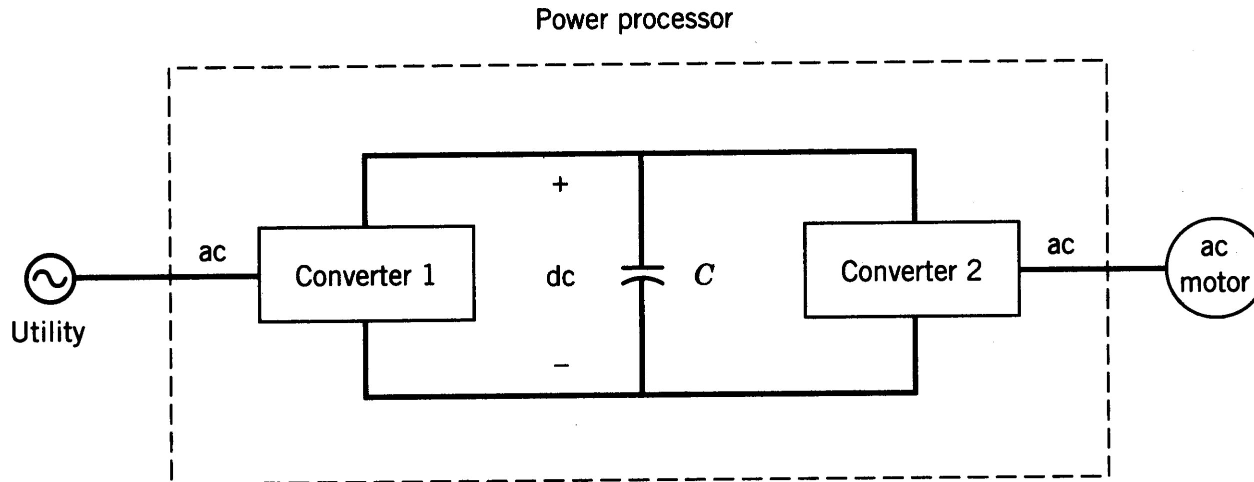

Figure 1-8 Block diagram of an ac motor drive.

- Converter 1 rectifies line-frequency ac into dc
- Capacitor acts as a filter; stores energy; decouples
- Converter 2 synthesizes low-frequency ac to motor
- Polarity of dc-bus voltage remains unchanged
  - ideally suited for transistors of converter 2

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Matrix Converter

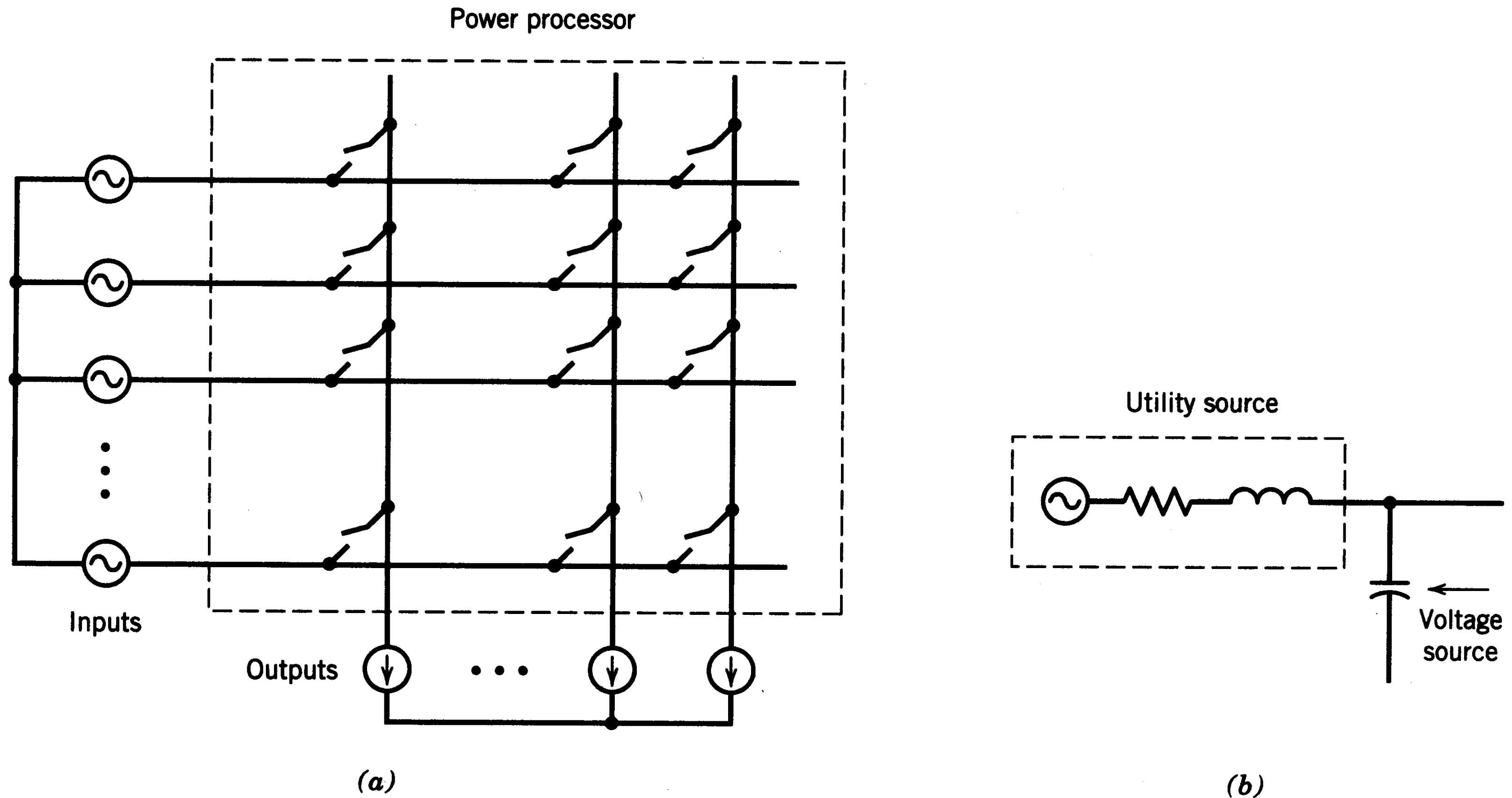

Figure 1-9 (*a*) Matrix converter. (*b*) Voltage source.

- Very general structure
- Would benefit from bi-directional and bi-polarity switches
- Being considered for use in specific applications

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Interdisciplinary Nature of Power Electronics

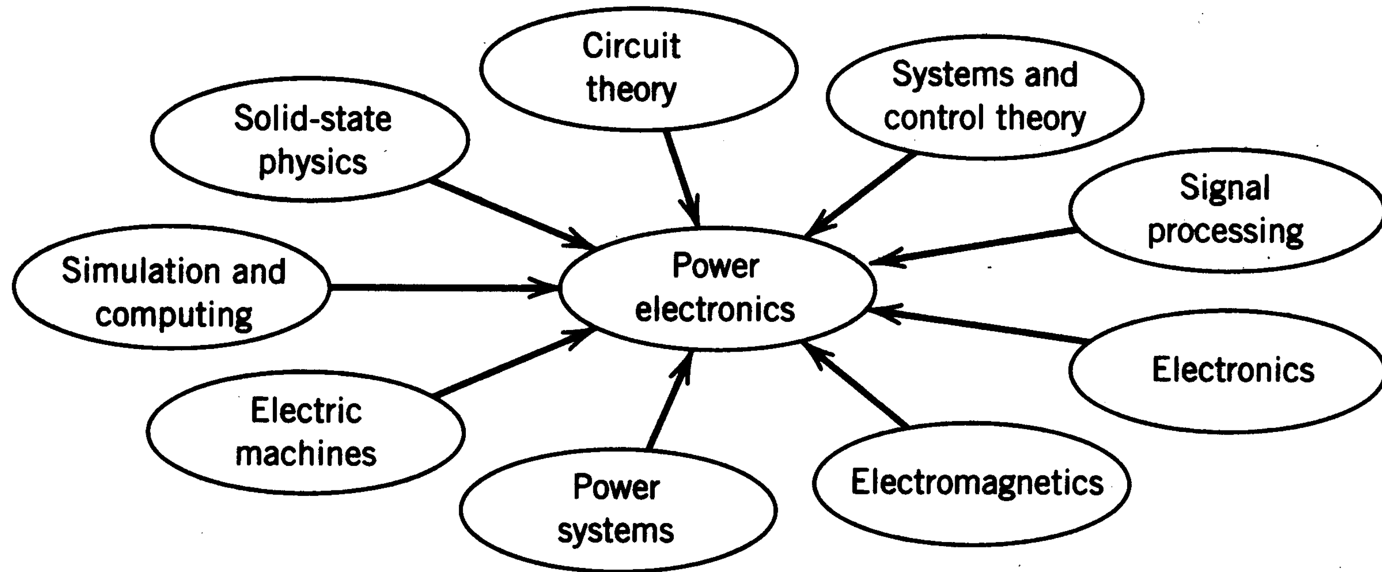

Figure 1-10 Interdisciplinary nature of power electronics.

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Chapter 2 Overview of Power Semiconductor Devices

Chapter 2 Overview of Power Semiconductor Switches **16**

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Diodes

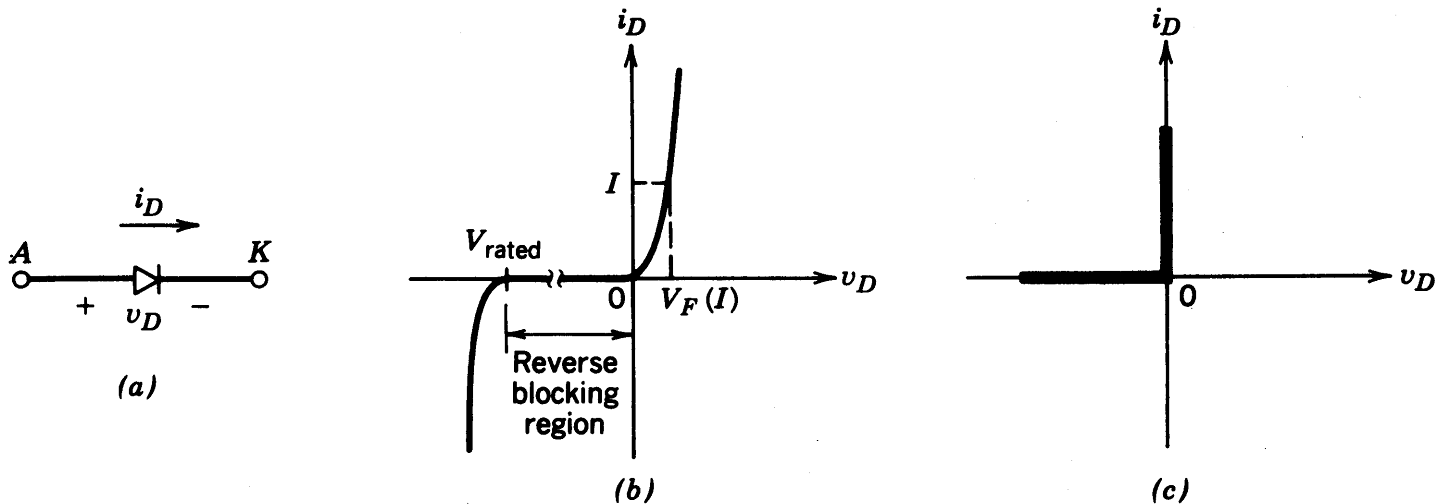

Figure 2-1 Diode: (*a*) symbol, (*b*) *i–v* characteristic, (*c*) idealized characteristic.

- On and off states controlled by the power circuit

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Diode Turn-Off

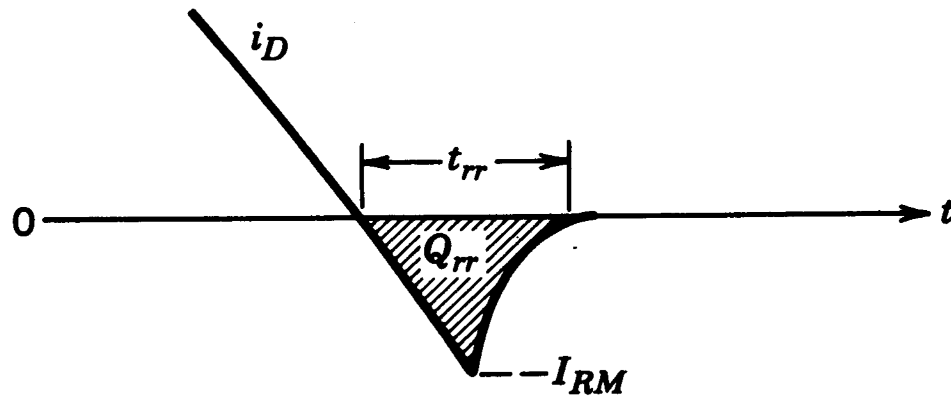

Figure 2-2 Diode turn-off.

- Fast-recovery diodes have a small reverse-recovery time

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Thyristors

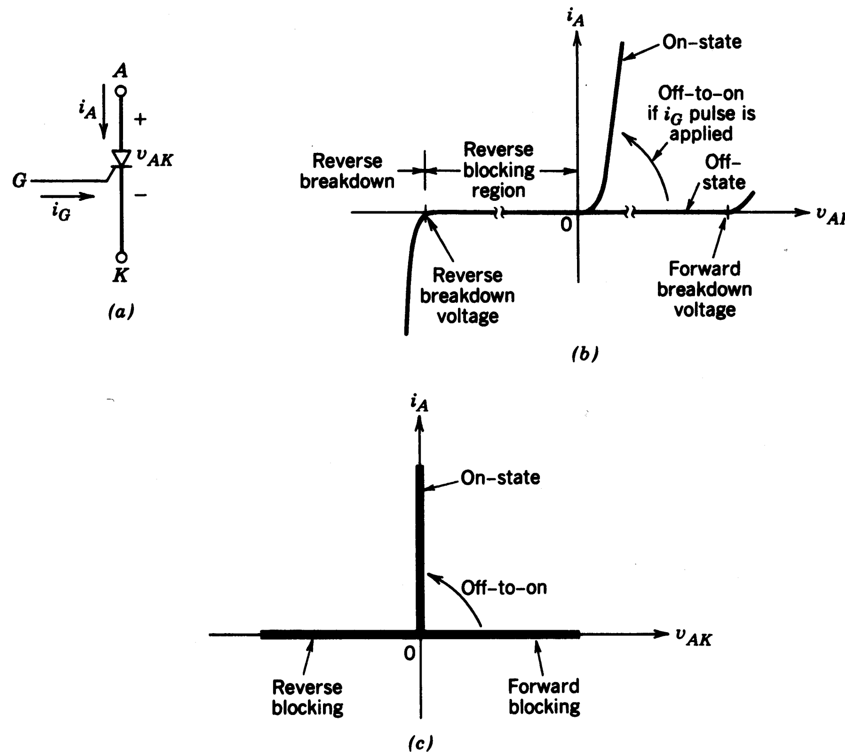

Figure 2-3 Thyristor: (*a*) symbol, (*b*) *i–v* characteristics, (*c*) idealized characteristics.

- Semi-controlled device
- Latches ON by a gate-current pulse if forward biased
- Turns-off if current tries to reverse

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Thyristor in a Simple Circuit

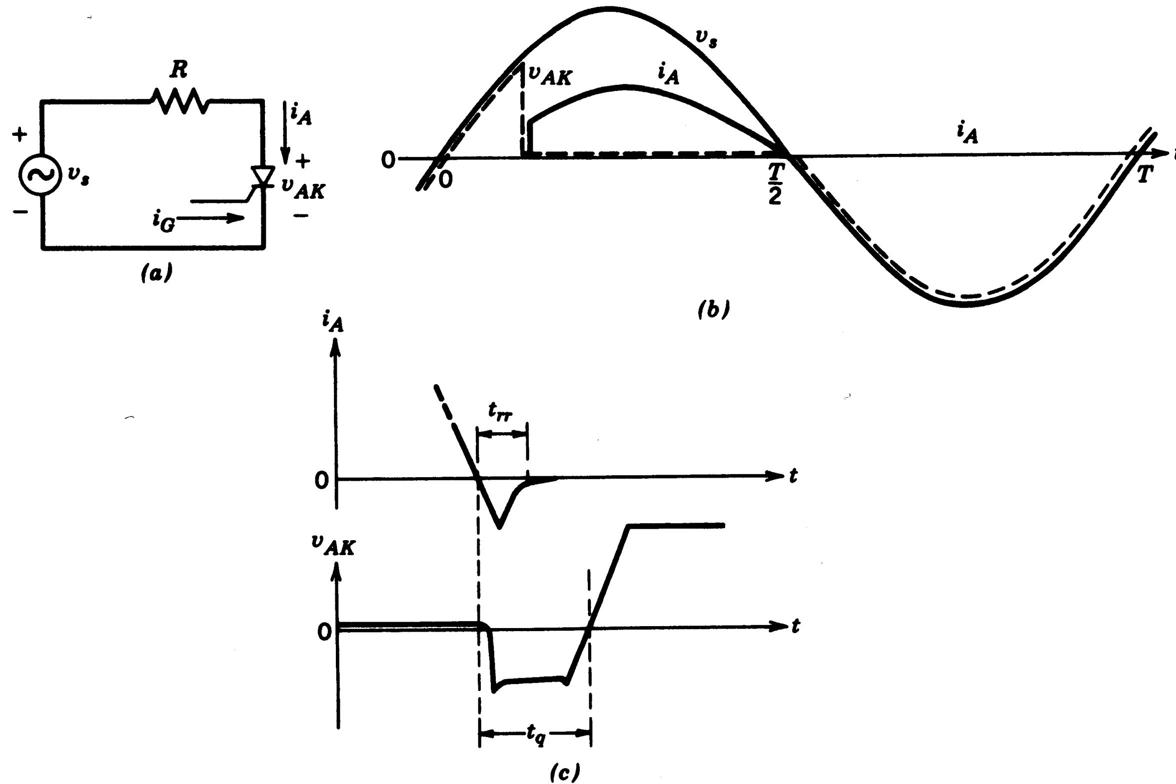

Figure 2-4 Thyristor: (*a*) circuit, (*b*) waveforms, (*c*) turn-off time interval t_q.

- For successful turn-off, reverse voltage required for an interval greater than the turn-off interval

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Generic Switch Symbol

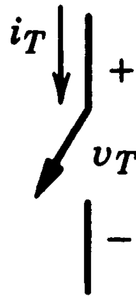

Figure 2-5 Generic controllable switch.

- Idealized switch symbol
- When on, current can flow only in the direction of the arrow
- Instantaneous switching from one state to the other
- Zero voltage drop in on-state
- Infinite voltage and current handling capabilities

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Switching Characteristics (linearized)

Switching Power Loss is proportional to:

- switching frequency
- turn-on and turn-off times

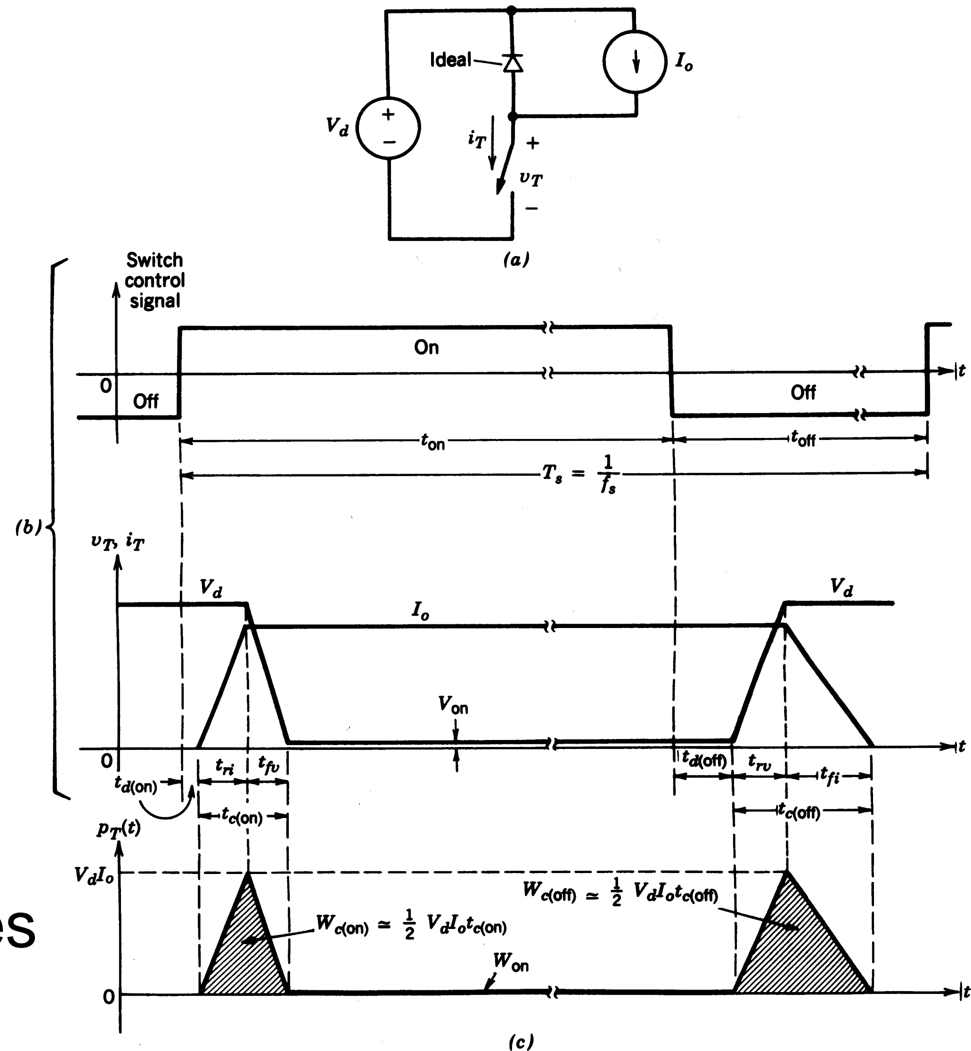

Figure 2-6 Generic-switch switching characteristics (linearized): (*a*) simplified clamped-inductive-switching circuit, (*b*) switch waveforms, (*c*) instantaneous switch power loss.

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Bipolar Junction Transistors (BJT)

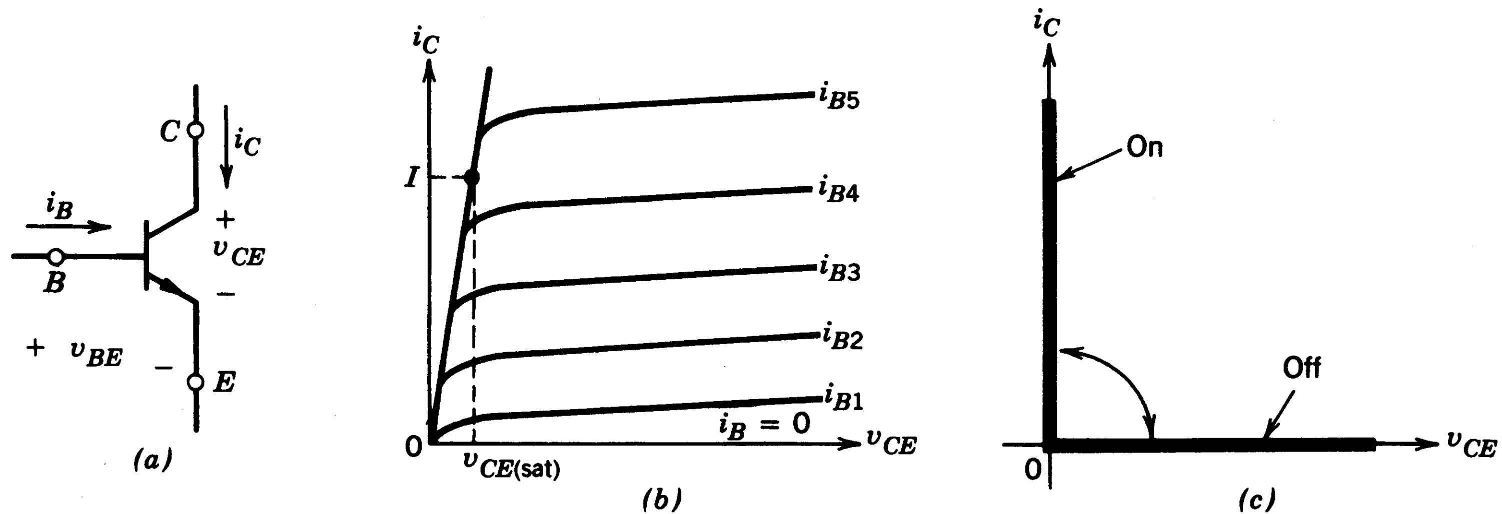

Figure 2-7 A BJT: (*a*) symbol, (*b*) *i–v* characteristics, (*c*) idealized characteristics.

- Used commonly in the past
- Now used in specific applications
- Replaced by MOSFETs and IGBTs

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Various Configurations of BJTs

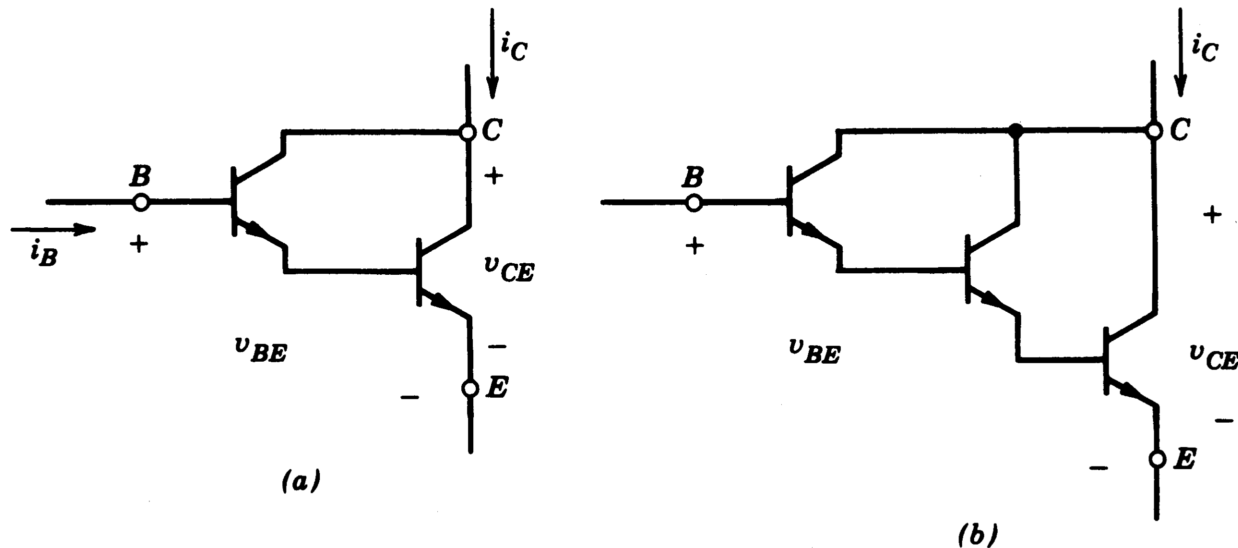

Figure 2-8 Darlington configurations: (*a*) Darlington, (*b*) triple Darlington.

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MOSFETs

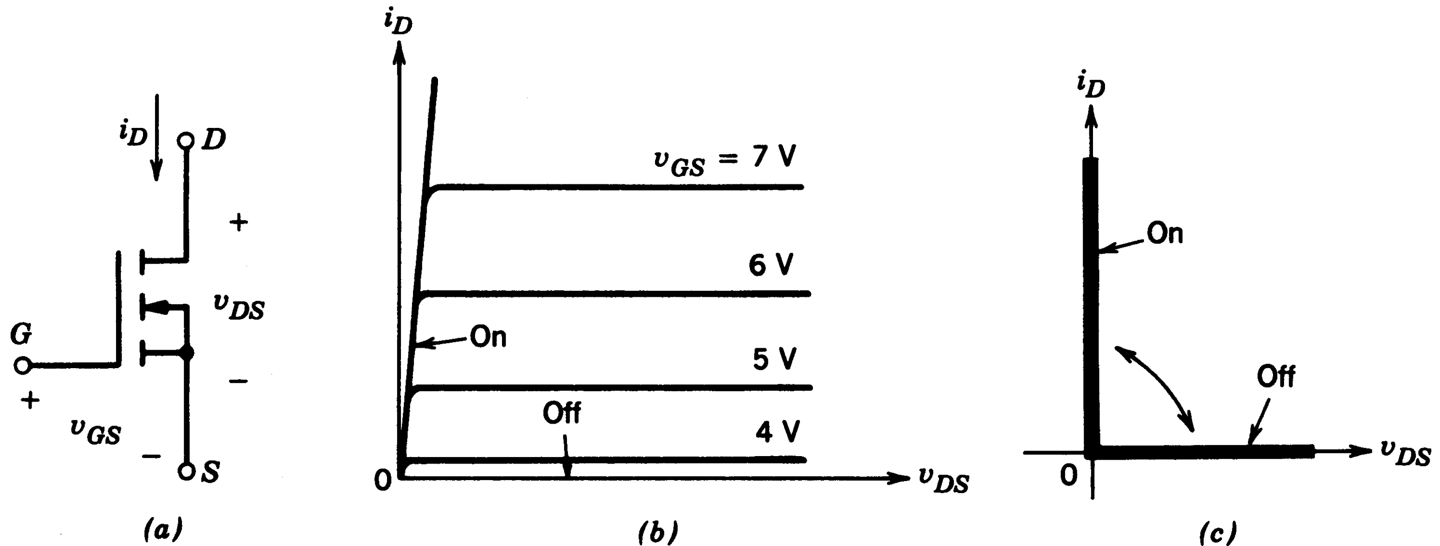

Figure 2-9 *N*-channel MOSFET: (*a*) symbol, (*b*) *i–v* characteristics, (*c*) idealized characteristics.

- Easy to control by the gate
- Optimal for low-voltage operation at high switching frequencies
- On-state resistance a concern at higher voltage ratings

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Gate-Turn-Off Thyristors (GTO)

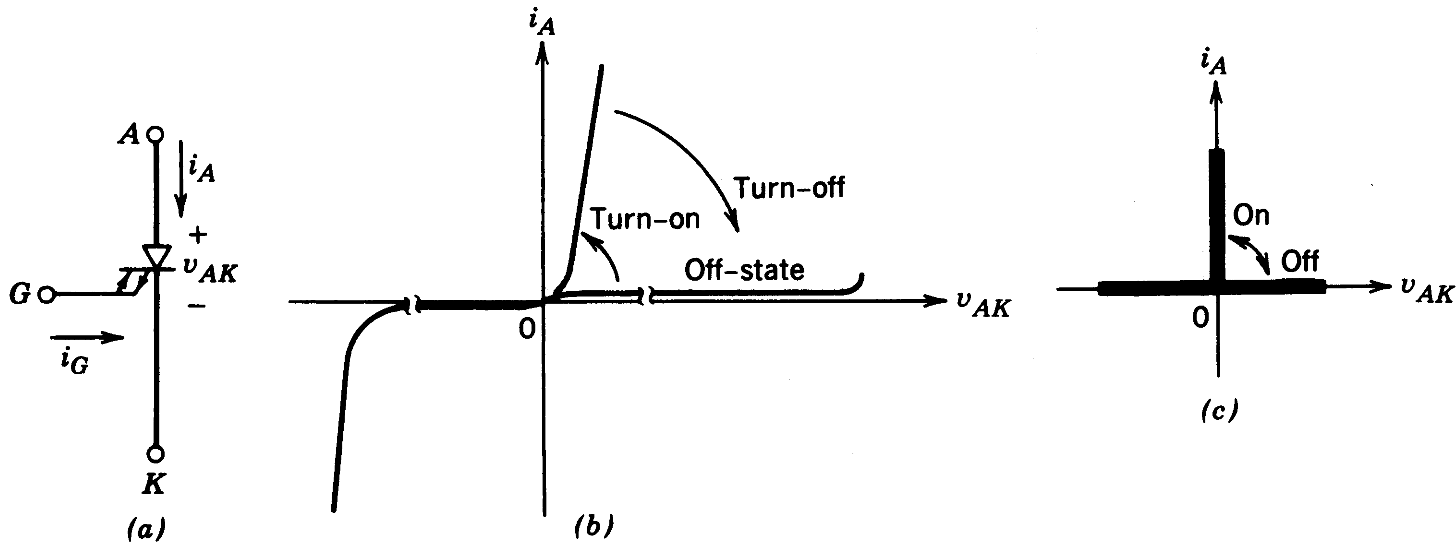

Figure 2-10 A GTO: (*a*) symbol, (*b*) *i–v* characteristics, (*c*) idealized characteristics.

- Slow switching speeds
- Used at very high power levels
- Require elaborate gate control circuitry

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GTO Turn-Off

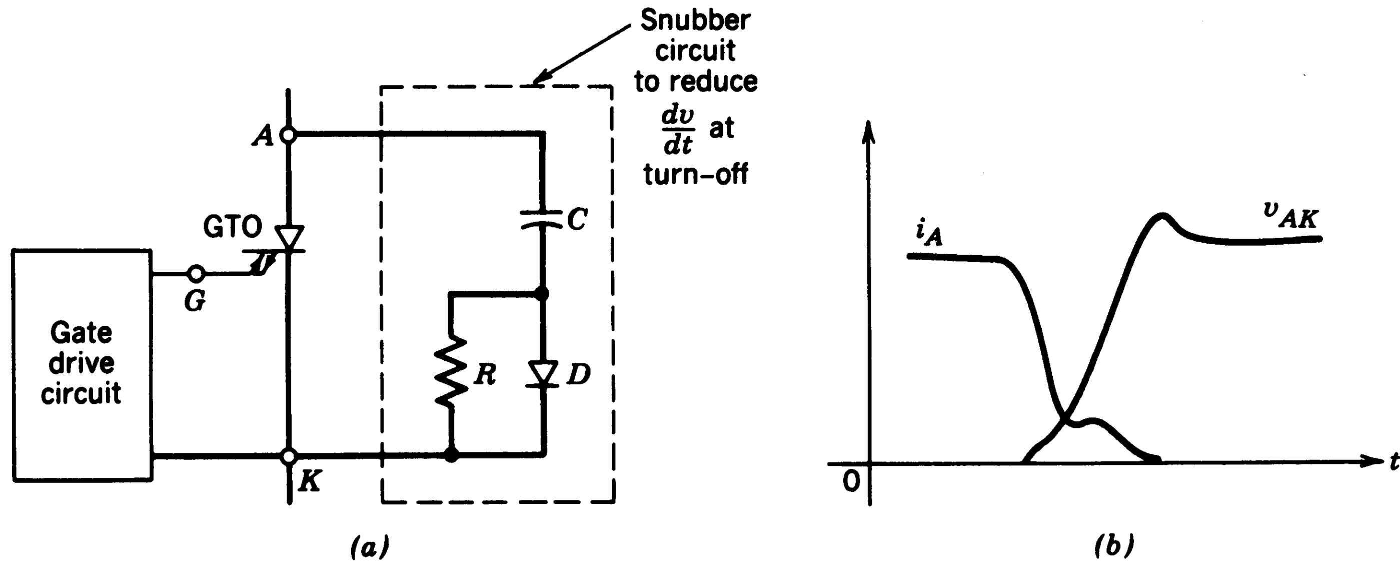

Figure 2-11 Gate turn-off transient characteristics: (*a*) snubber circuit, (*b*) GTO turn-off characteristic.

- Need a turn-off snubber

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IGBT

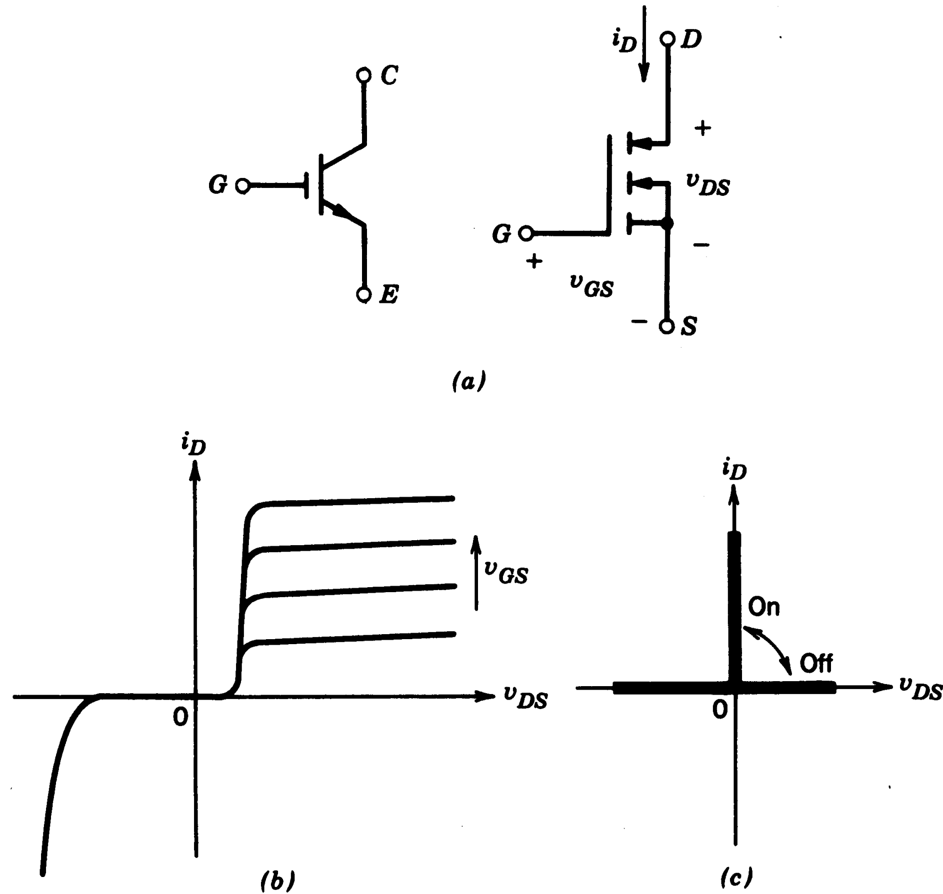

Figure 2-12 An IGBT: (*a*) symbol, (*b*) *i–v* characteristics, (*c*) idealized characteristics.

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MCT

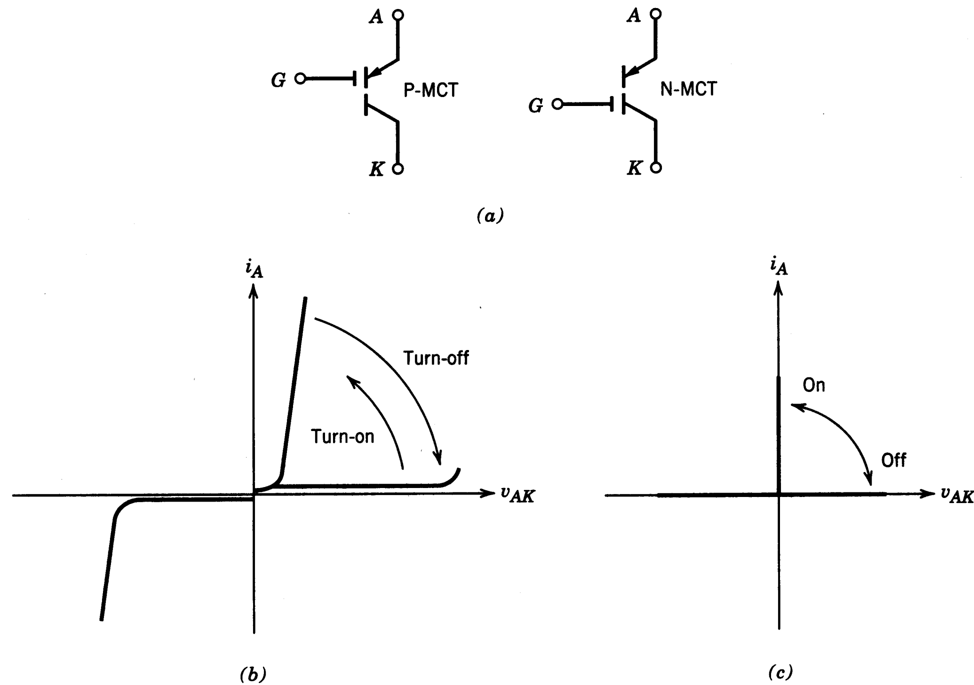

Figure 2-13 An MCT: (*a*) circuit symbols, (*b*) *i–v* characteristic, (*c*) idealized characteristics.

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Comparison of Controllable Switches

Table 2-1 Relative Properties of Controllable Switches

Device	*Power Capability*	*Switching Speed*
BJT/MD	Medium	Medium
MOSFET	Low	Fast
GTO	High	Slow
IGBT	Medium	Medium
MCT	Medium	Medium

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Summary of Device Capabilities

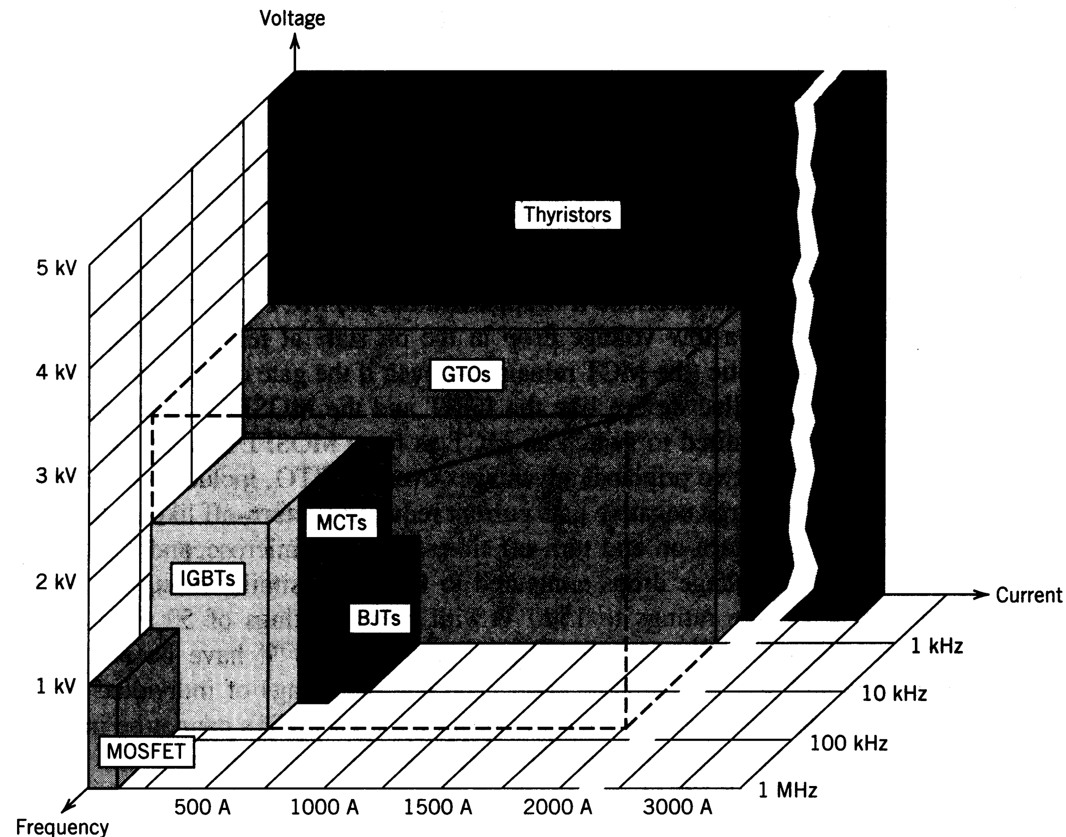

Figure 2-14 Summary of power semiconductor device capabilities. All devices except the MCT have a relatively mature technology, and only evolutionary improvements in the device capabilities are anticipated in the next few years. However, MCT technology is in a state of rapid expansion, and significant improvements in the device capabilities are possible, as indicated by the expansion arrow in the diagram.

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Chapter 3

Review of Basic Electrical and Magnetic Circuit Concepts

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Symbols and Conventions

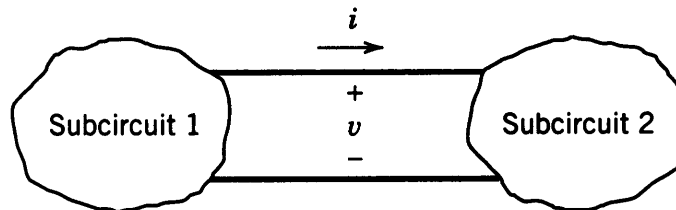

Figure 3-1 Instantaneous power flow.

- Symbols
- Polarity of Voltages; Direction of Currents
- MKS SI units

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Sinusoidal Steady State

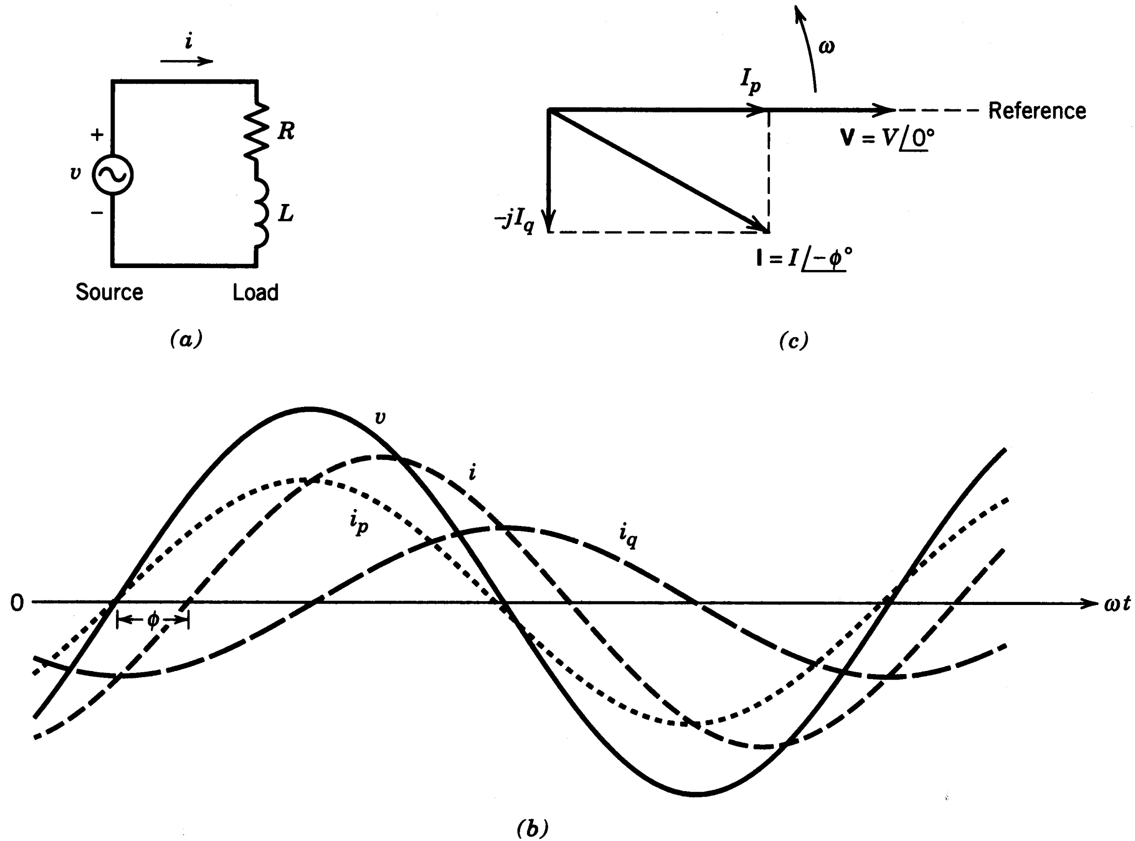

Figure 3-2 Sinusoidal steady state.

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Three-Phase Circuit

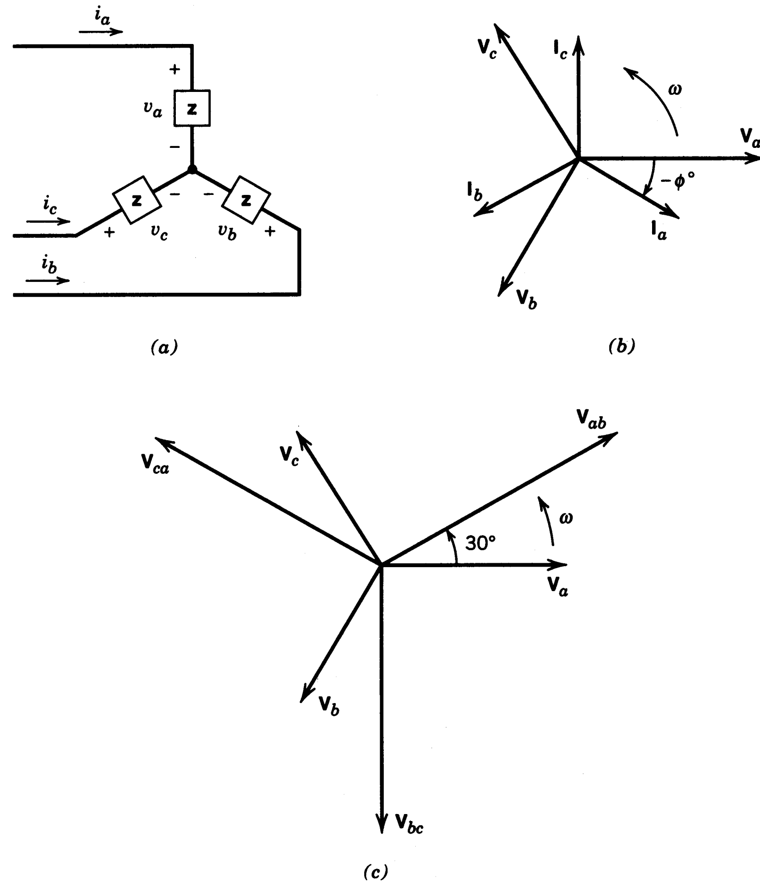
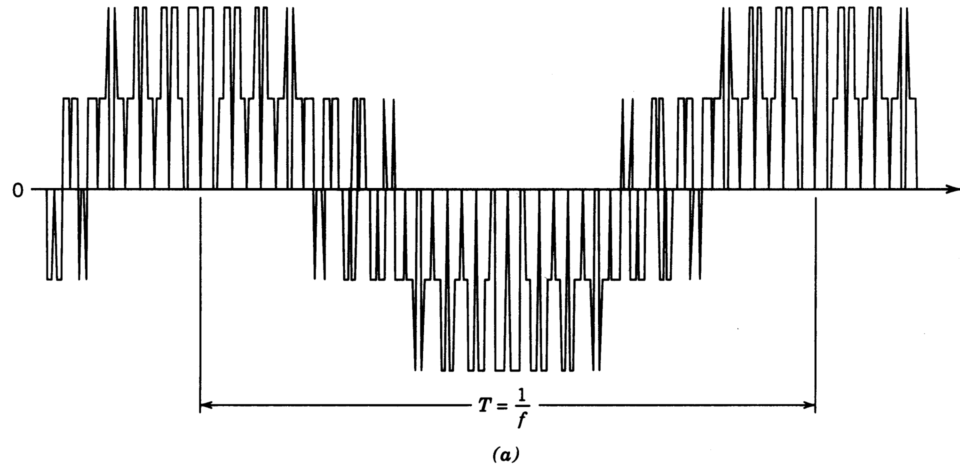


Figure 3-3 Three-phase circuit.

Steady State in Power Electronics



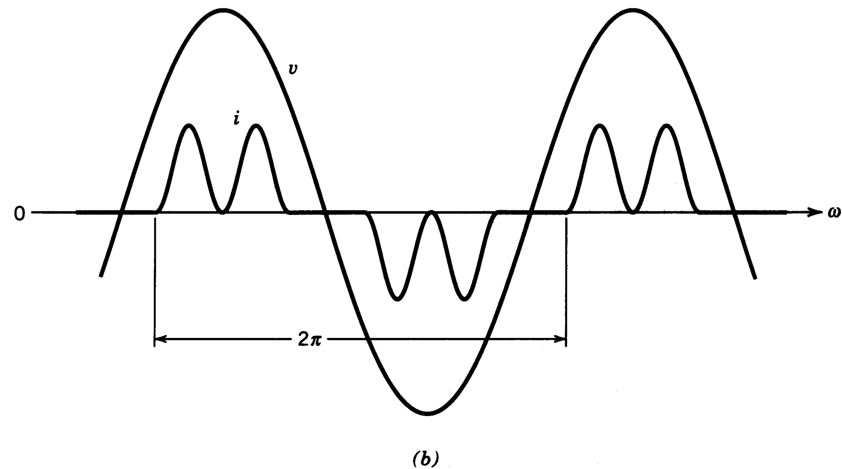


Figure 3-4 Nonsinusoidal waveforms in steady state.

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Fourier Analysis

Table 3-1 Use of Symmetry in Fourier Analysis

Symmetry	*Condition Required*	a_h and b_h
Even	$f(-t) = f(t)$	$b_h = 0 \quad a_h = \frac{2}{\pi}\int_0^{\pi} f(t)\cos(h\omega t)\, d(\omega t)$
Odd	$f(-t) = -f(t)$	$a_h = 0 \quad b_h = \frac{2}{\pi}\int_0^{\pi} f(t)\sin(h\omega t)\, d(\omega t)$
Half-wave	$f(t) = -f(t + \frac{1}{2}T)$	$a_h = b_h = 0$ for even h $a_h = \frac{2}{\pi}\int_0^{\pi} f(t)\cos(h\omega t)\, d(\omega t)$ for odd h $b_h = \frac{2}{\pi}\int_0^{\pi} f(t)\sin(h\omega t)\, d(\omega t)$ for odd h
Even quarter-wave	Even and half-wave	$b_h = 0$ for all h $a_h = \begin{cases} \frac{4}{\pi}\int_0^{\pi/2} f(t)\cos(h\omega t)\, d(\omega t) & \text{for odd } h \\ 0 & \text{for even } h \end{cases}$
Odd quarter-wave	Odd and half-wave	$a_h = 0$ for all h $b_h = \begin{cases} \frac{4}{\pi}\int_0^{\pi/2} f(t)\sin(h\omega t)\, d(\omega t) & \text{for odd } h \\ 0 & \text{for even } h \end{cases}$

Distortion in the Input Current

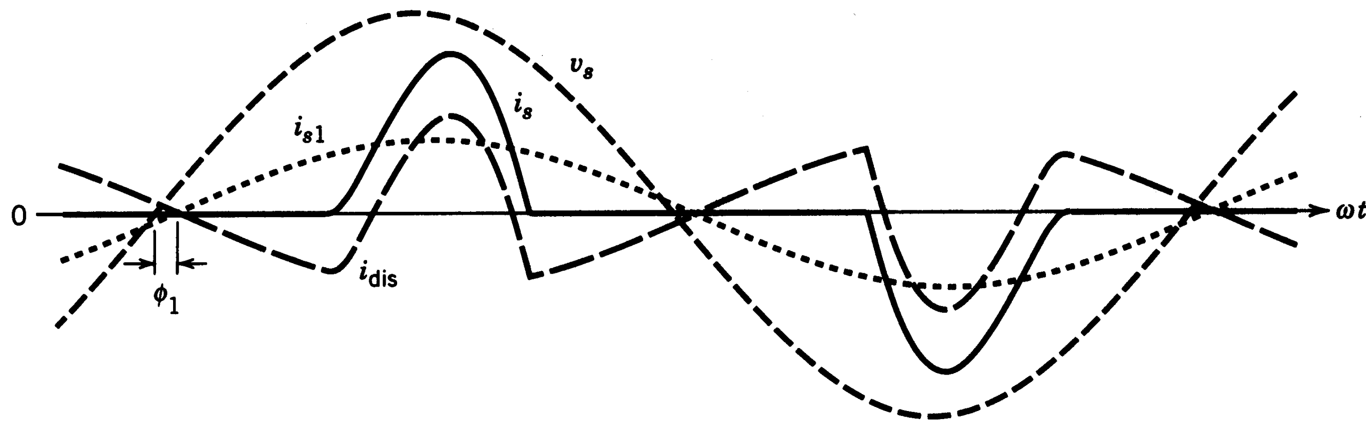

Figure 3-5 Line-current distortion.

- Voltage is assumed to be sinusoidal
- Subscript "1" refers to the fundamental
- The angle is between the voltage and the current fundamental

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Phasor Representation

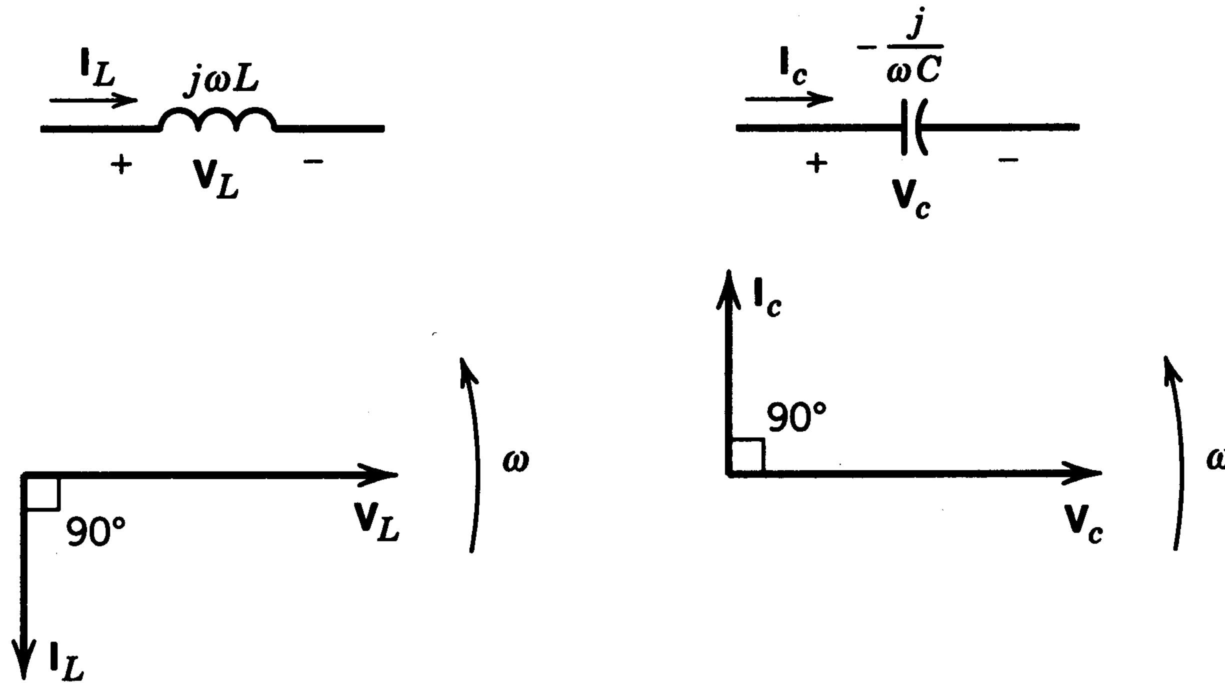

Figure 3-6 Phasor representation.

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Response of *L* and *C*

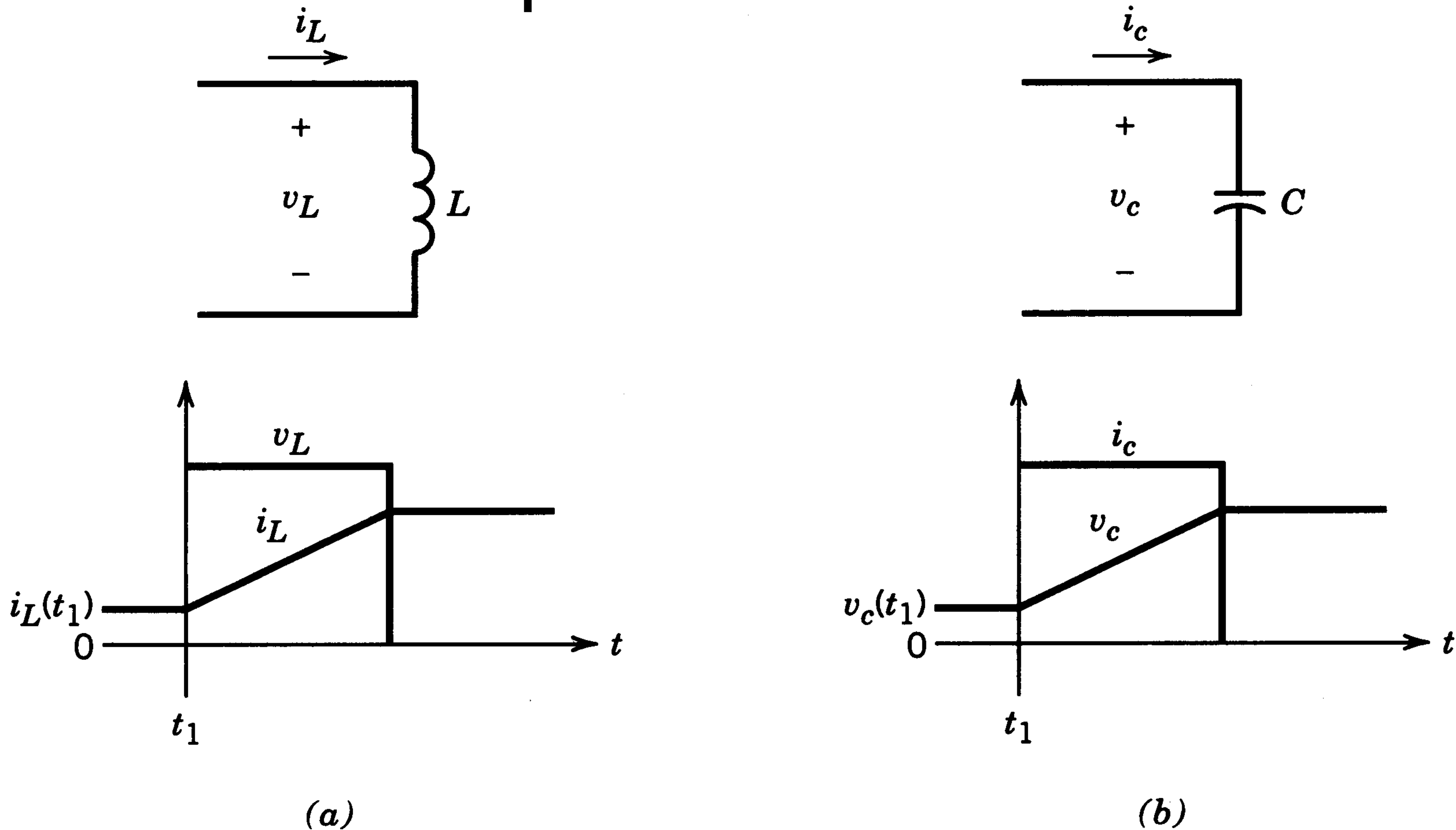

Figure 3-7 Inductor and capacitor response.

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Inductor Voltage and Current in Steady State

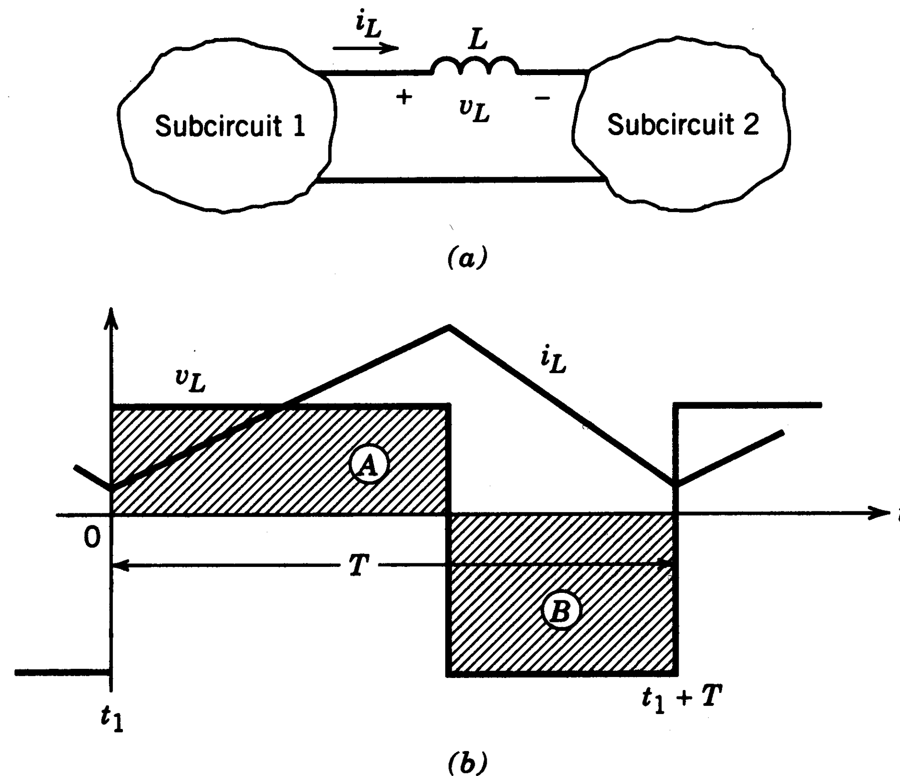

Figure 3-8 Inductor response in steady state.

- Volt-seconds over T equal zero.

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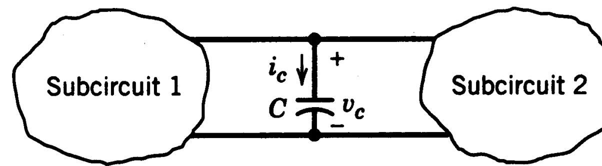
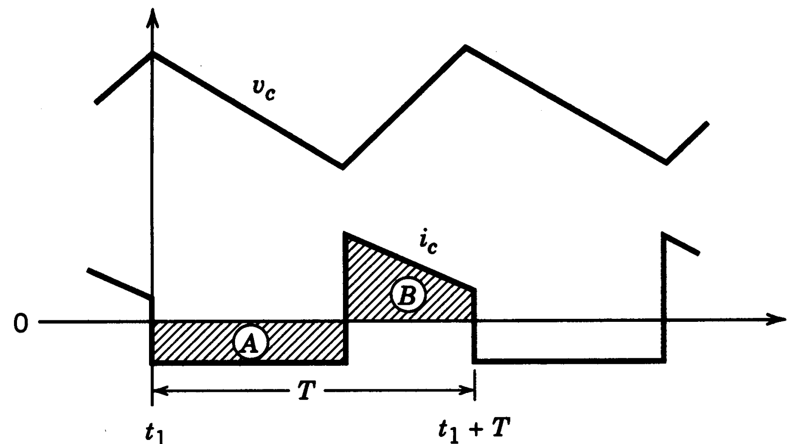
Capacitor Voltage and Current in Steady State



(a)

- Amp-seconds over T equal zero.



(b)

Figure 3-9 Capacitor response in steady state.

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Ampere's Law

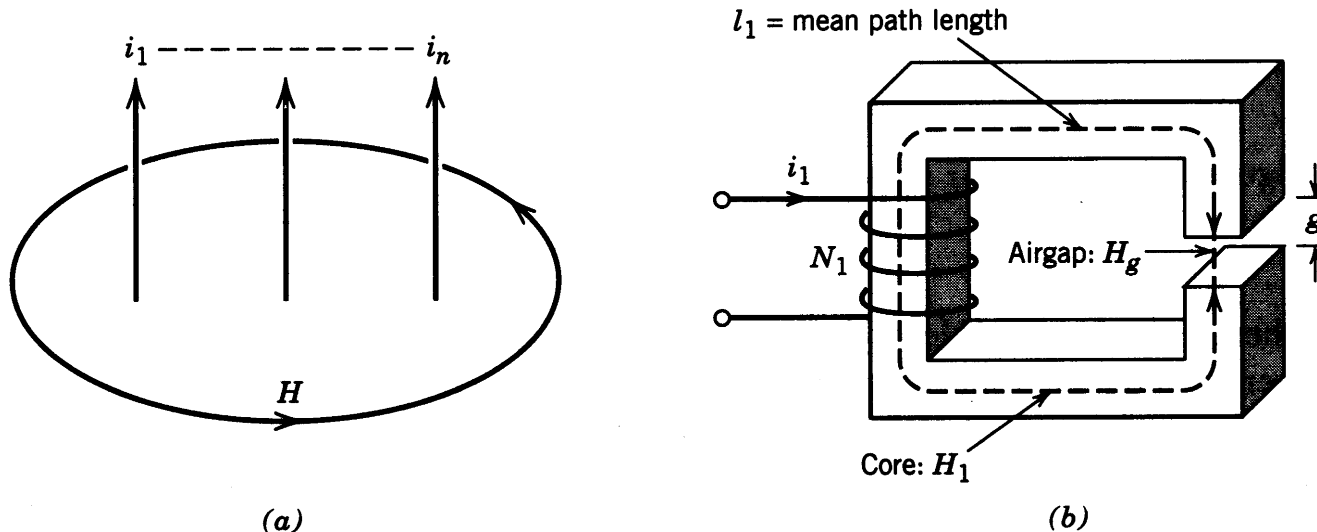

Figure 3-10 (*a*) General formulation of Ampere's law. (*b*) Specific example of Ampere's law in the case of a winding on a magnetic core with an airgap.

- Direction of magnetic field due to currents
- Ampere's Law: Magnetic field along a path

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Direction of Magnetic Field

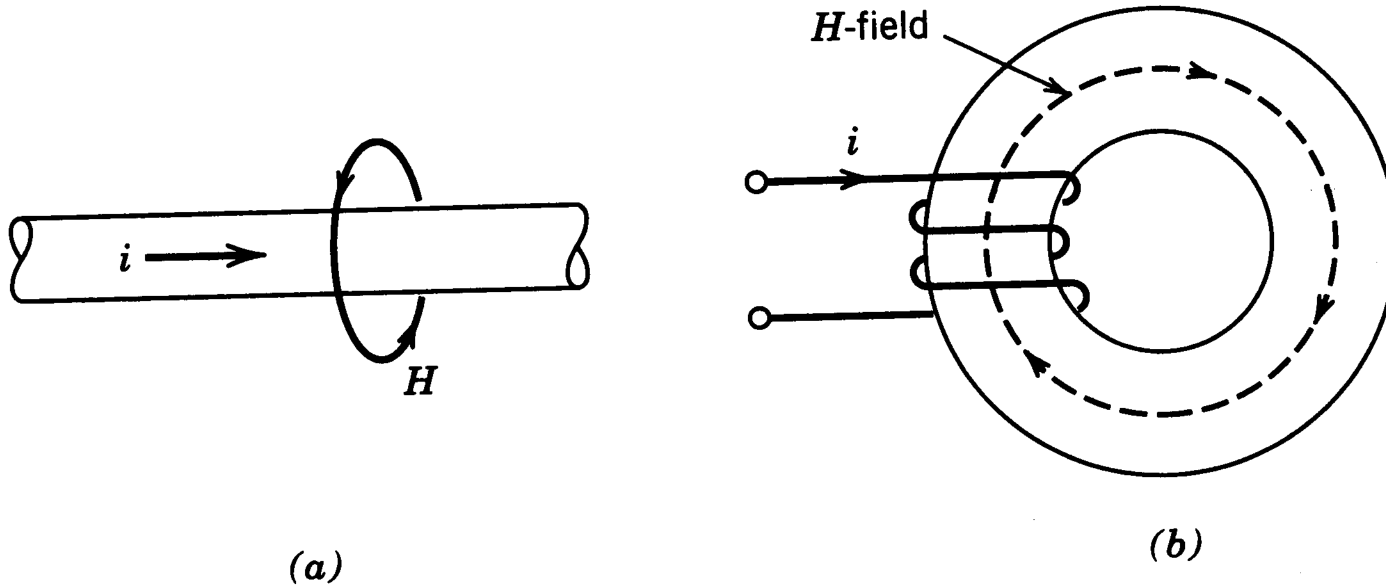

Figure 3-11 Determination of the magnetic field direction via the right-hand rule in (*a*) the general case and (*b*) a specific example of a current-carrying coil wound on a toroidal core.

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B-H Relationship; Saturation

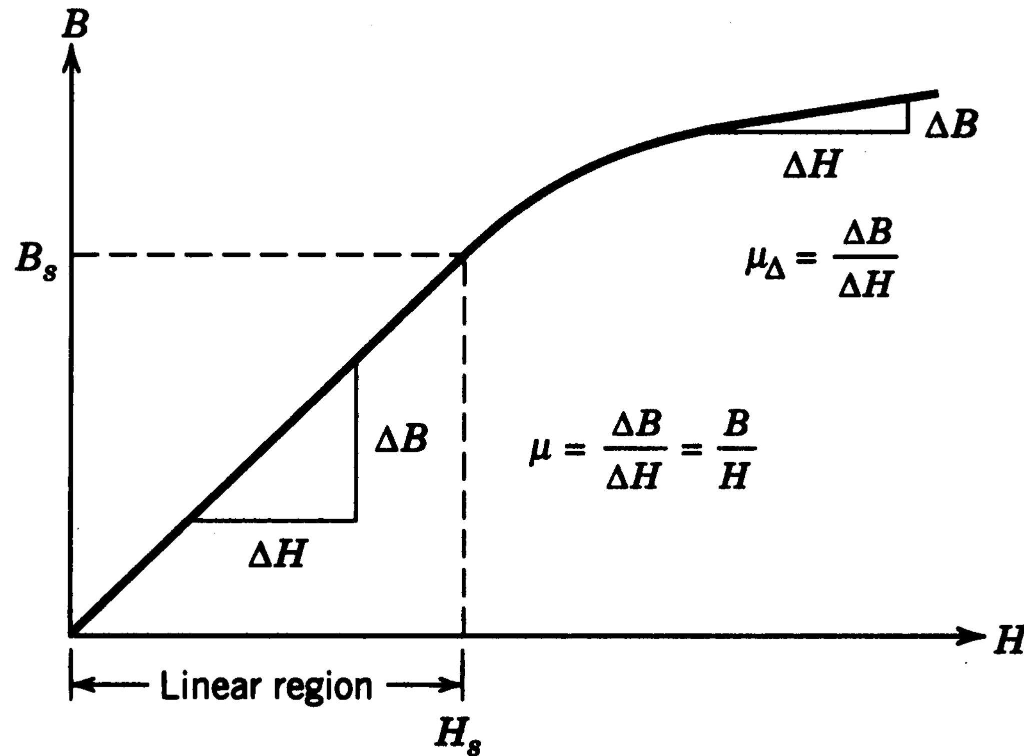

Figure 3-12 Relation between *B*- and *H*-fields.

- Definition of permeability

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Continuity of Flux Lines

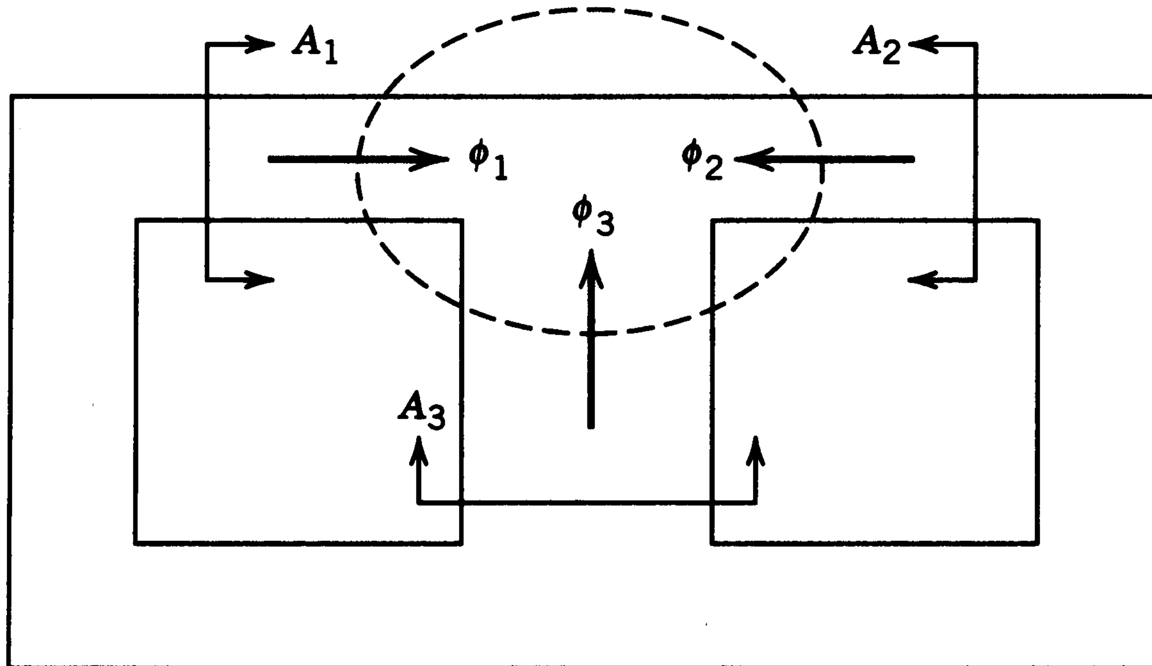

Figure 3-13 **Continuity of flux.**

$$f_1 + f_2 + f_3 = 0$$

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Concept of Magnetic Reluctance

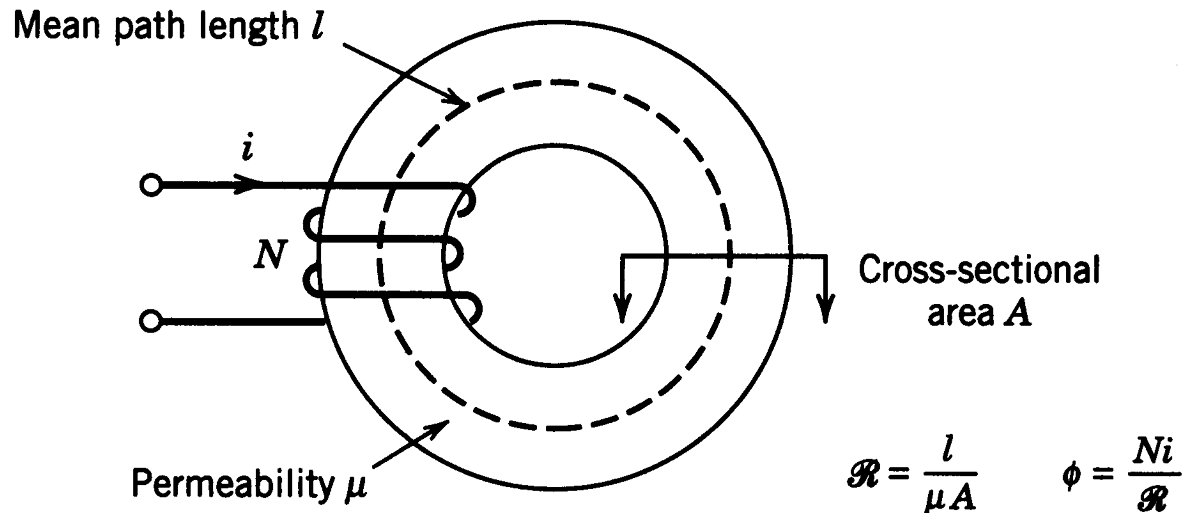

Figure 3-14 Magnetic reluctance.

- Flux is related to ampere-turns by reluctance

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Analogy between Electrical and Magnetic Variables

Table 3-2 Electrical–Magnetic Analogy

Magnetic Circuit	*Electric Circuit*
mmf Ni	v
Flux ϕ	i
reluctance $\mathcal{R}$	R
permeability μ	$1/\rho$, where ρ = resistivity

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Analogy between Equations in Electrical and Magnetic Circuits

Table 3-3 Magnetic–Electrical Circuit Equation Analogy

Magnetic	*Electrical (dc)*
$\frac{Ni}{\phi} = \mathcal{R} = \frac{l}{\mu A}$	Ohm's law: $\frac{v}{i} = R = \frac{l}{A/\rho}$
$\phi \sum_k \mathcal{R}_k = \sum_m N_m i_m$	Kirchhoff's voltage law: $i \sum_k R_k = \sum_m v_m$
$\sum \phi_k = 0$	Kirchhoff's current law: $\sum_k i_k = 0$

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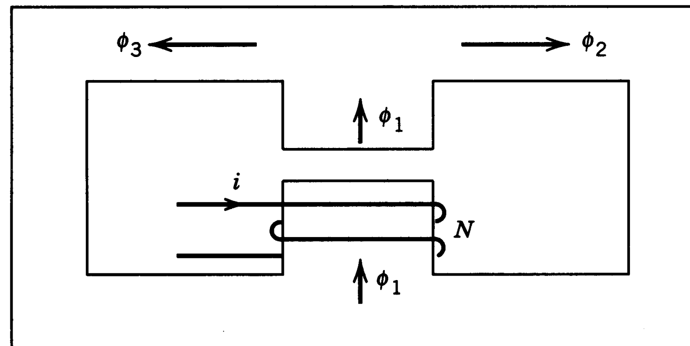
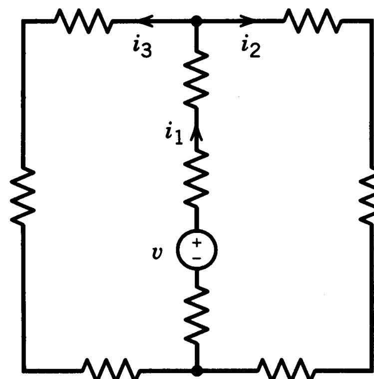
Magnetic Circuit and its Electrical Analog



(a)



(b)

Figure 3-15 (a) Magnetic circuit. (b) An electrical analog.

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Faraday's Law and Lenz's Law

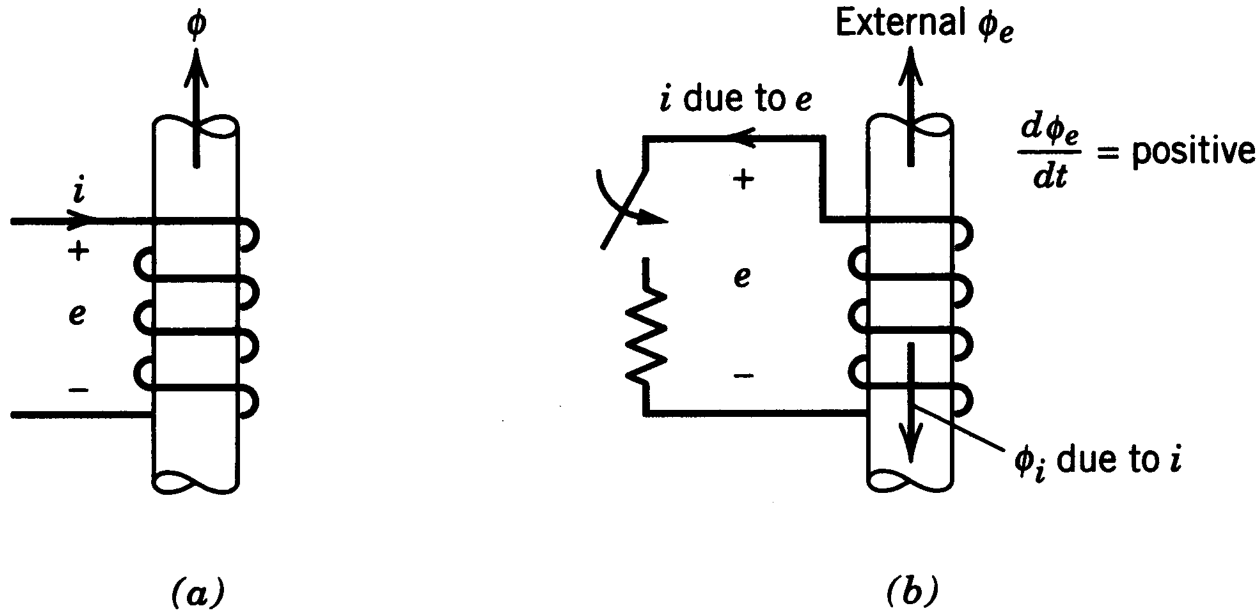

Figure 3-16 (*a*) Flux direction and voltage polarity. (*b*) Lenz's law.

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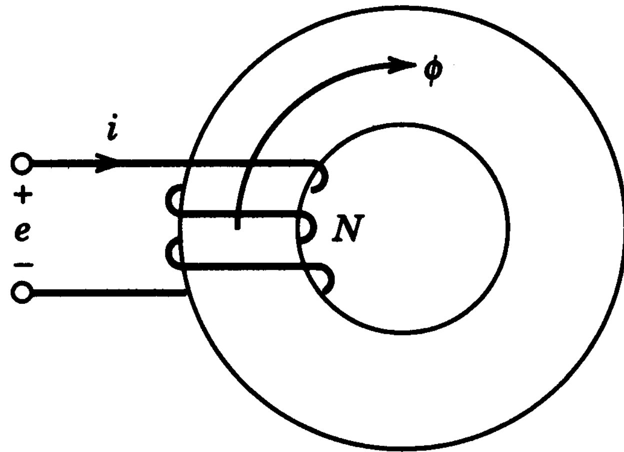
Inductance L



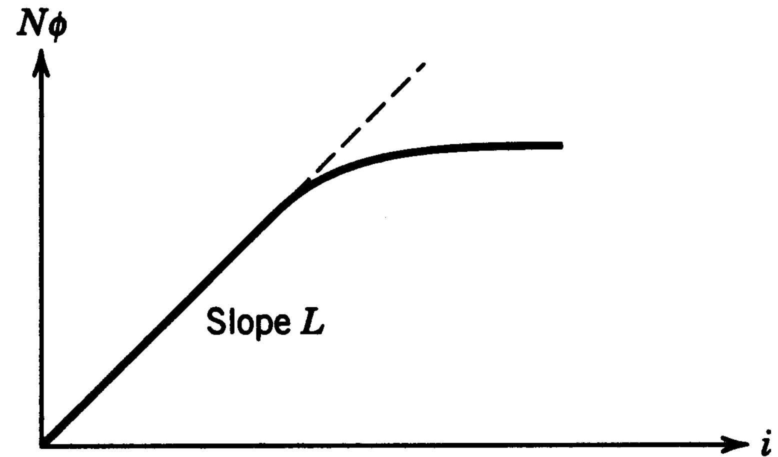


Figure 3-17 Self-inductance L.

- Inductance relates flux-linkage to current

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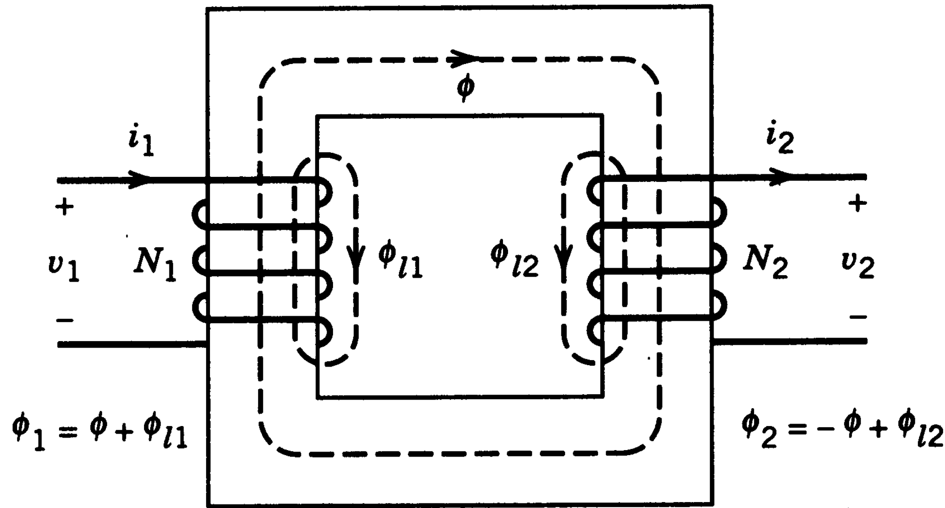
Analysis of a Transformer



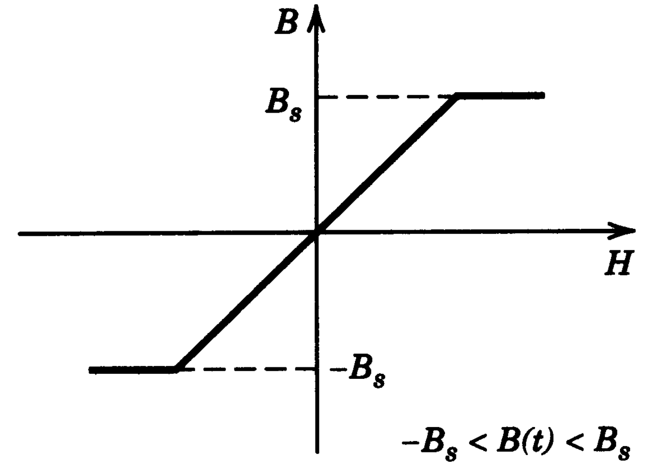


Figure 3-18 (*a*) Cross section of a transformer. (*b*) The *B–H* characteristics of the core.

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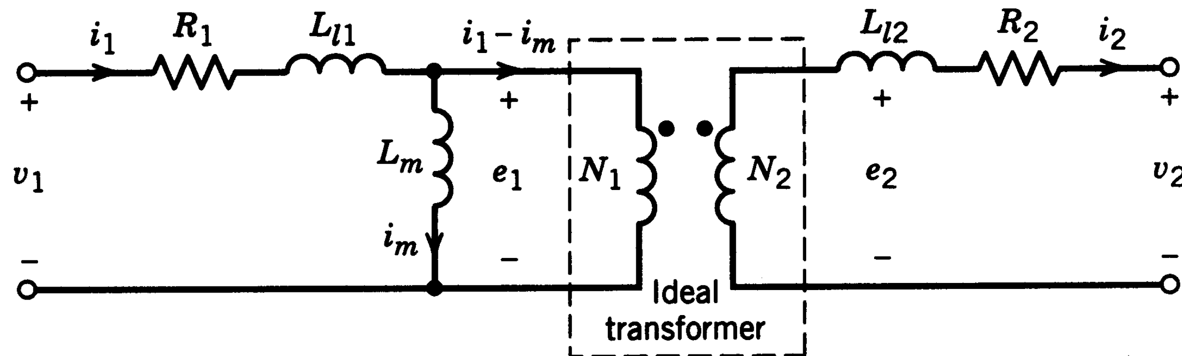
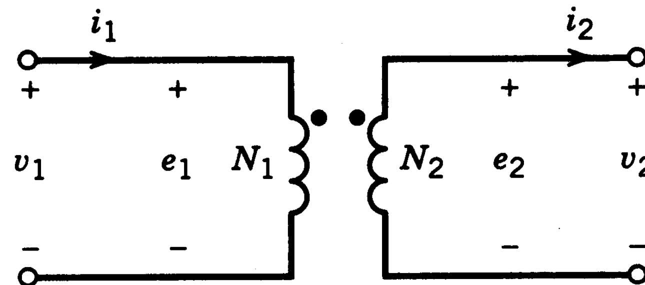
Transformer Equivalent Circuit



(a)



(b)

Figure 3-19 Equivalent circuit for (*a*) a physically realizable transformer wound on a lossless core and (*b*) an ideal transformer.

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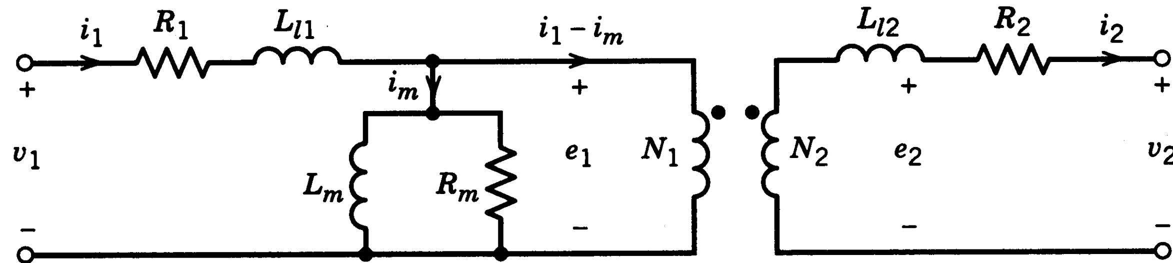
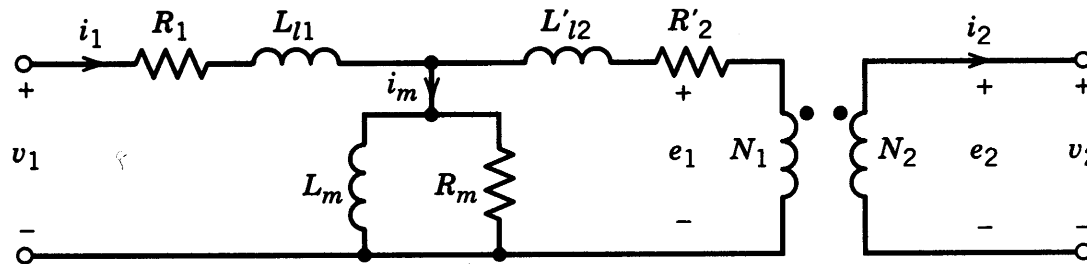
Including the Core Losses



(a)



(b)

Figure 3-21 Equivalent circuit of a transformer including the effects of hysteresis loss. (*a*) Circuit components are on both sides (coil 1 and coil 2 sides) of the ideal transformer. (*b*) Components from the secondary (coil 2) side are reflected across the ideal transformer to the primary (coil 1) side.

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Transformer Core Characteristic

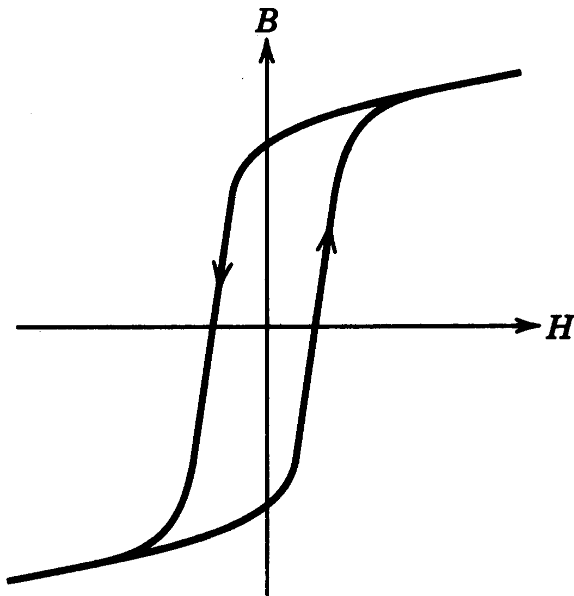

Figure 3-20 *B–H* characteristic of a transformer core having hysteresis and hence magnetic losses.

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Chapter 4
Computer Simulation

Chapter 4 Computer Simulation of Power Electronic Converters and Systems **61**

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4-7 Equation Solvers 72
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System to be Simulated

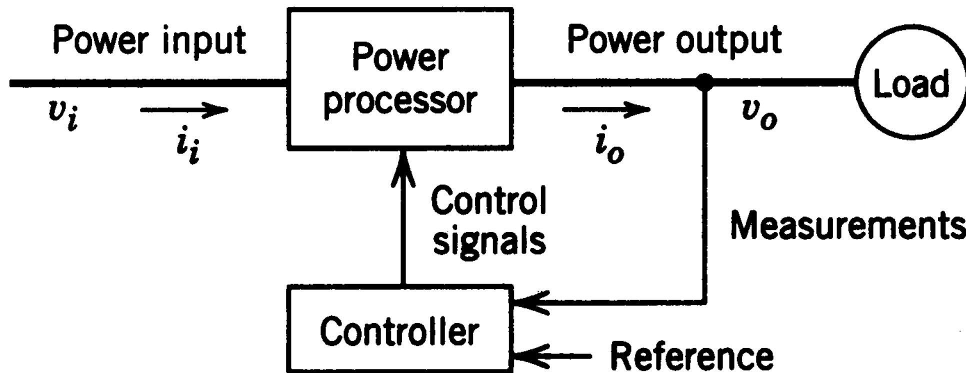

Figure 4-1 Power electronics system: a block diagram.

- Challenges in modeling power electronic systems

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Large-Signal System Simulation

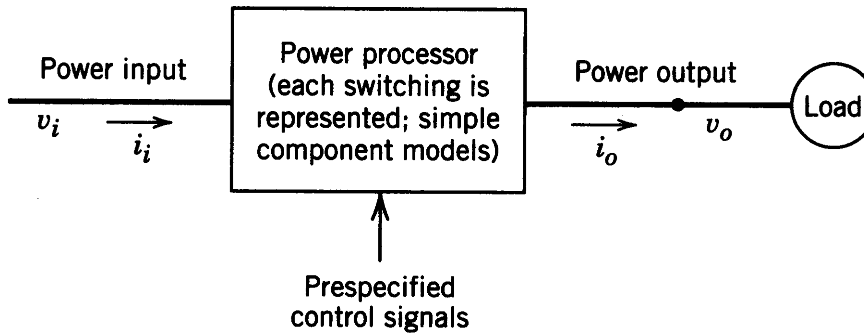

Figure 4-2 Open-loop, large-signal simulation.

- Simplest component models

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Small-Signal Linearized Model for Controller Design

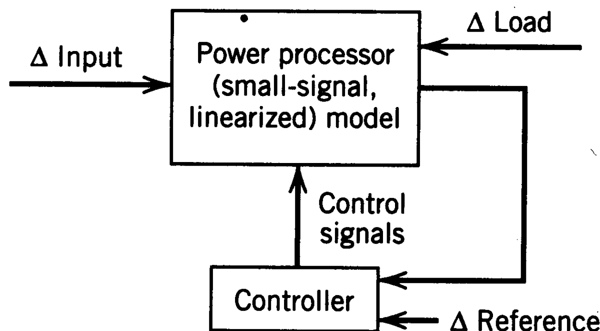

Figure 4-3 Small-signal (linear) model and controller design.

- System linearized around the steady-state point

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Closed-Loop Operation: Large Disturbances

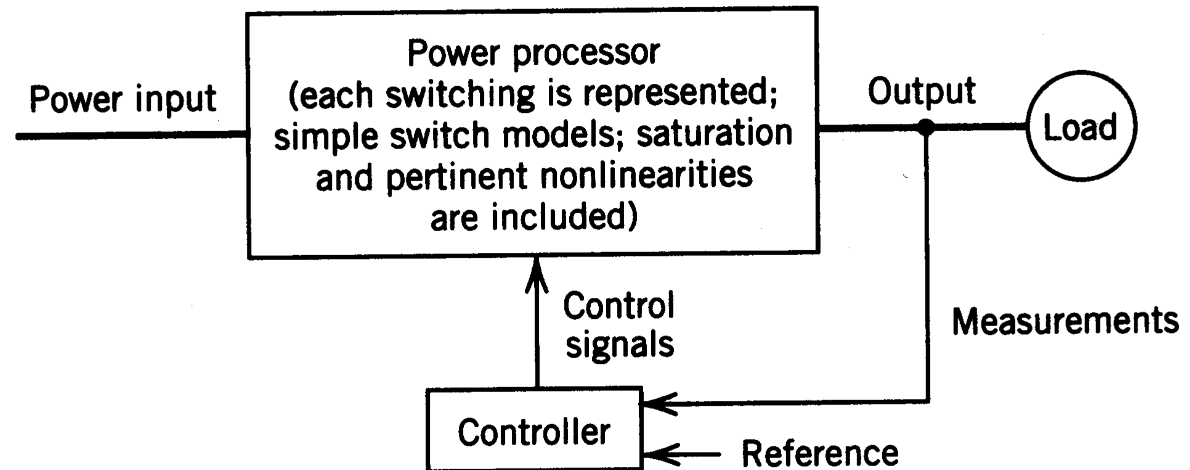

Figure 4-4 Closed-loop, large-signal system behavior.

- Simplest component models
- Nonlinearities, Limits, etc. are included

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Modeling of Switching Operation

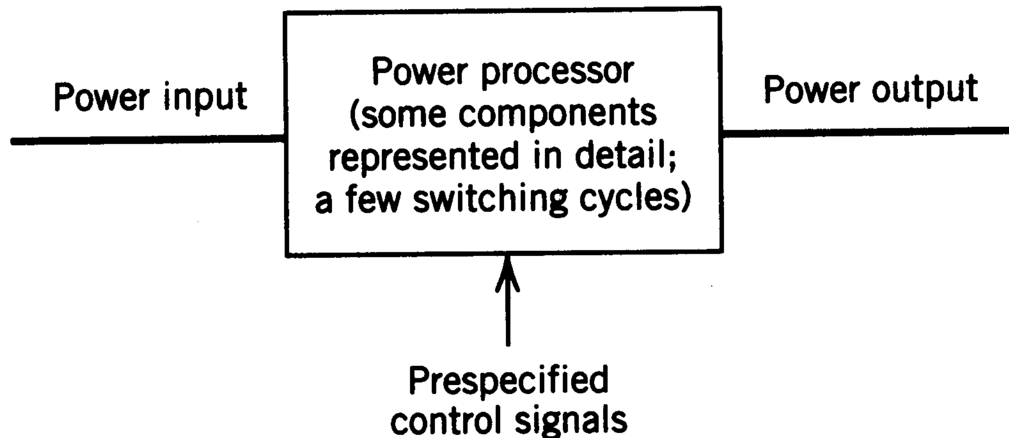

Figure 4-5 Switching details.

- Detailed device models
- Just a few switching cycles are studied

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Modeling of a Simple Converter

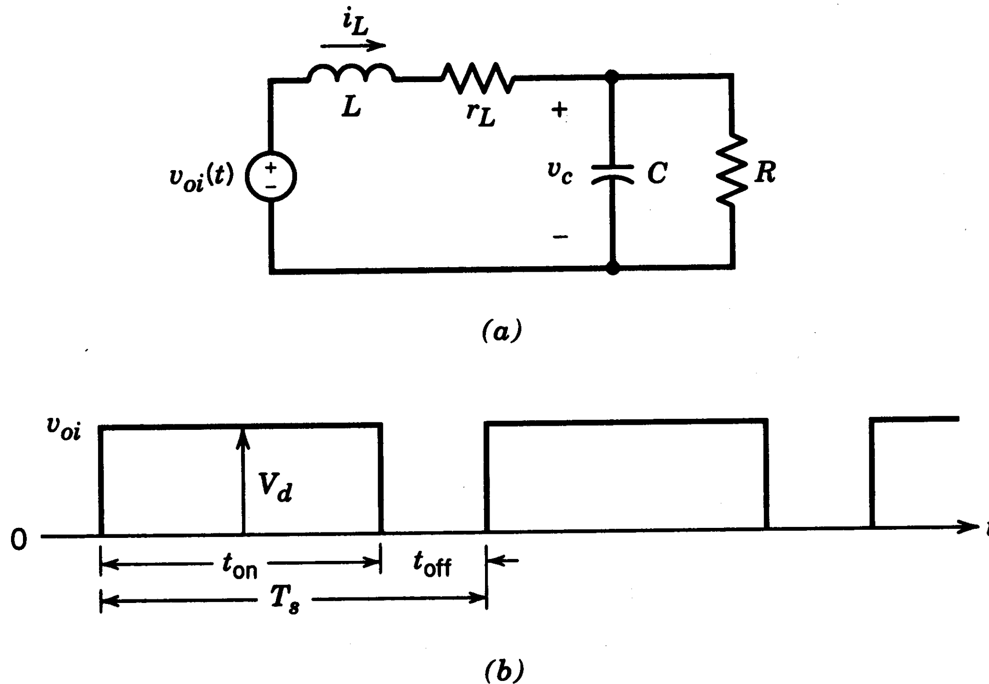

Figure 4-6 Simplified equivalent circuit of a switch-mode, regulated dc power supply (same as in Fig. 1-3).

- Input voltage takes on two discrete values

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Trapezoidal Method of Integration

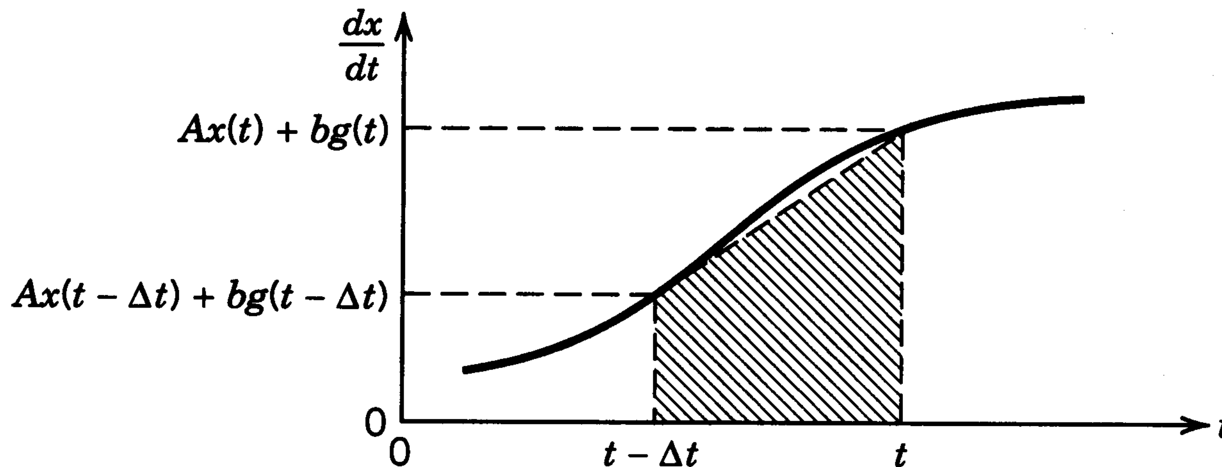

Figure 4-7
Trapezoidal method of integration.

- The area shown above represents the integral

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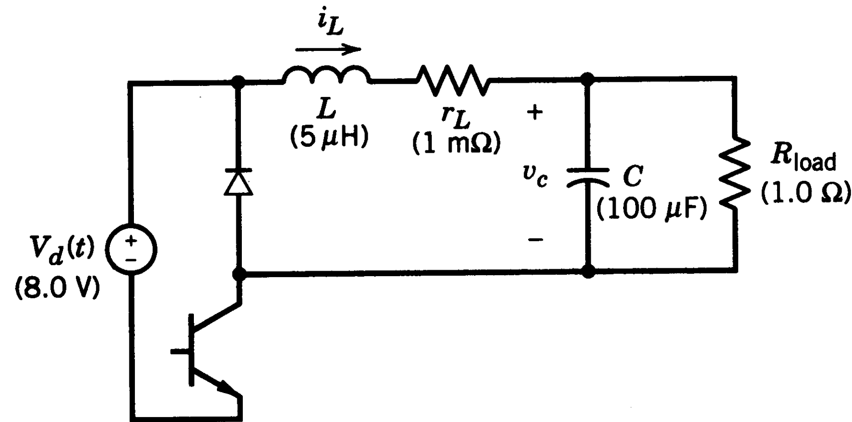
A Simple Example



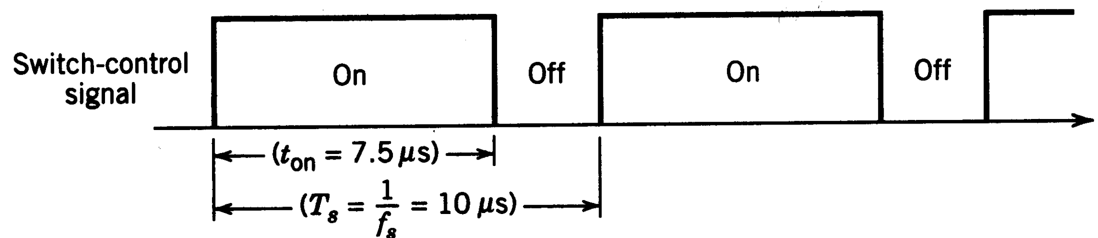


Figure 4-8 (a) Circuit for simulation. (b) Switch control waveform.

- The input voltage takes on two discrete values

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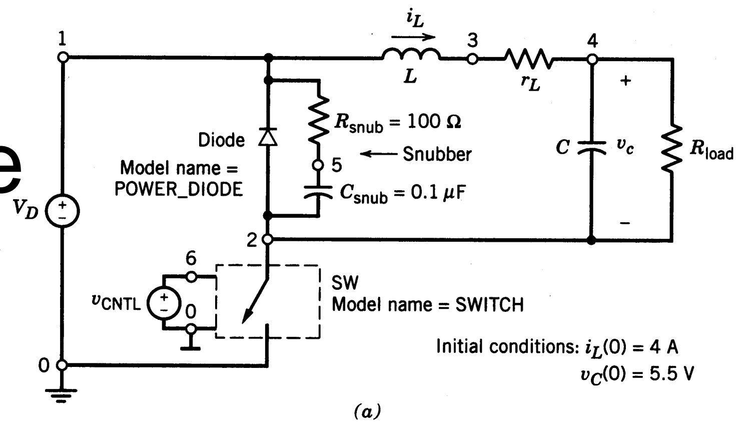
Modeling using PSpice




```
PSpice Example
*
DIODE   2  1  POWER_DIODE
Rsnub   1  5  100.0
Csnub   5  2  0.1uF
*
SW      2  0  6  0  SWITCH
VCNTL   6  0  PULSE(0V,1V,0s,1ns,1ns,7.5us,10us)
*
L       1  3  5uH   IC=4A
rL      3  4  1m
C       4  2  100uF IC=5.5V
RLOAD   4  2  1.0
*
VD      1  0  8.0V
*
.MODEL POWER_DIODE D(RS=0.01,CJO=10pF)
.MODEL SWITCH VSWITCH(RON=0.01)
.TRAN  10us  500.0us  0s  0.2us  uic
.PROBE
.END
```

(b)

Figure 4-9 PSpice simulation of circuit in Fig. 4-8.

- Schematic approach is far superior

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PSpice-based Simulation

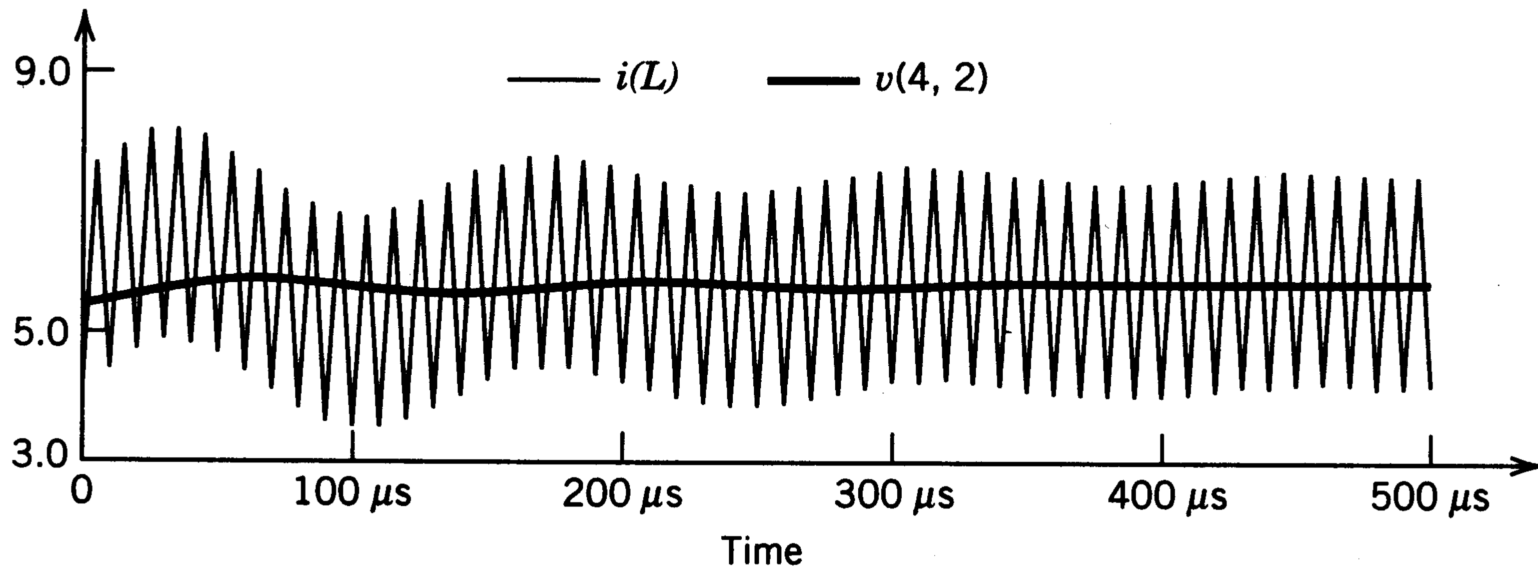

Figure 4-10 Results of PSpice simulation: i_L and v_c.

- Simulation results

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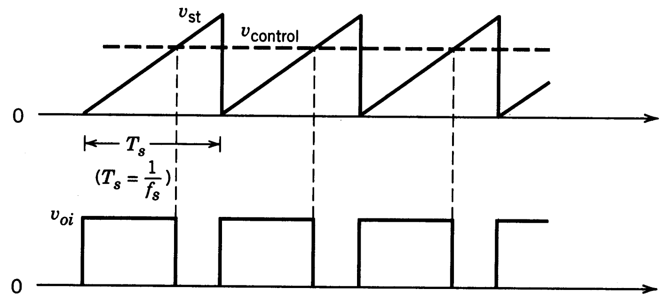
Simulation using MATLAB



(a)

```
% Solution of the Circuit in Fig. 4-6 using Trapezoidal Method of Integration.
clc,clg,clear
% Input Data
Vd=8; L=5e-6; C=100e-6; rL=1e-3; R=1.0; fs=100e3; Vcontrol=0.75;
Ts=1/fs; tmax=50*Ts; deltat=Ts/50;
%
time= 0:deltat:tmax;
vst= time/Ts - fix(time/Ts);
voi= Vd * (Vcontrol > vst);
%
A=[-rL/L -1/L; 1/C -1/(C*R)];
b=[1/L 0]';
MN=inv(eye(2) - deltat/2 * A);
M=MN * (eye(2)+ deltat/2 * A);
N=MN * deltat/2 * b;
%
iL(1)=4.0; vC(1)=5.5;
timelength=length(time);
%
for k = 2:timelength
x = M * [iL(k-1) vC(k-1)]' + N * (voi(k) + voi(k-1));
iL(k) = x(1); vC(k) = x(2);
end
%
plot(time,iL,time,vC)
meta Example
```

(b)

Figure 4-11 MATLAB simulation of circuit in Fig. 4-6.

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MATLAB-based Simulation

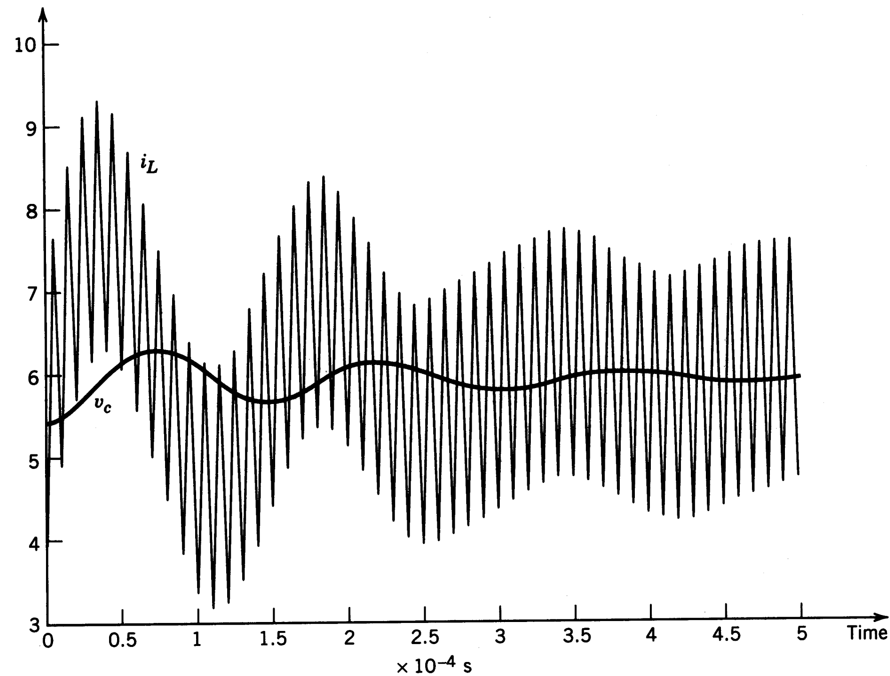

Figure 4-12 MATLAB simulation results.

- Simulation results

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Chapter 5

Diode Rectifiers

Chapter 5 Line-Frequency Diode Rectifiers: Line-Frequency ac → Uncontrolled dc 79

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5-2 Basic Rectifier Concepts 80
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5-4 Voltage-Doubler (Single-Phase) Rectifiers 100
5-5 Effect of Single-Phase Rectifiers on Neutral Currents in Three-Phase, Four-Wire Systems 101
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Diode Rectifier Block Diagram

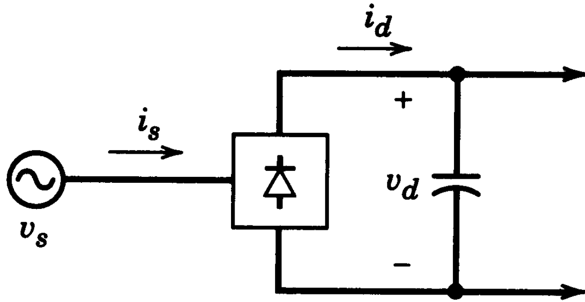

Figure 5-1 Block diagram of a rectifier.

- Uncontrolled utility interface (ac to dc)

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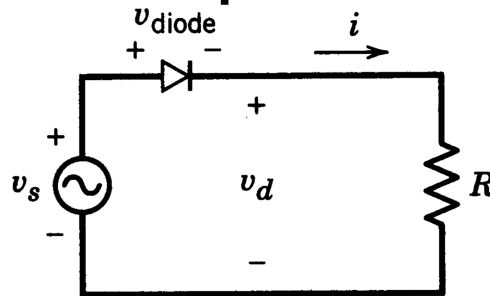
A Simple Circuit



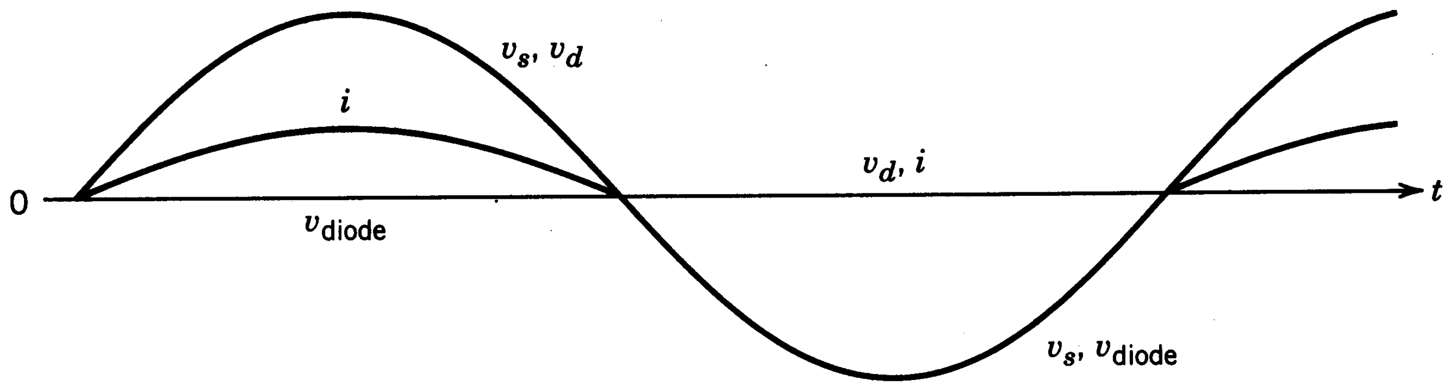


Figure 5-2 Basic rectifier with a load resistance.

- Resistive load

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A Simple Circuit (*R-L* Load)

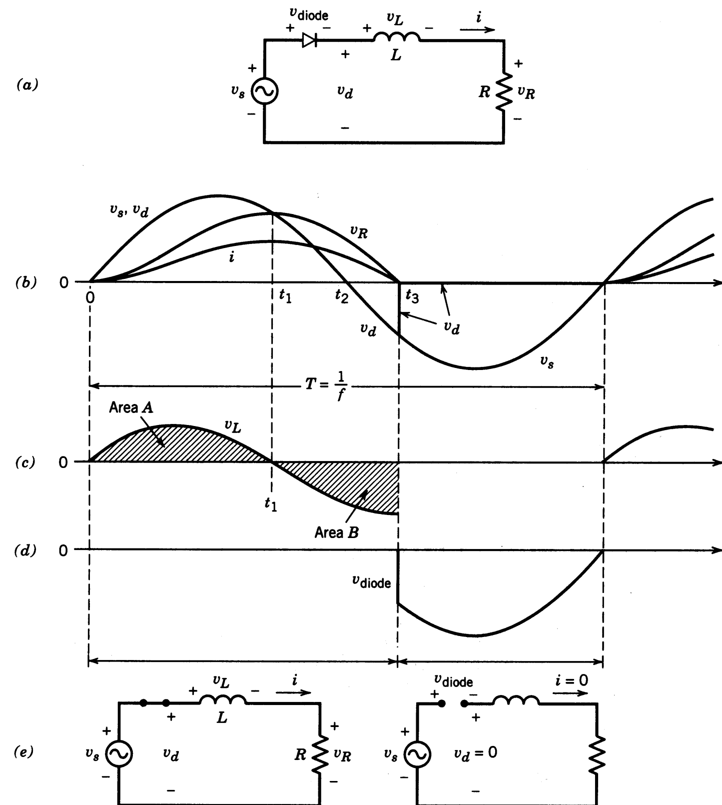

Figure 5-3 Basic rectifier with an inductive load.

- Current continues to flows for a while even after the input voltage has gone negative

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A Simple Circuit (Load has a dc back-emf)

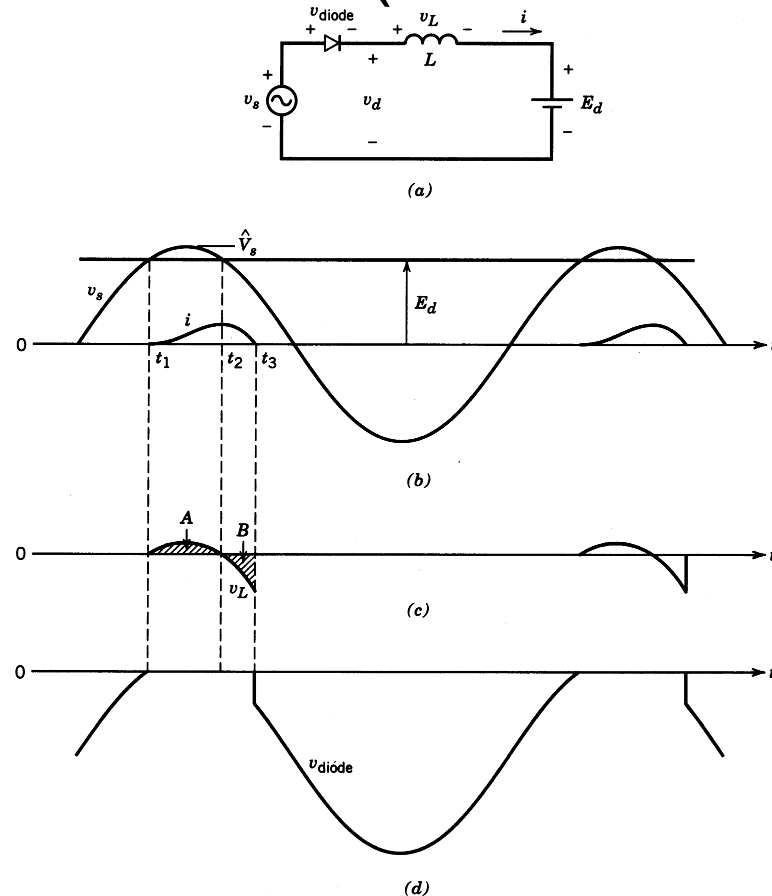

Figure 5-4 Basic rectifier with an internal dc voltage.

- Current begins to flow when the input voltage exceeds the dc back-emf
- Current continues to flows for a while even after the input voltage has gone below the dc back-emf

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Single-Phase Diode Rectifier Bridge

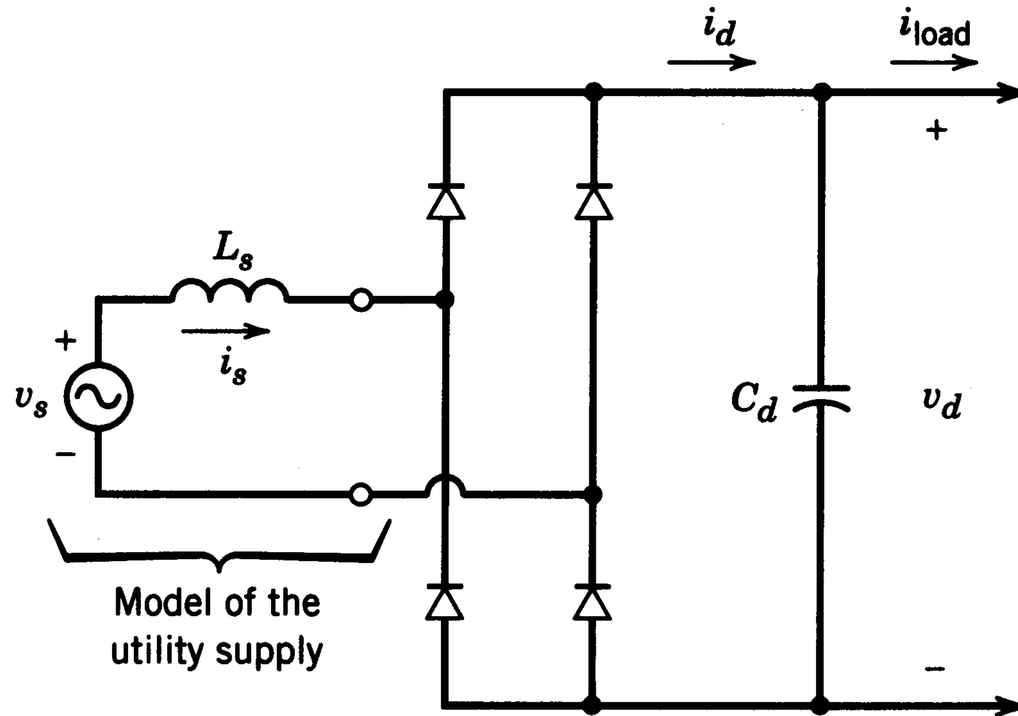

Figure 5-5 Single-phase diode bridge rectifier.

- Large capacitor at the dc output for filtering and energy storage

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Diode-Rectifier Bridge Analysis

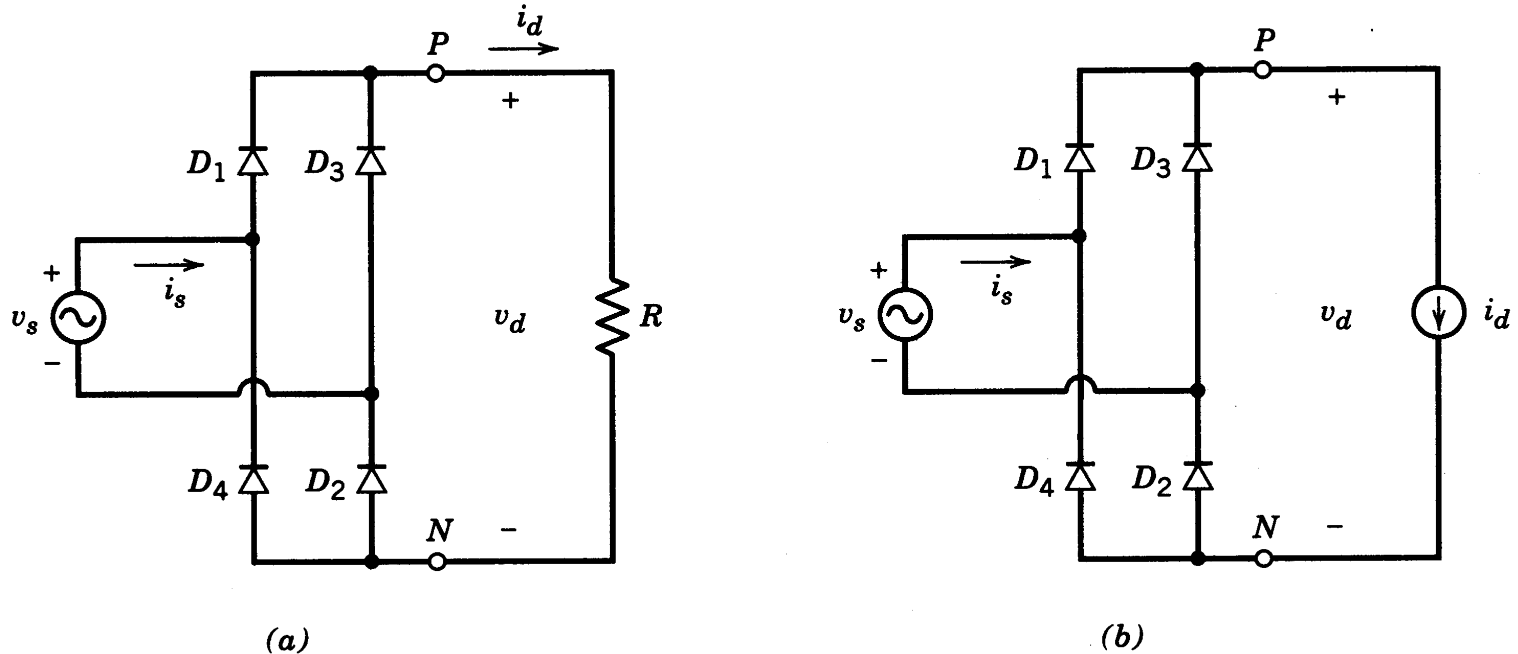

Figure 5-6 Idealized diode bridge rectifiers with $L_s = 0$.

- Two simple (idealized) cases to begin with

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Redrawing Diode-Rectifier Bridge

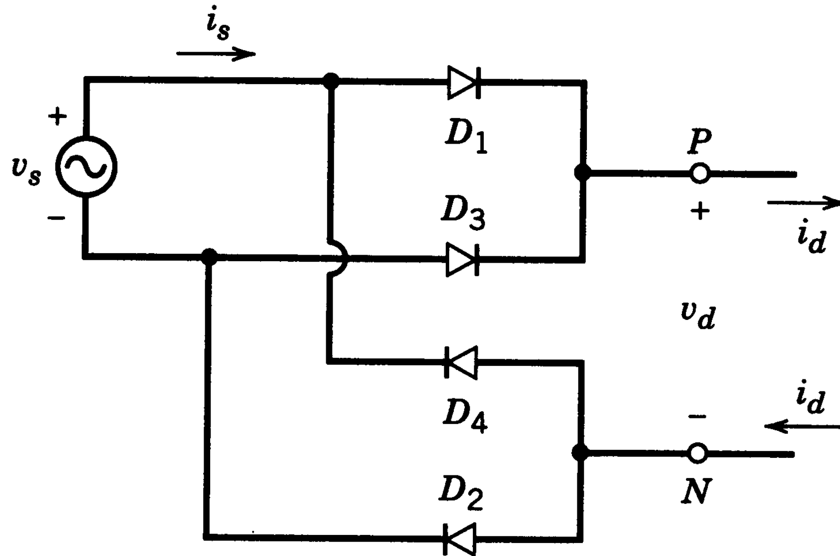

Figure 5-7 Redrawn rectifiers of Fig. 5-6.

- Two groups, each with two diodes

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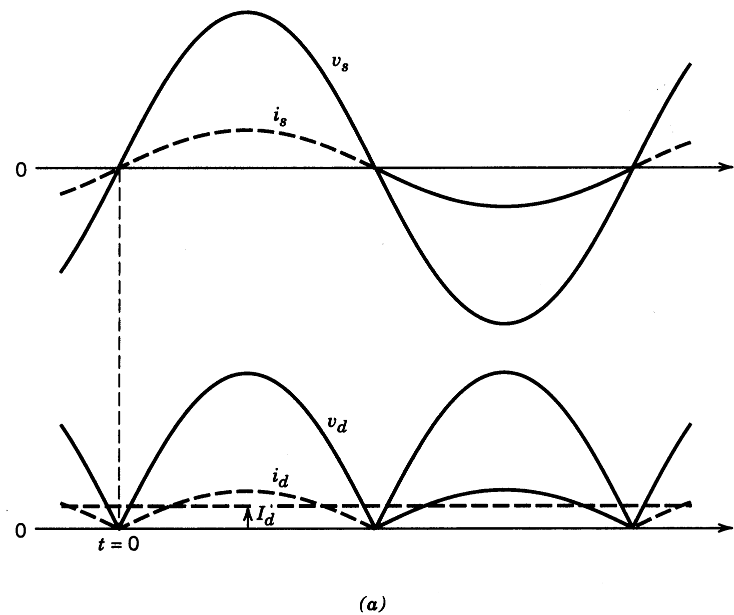
Waveforms with a purely resistive load and a purely dc current at the output



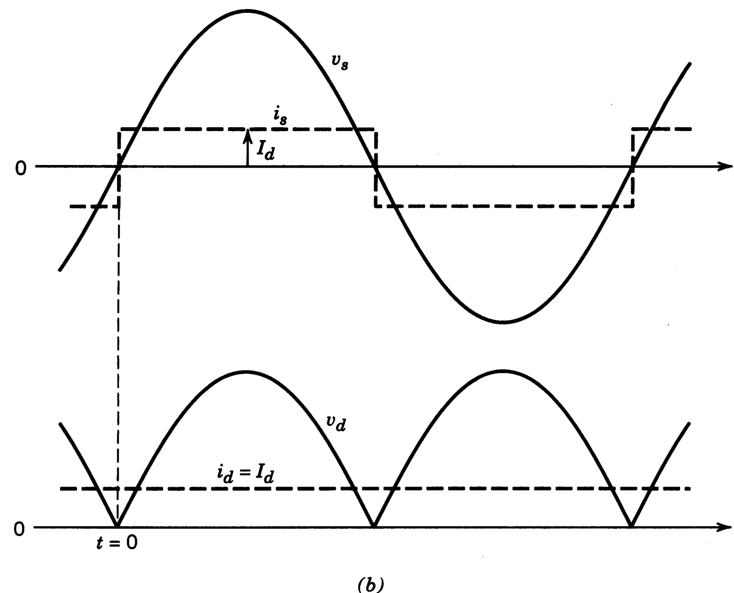


Figure 5-8 Waveforms in the rectifiers of (*a*) Fig. 5-6*a* and (*b*) Fig. 5-6*b*.

- In both cases, the dc-side voltage waveform is the same

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Diode-Rectifier Bridge Input Current

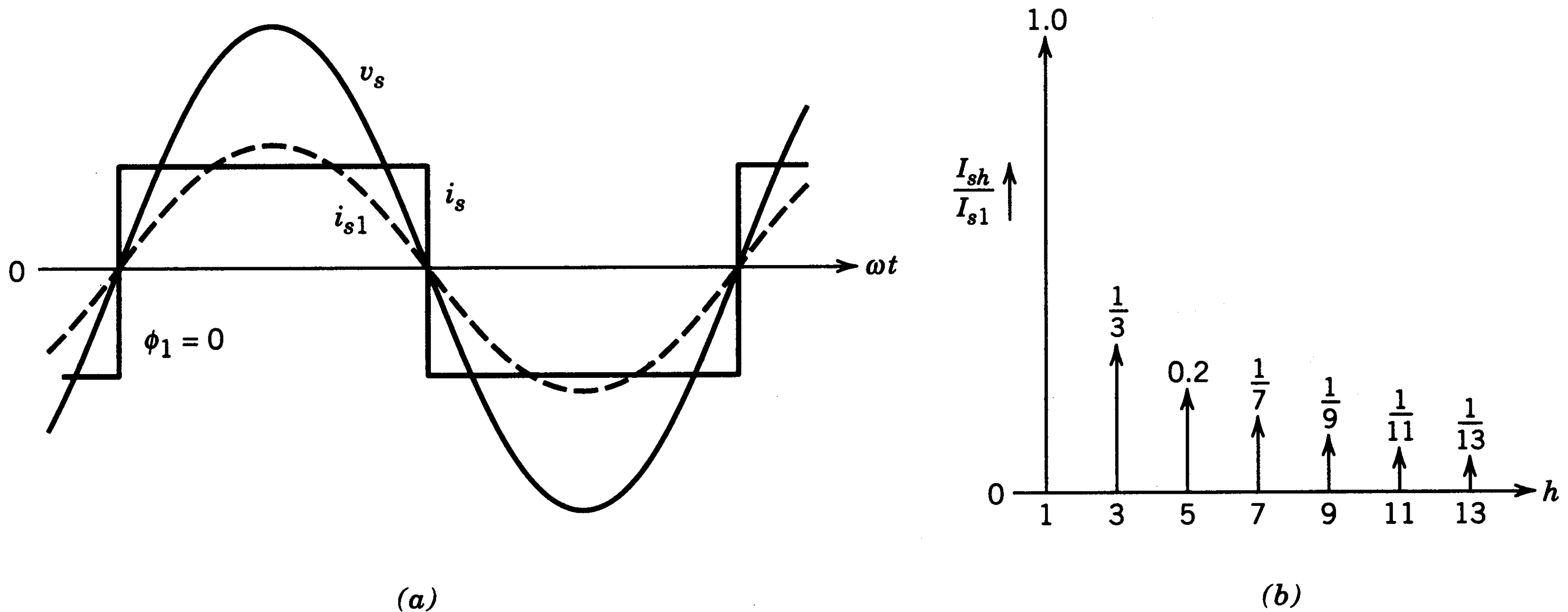


Figure 5-9 Line current i_s in the idealized case.

- Idealized case with a purely dc output current

Diode-Rectifier Bridge Analysis with AC-Side Inductance

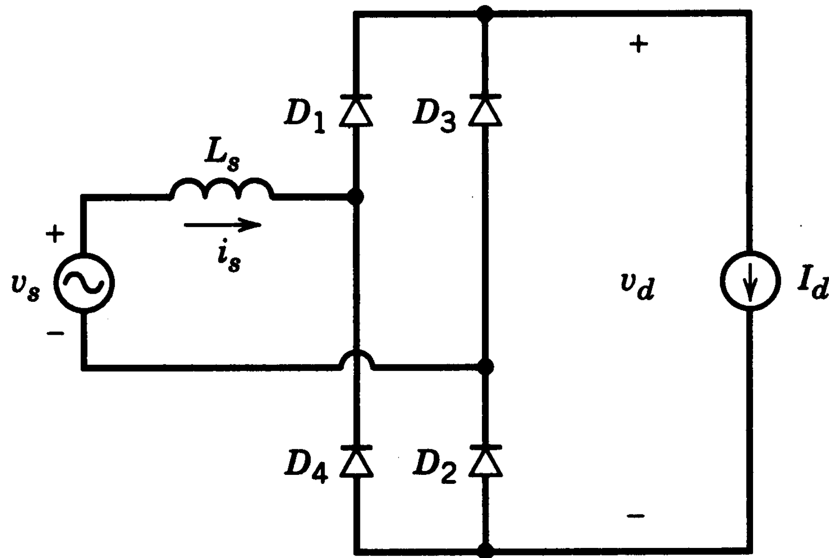
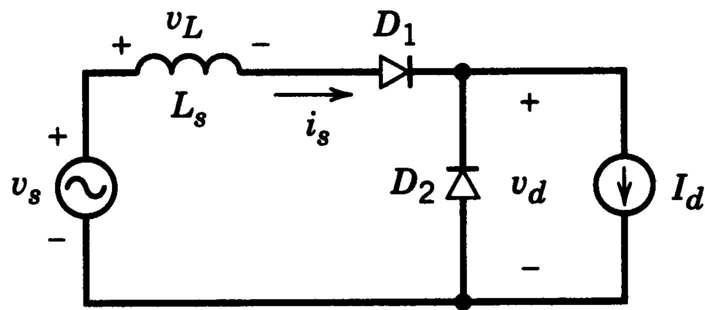


Figure 5-10 Single-phase rectifier with L_s.

- Output current is assumed to be purely dc

Understanding Current Commutation



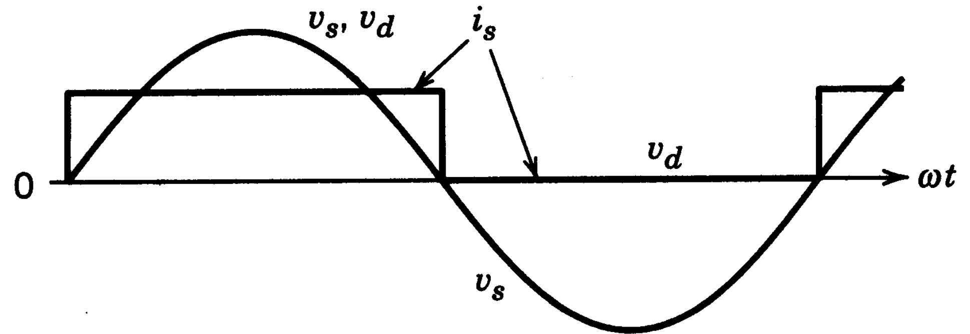


Figure 5-11 Basic circuit to illustrate current commutation. Waveforms assume $L_s = 0$.

- Assuming inductance in this circuit to be zero

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Understanding Current Commutation (cont.)

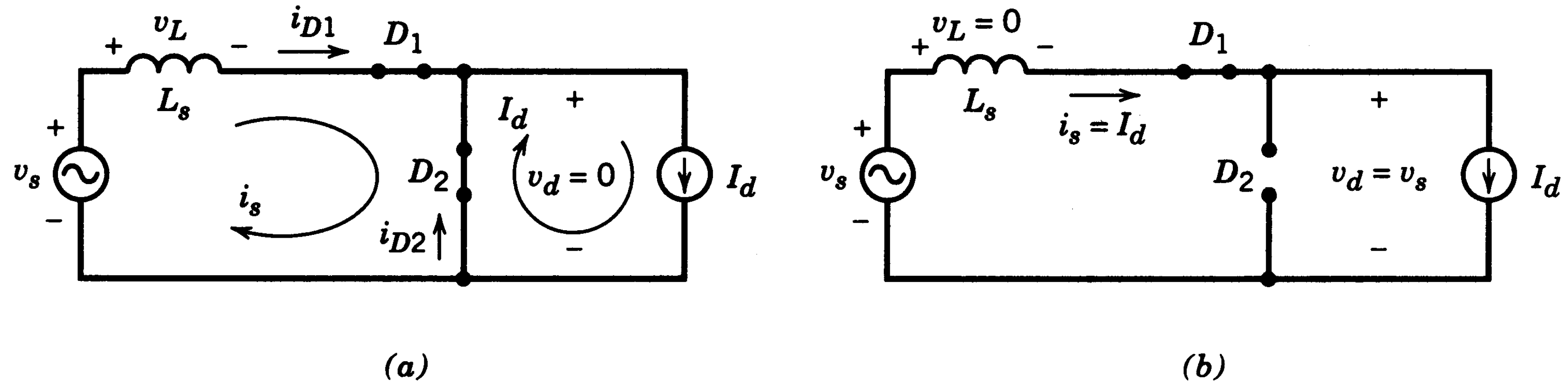

Figure 5-12 (*a*) Circuit during the commutation. (*b*) Circuit after the current commutation is completed.

- Inductance in this circuit is included

Current Commutation Waveforms

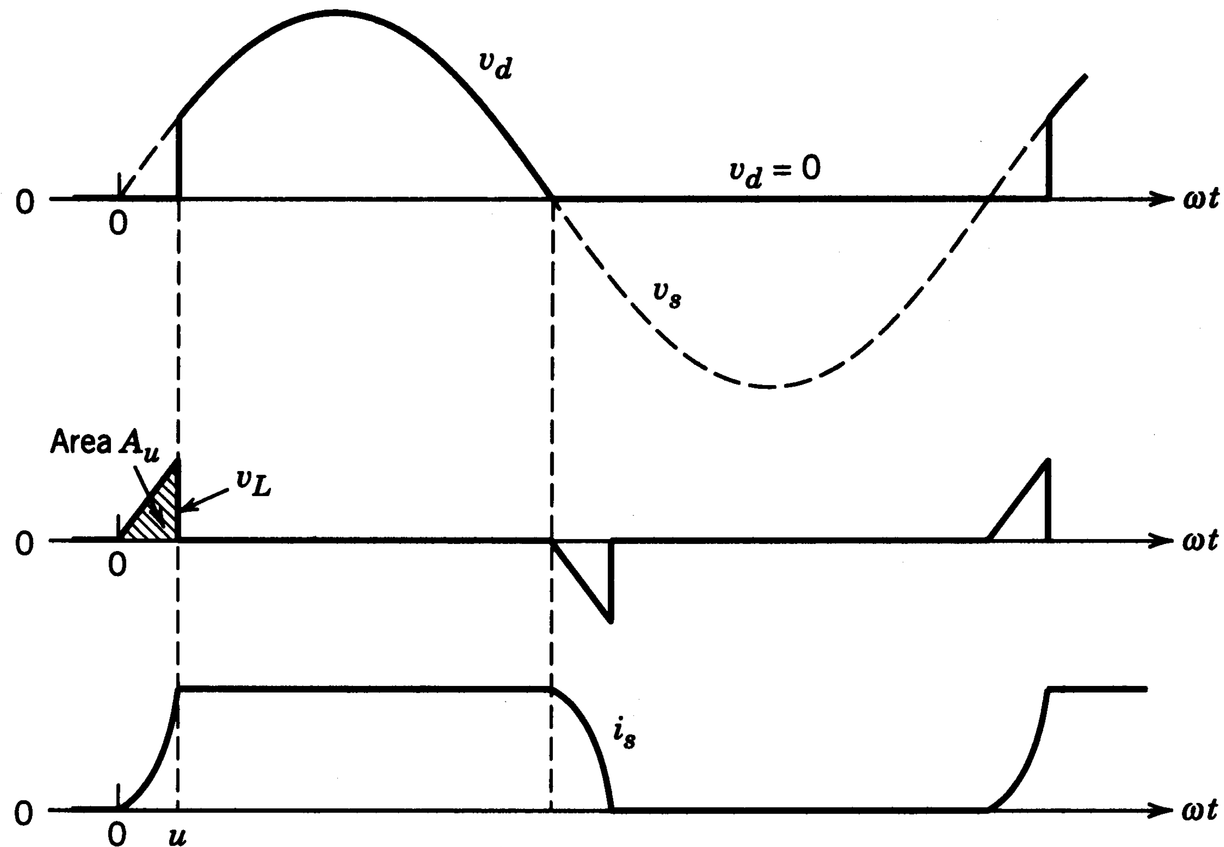

Figure 5-13 Waveforms in the basic circuit of Fig. 5-11. Note that a large value of L_s is used to clearly show the commutation interval.

- Shows the volt-seconds needed to commutate current

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Current Commutation in Full-Bridge Rectifier

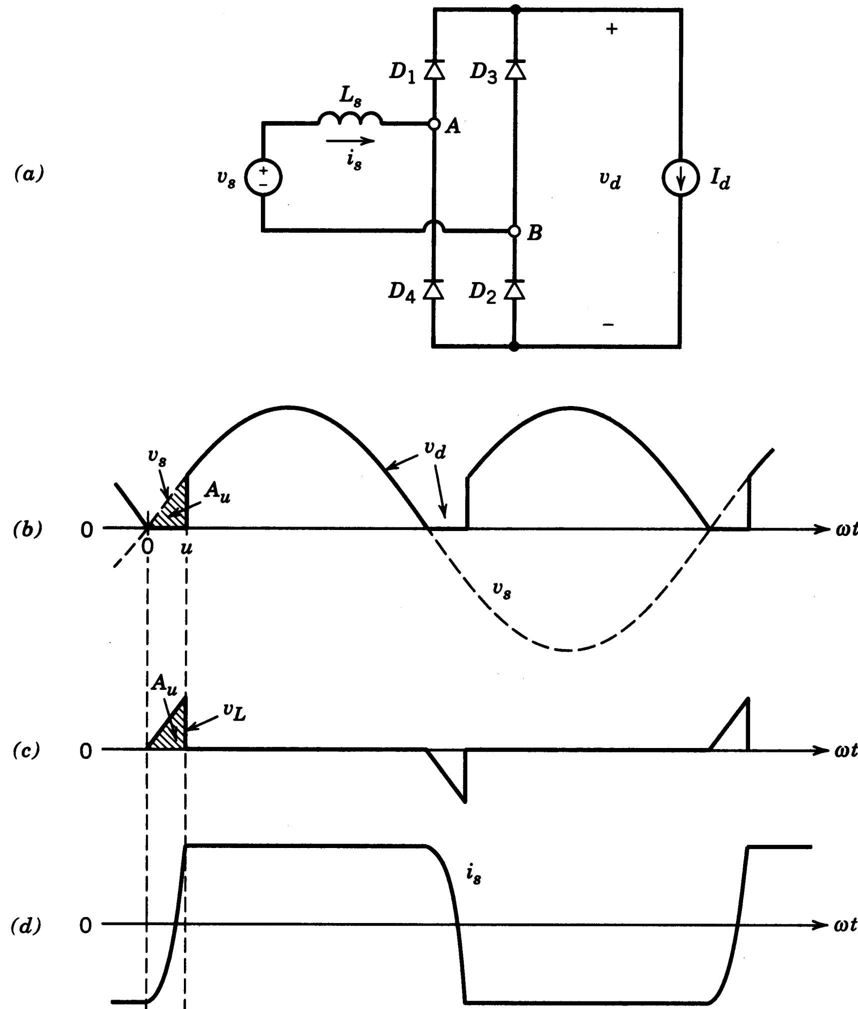

Figure 5-14 (*a*) Single-phase diode rectifier with L_s. (*b*) Waveforms.

- Shows the necessary volt-seconds

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Understanding Current Commutation

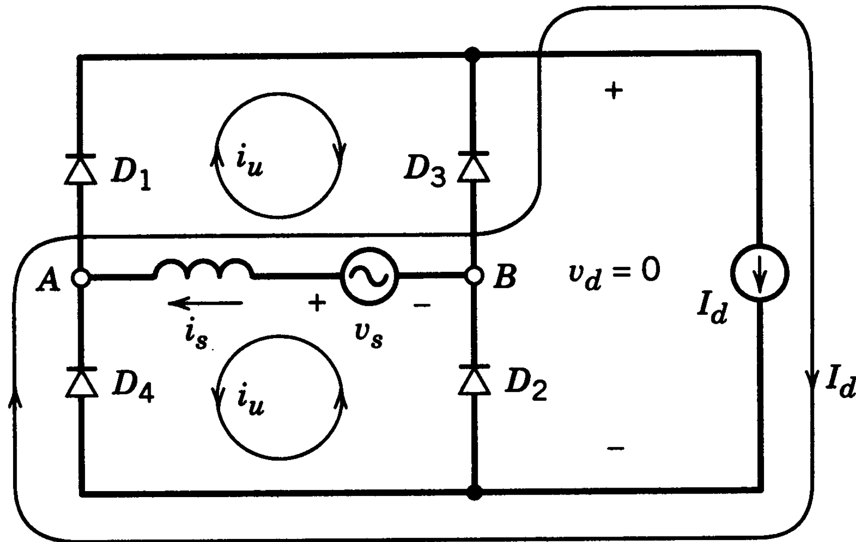
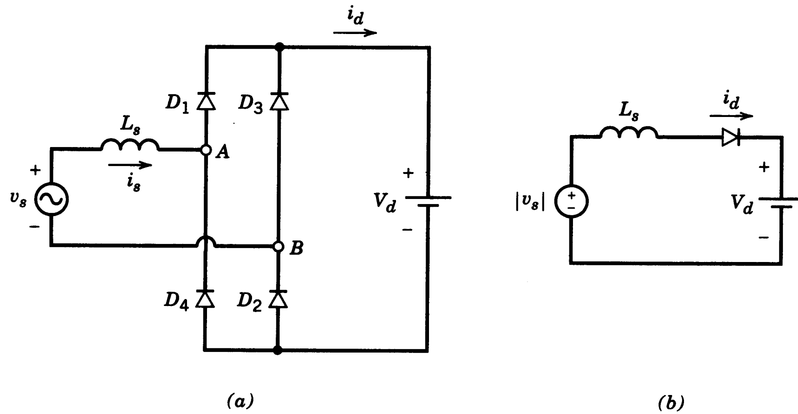


Figure 5-15 Redrawn circuit of Fig. 5-14*a* during current commutation.

- Note the current loops for analysis

Rectifier with a dc-side voltage



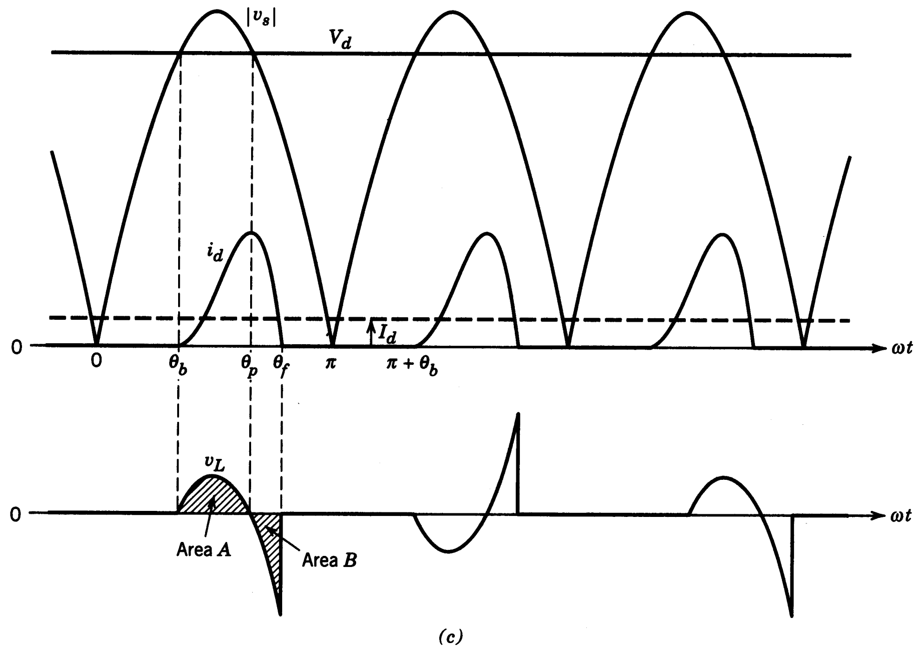


Figure 5-16 (*a*) Rectifier with a constant dc-side voltage. (*b*) Equivalent circuit. (*c*) Waveforms.

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DC-Side Voltage and Current Relationship

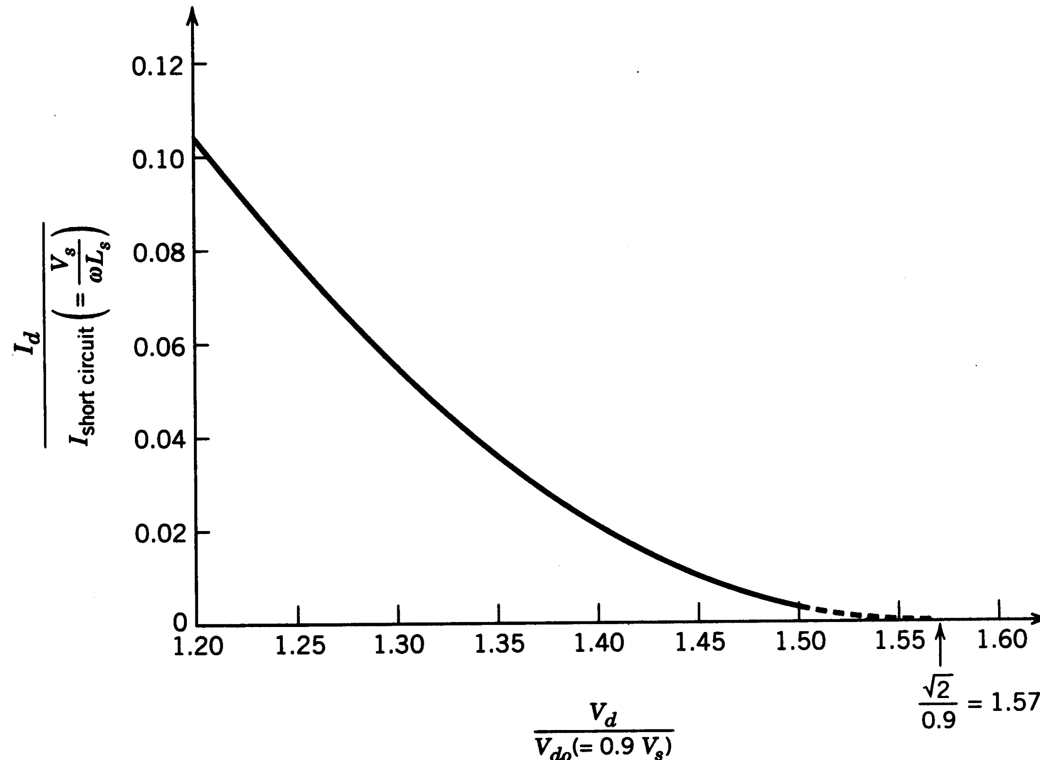

Figure 5-17 Normalized I_d versus V_d in the rectifier of Fig. 5-16*a* with a constant dc-side voltage.

- Zero current corresponds to dc voltage equal to the peak of the input ac voltage

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Effect of DC-Side Current on THD, PF and DPF

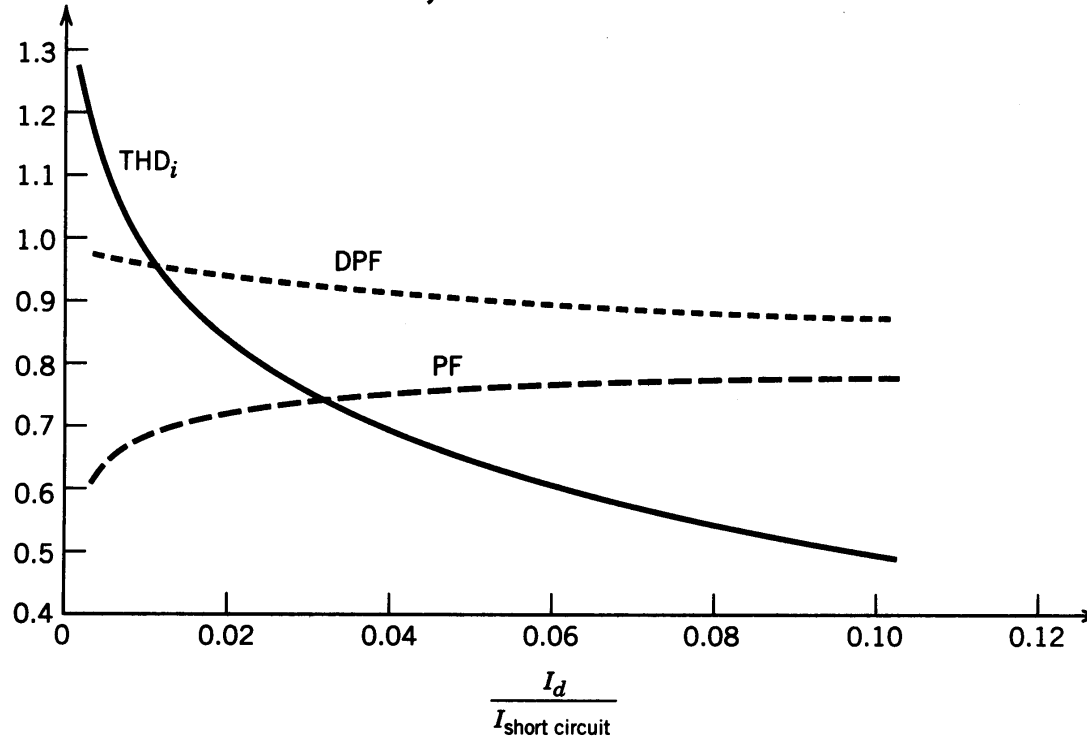

Figure 5-18 Total harmonic distortion, DPF, and PF in the rectifier of Fig. 5-16*a* with a constant dc-side voltage.

- Very high THD at low current values

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Crest Factor versus the Current Loading

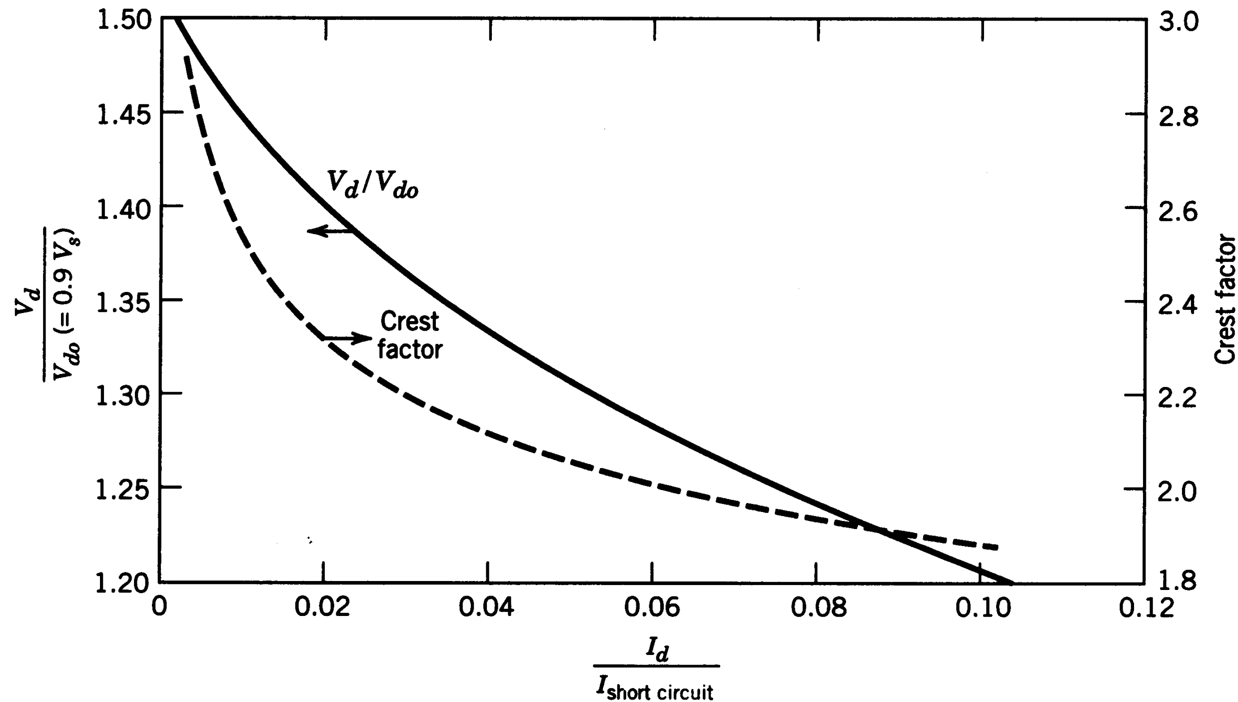

Figure 5-19 Normalized V_d and the crest factor in the rectifier of Fig. 5-16*a* with a constant dc-side voltage.

- The Crest Factor is very high at low values of current

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Diode-Rectifier with a Capacitor Filter

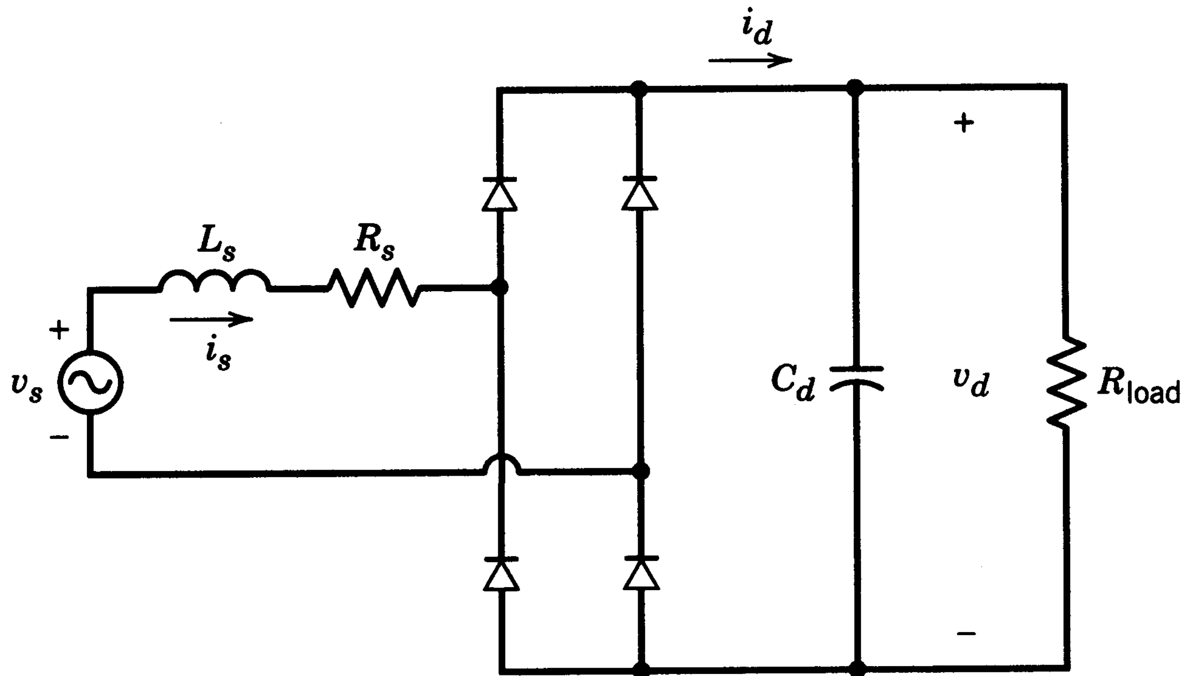

Figure 5-20 Practical diode–bridge rectifier with a filter capacitor.

- Power electronics load is represented by an equivalent load resistance

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Diode Rectifier Bridge

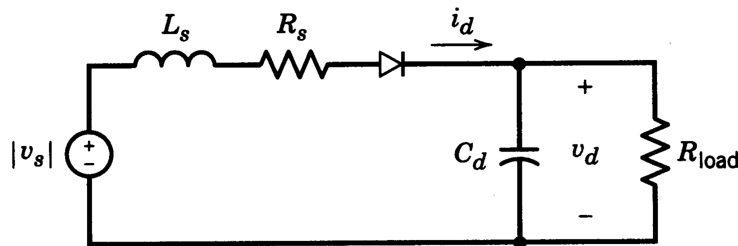

Figure 5-21 Equivalent circuit of Fig. 5-20.

- Equivalent circuit for analysis on one-half cycle basis

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Diode-Bridge Rectifier: Waveforms

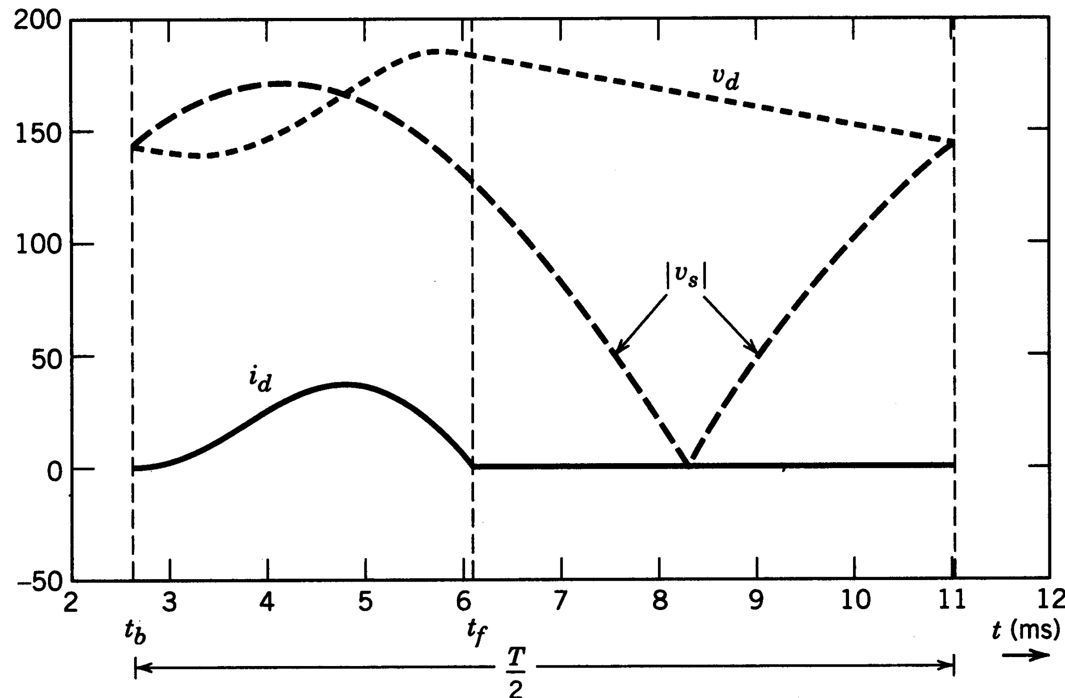

Figure 5-22 Waveforms in the circuit of Fig. 5-20, obtained in Example 5-1.

- Analysis using MATLAB

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Diode-Bridge Rectifier: Waveforms

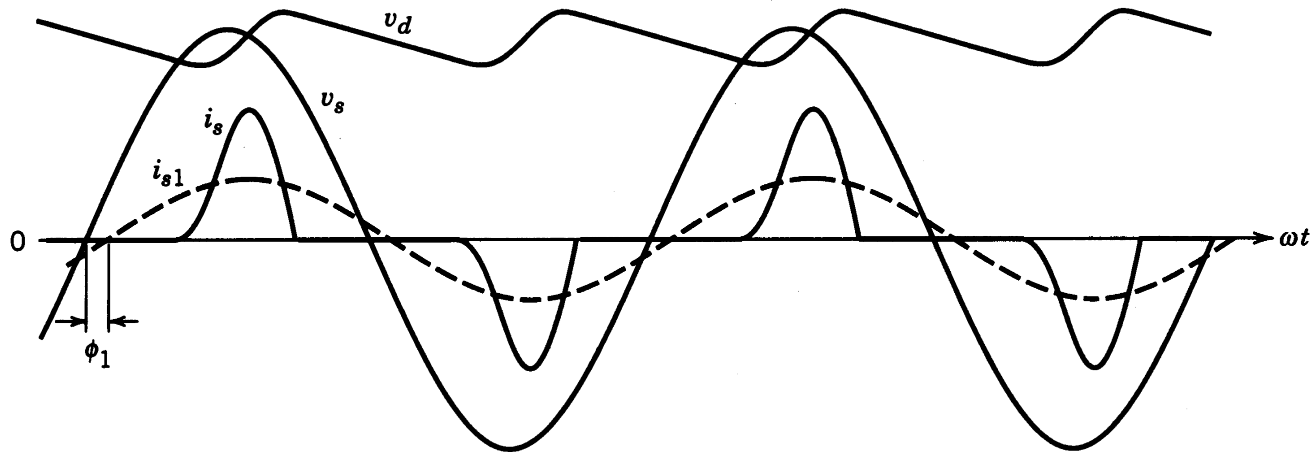

Figure 5-23 Waveforms in the circuit of Fig. 5-20, obtained in Example 5-2.

- Analysis using PSpice

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Input Line-Current Distortion

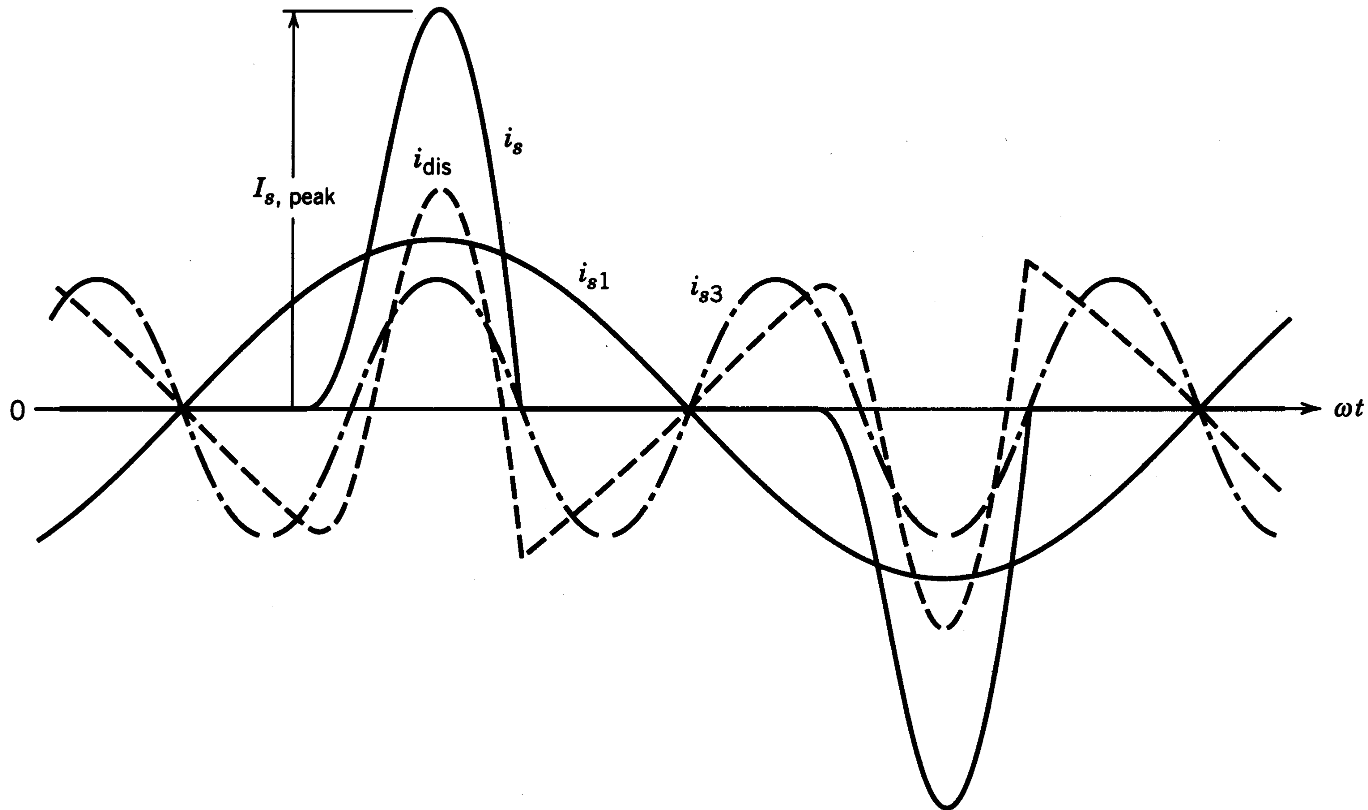

Figure 5-24 Distorted line current in the rectifier of Fig. 5-20.

- Analysis using PSpice

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Line-Voltage Distortion

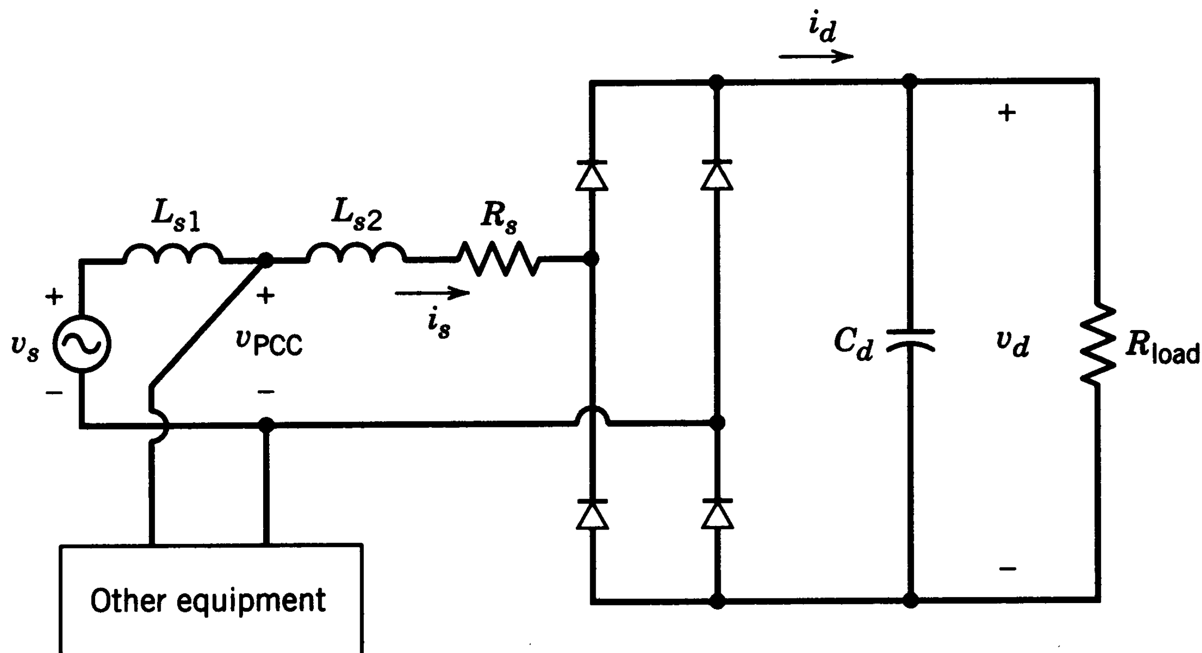

Figure 5-25 Line-voltage notching and distortion.

- PCC is the point of common coupling

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Line-Voltage Distortion

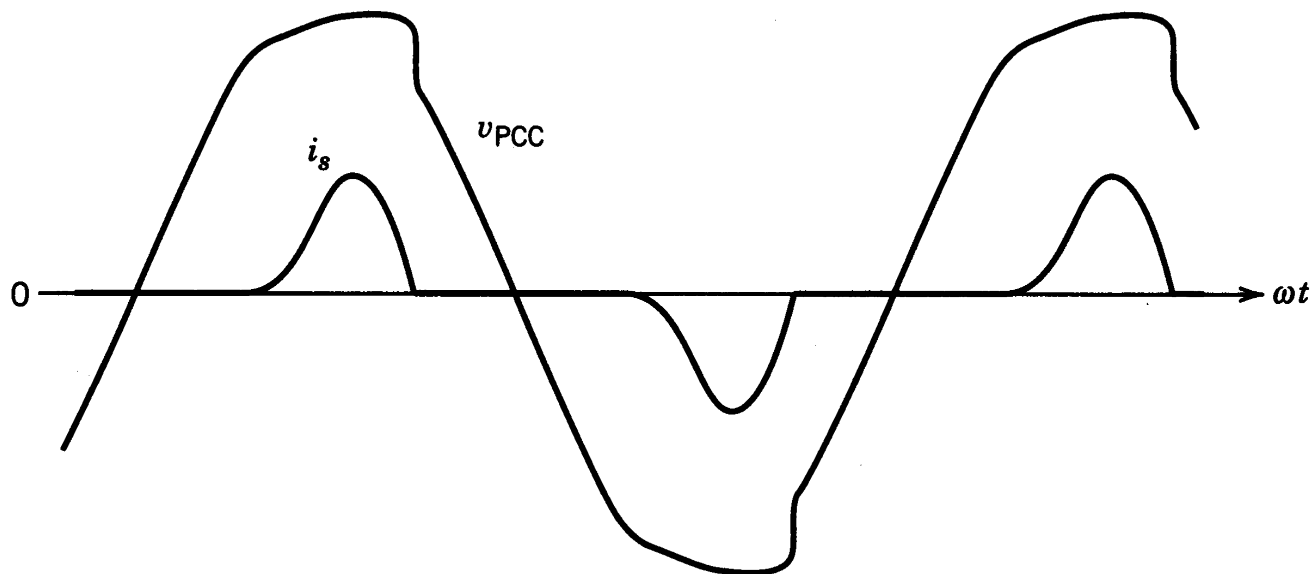

Figure 5-26 Voltage waveform at the point of common coupling in the circuit of Fig. 5-25.

- Distortion in voltage supplied to other loads

Voltage Doubler Rectifier

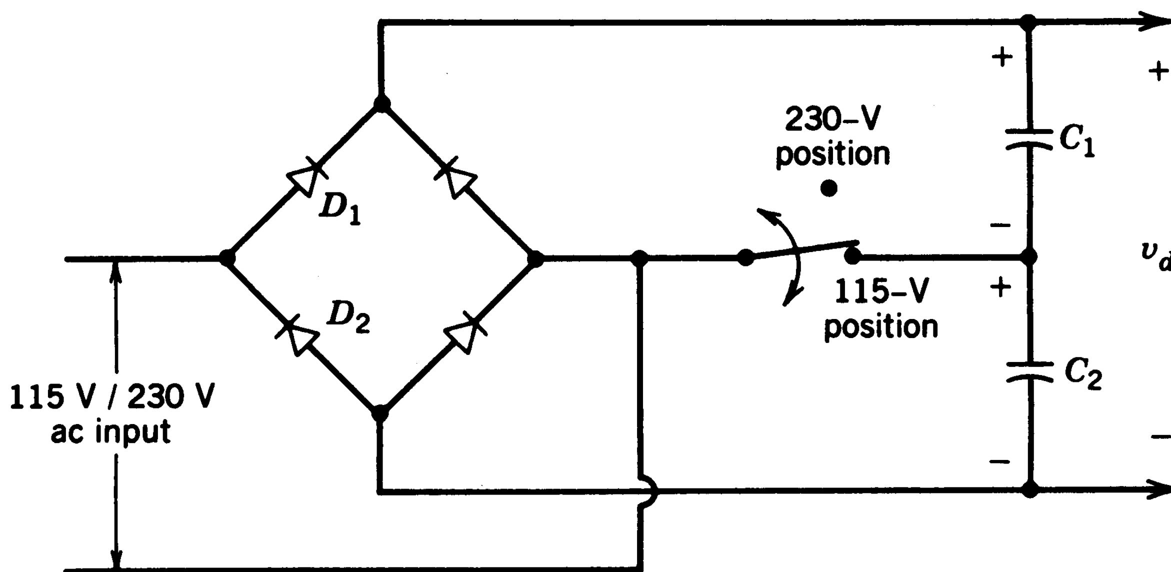

Figure 5-27 Voltage-doubler rectifier.

- In 115-V position, one capacitor at-a-time is charged from the input.

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A Three-Phase, Four-Wire System

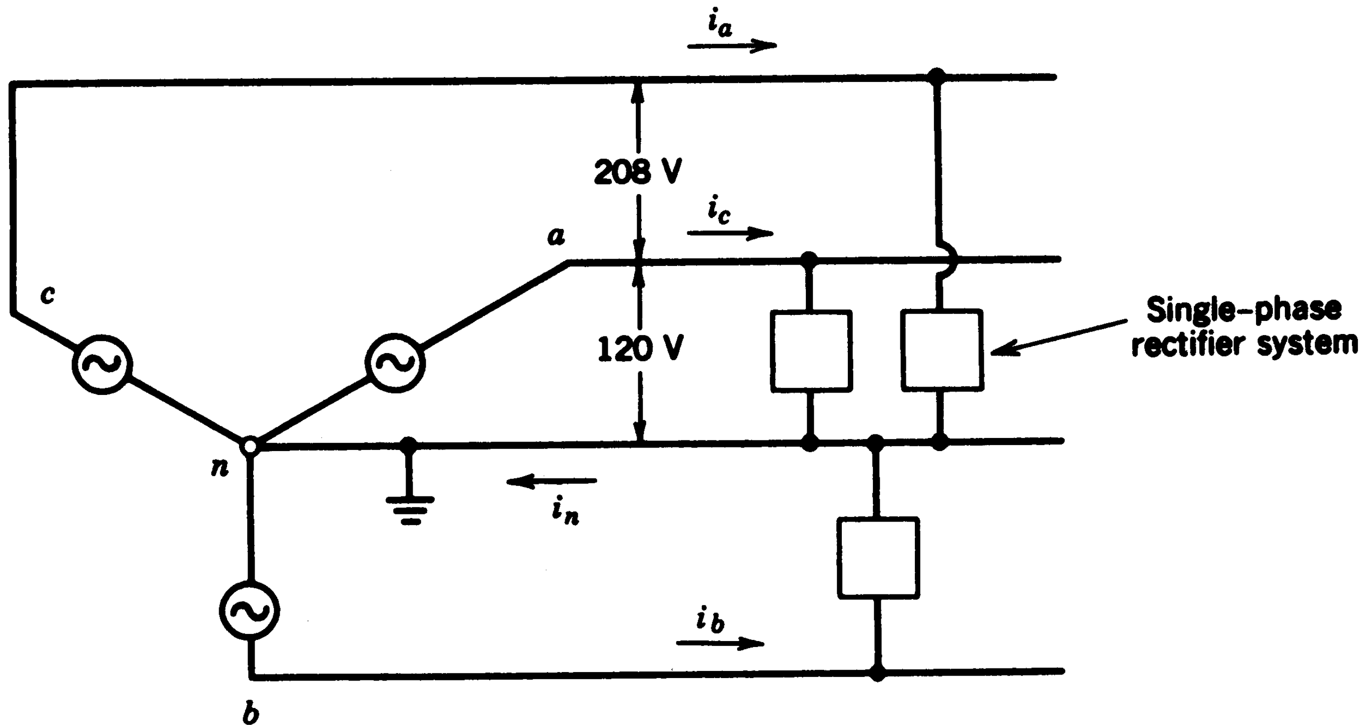

Figure 5-28 Three-phase, four-wire system.

- A common neutral wire is assumed

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Current in A Three-Phase, Four-Wire System

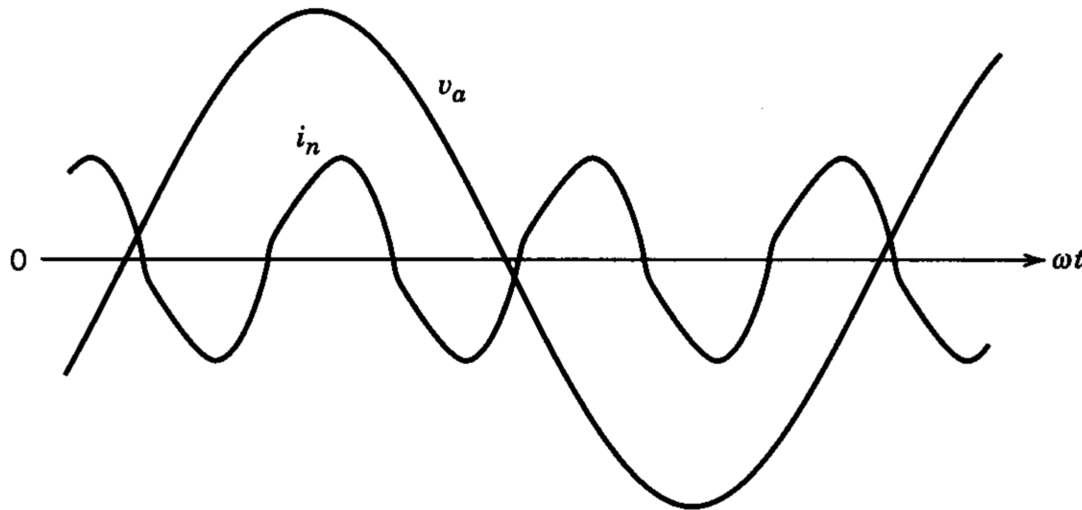

Figure 5-29 Neutral-wire current i_n.

- The current in the neutral wire can be very high

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Three-Phase, Full-Bridge Rectifier

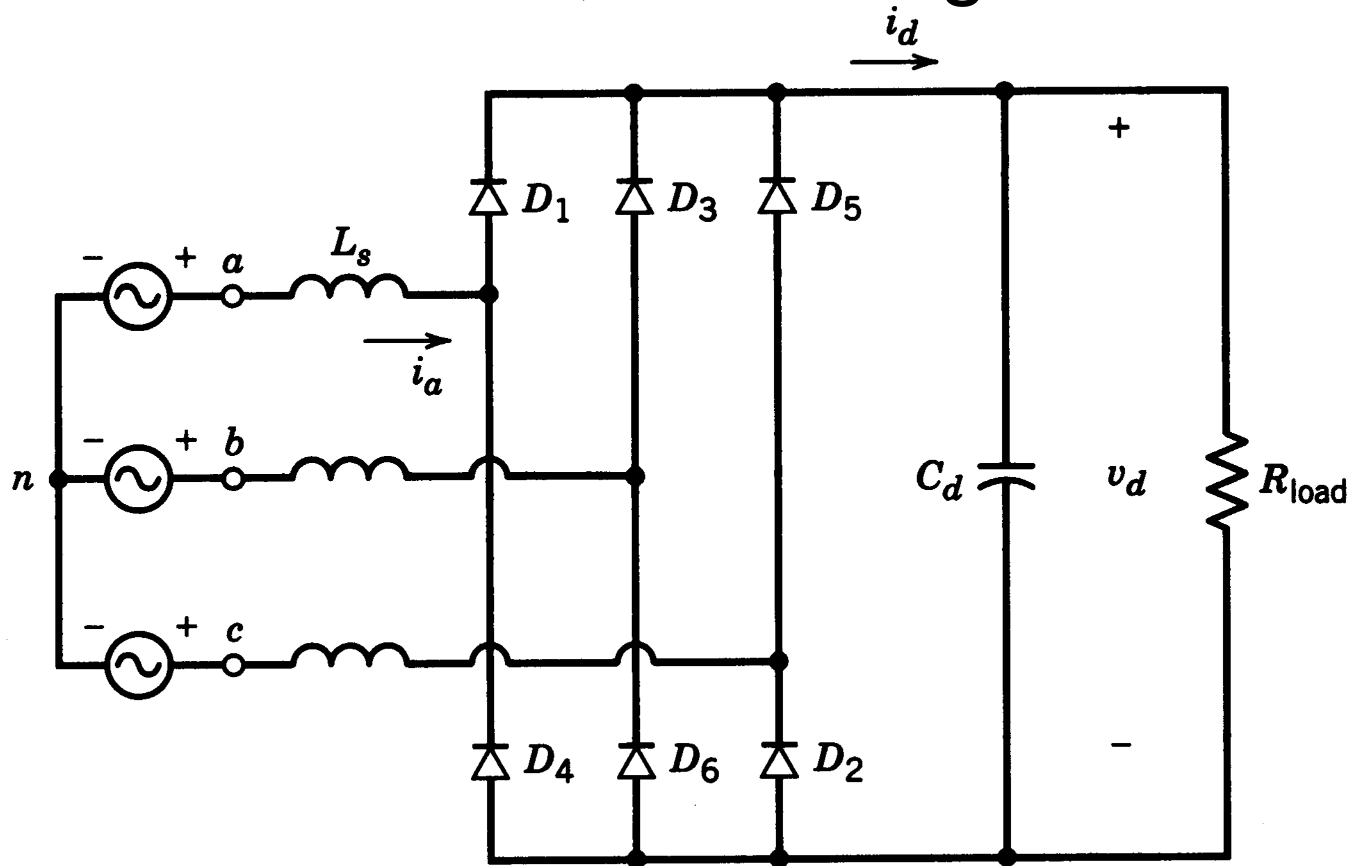

Figure 5-30 Three-phase, full-bridge rectifier.

- Commonly used

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Three-Phase, Full-Bridge Rectifier: Redrawn

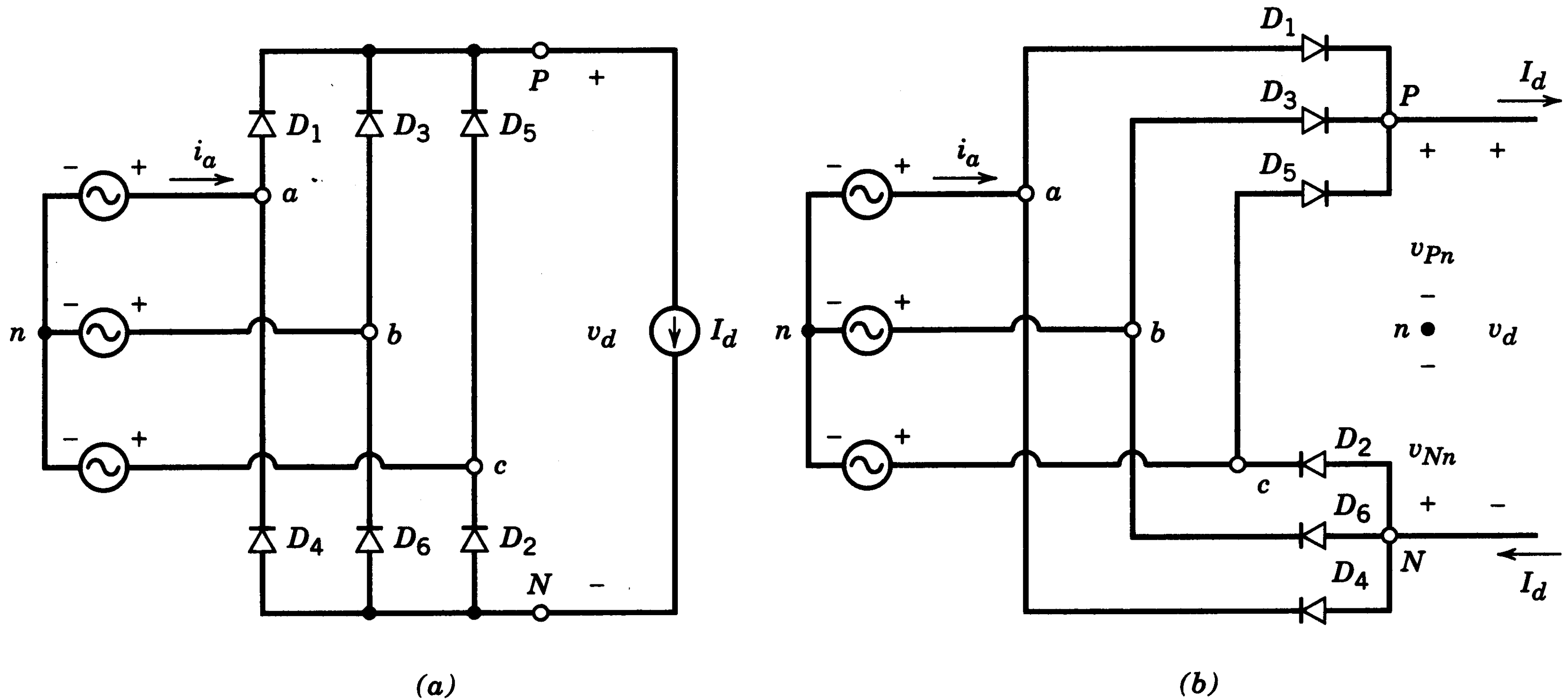

Figure 5-31 Three-phase rectifier with a constant dc current.

- Two groups with three diodes each

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Three-Phase, Full-Bridge Rectifier Waveforms

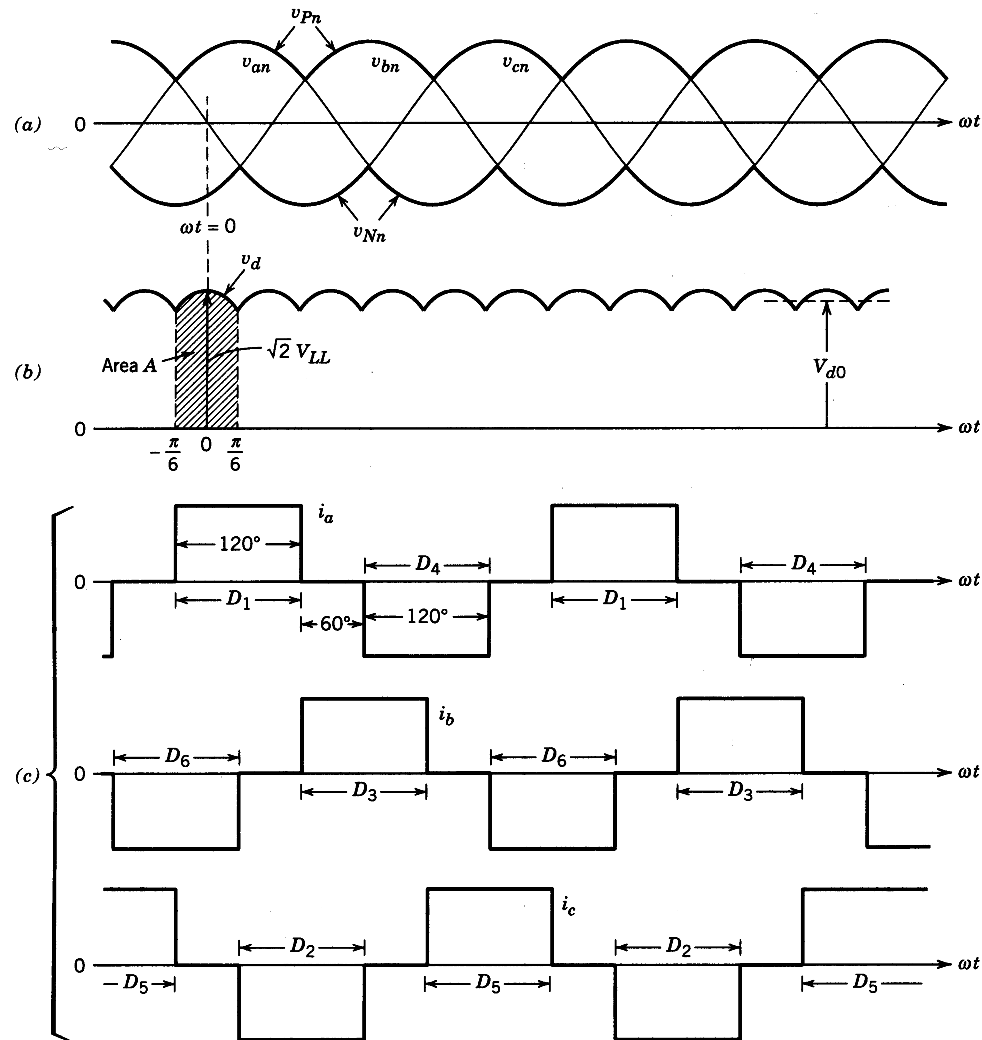

Figure 5-32 Waveforms in the circuit of Fig. 5-31.

- Output current is assumed to be dc

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Three-Phase, Full-Bridge Rectifier: Input Line-Current

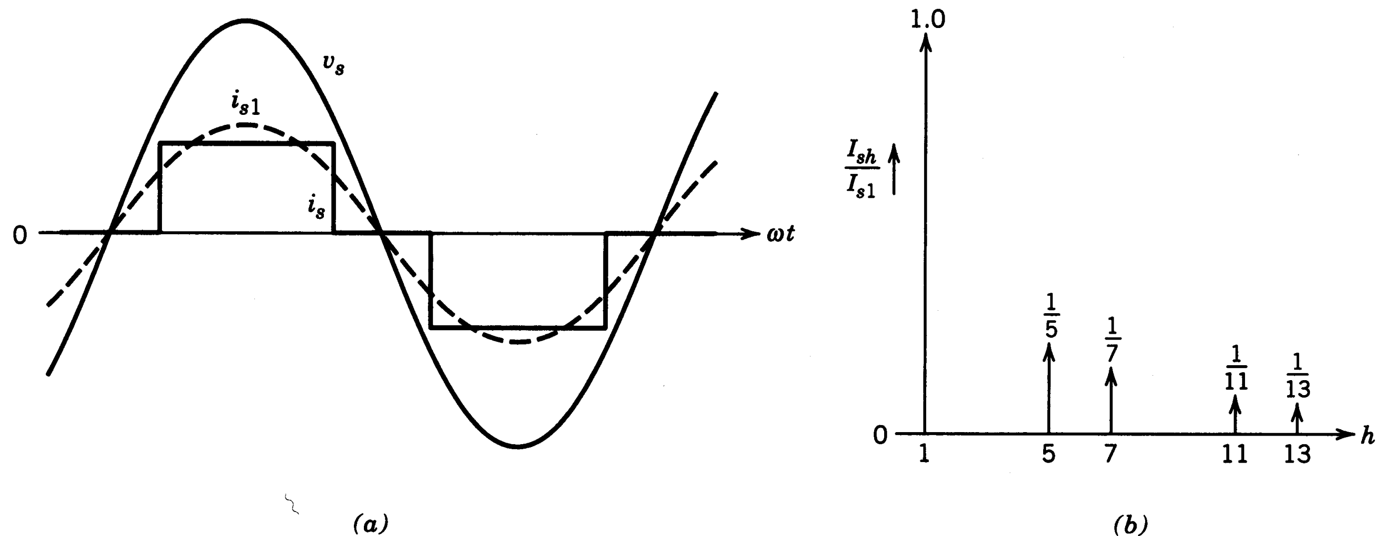

Figure 5-33 Line current in a three-phase rectifier in the idealized case with $L_s = 0$ and a constant dc current.

- Assuming output current to be purely dc and zero ac-side inductance

Three-Phase, Full-Bridge Rectifier

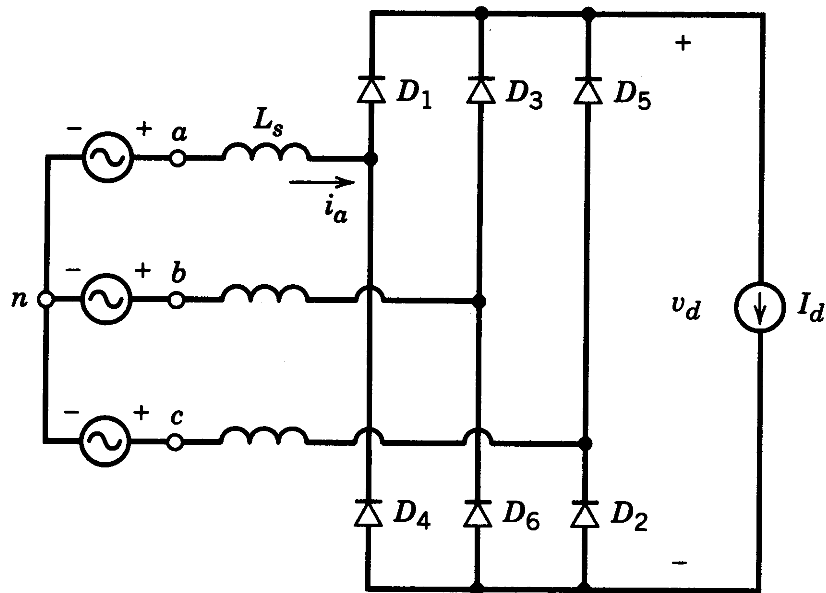

Figure 5-34 Three-phase rectifier with a finite L_s and a constant dc current.

- Including the ac-side inductance

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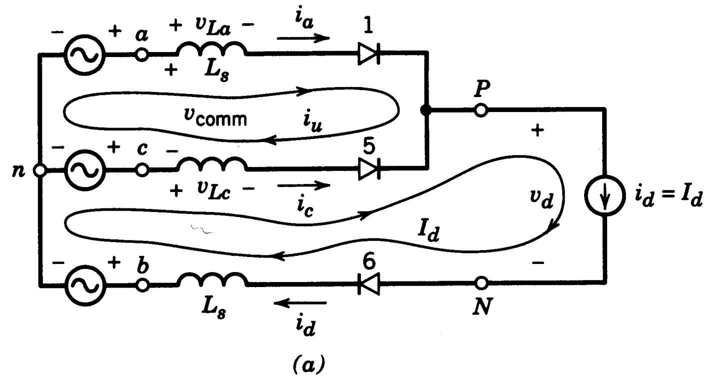
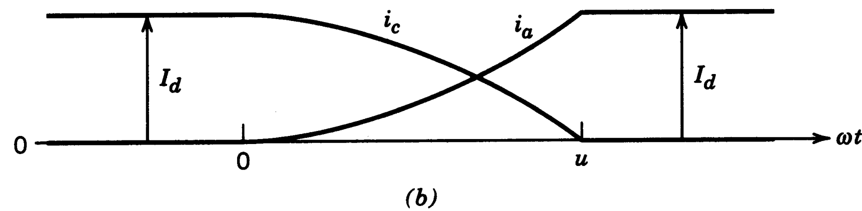
3-Phase Rectifier: Current Commutation

- output current is assumed to be purely dc





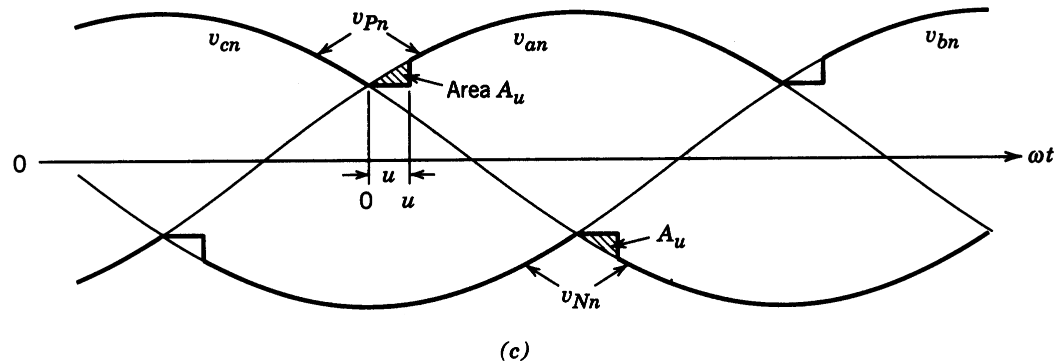


Figure 5-35 Current commutation process.

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Rectifier with a Large Filter Capacitor

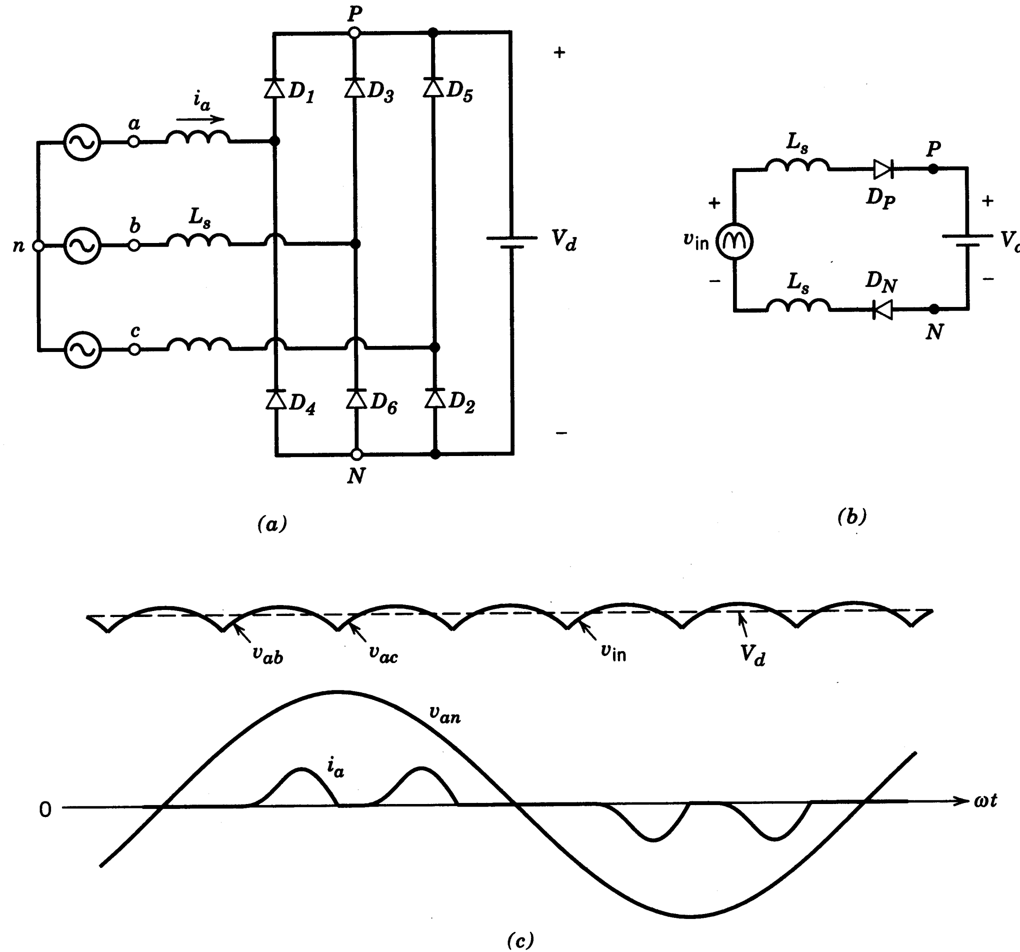

Figure 5-36 (a) Three-phase rectifier with a finite L_s and a constant dc voltage. (b) Equivalent circuit. (c) Waveforms.

- Output voltage is assumed to be purely dc

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Three-Phase, Full-Bridge Rectifier

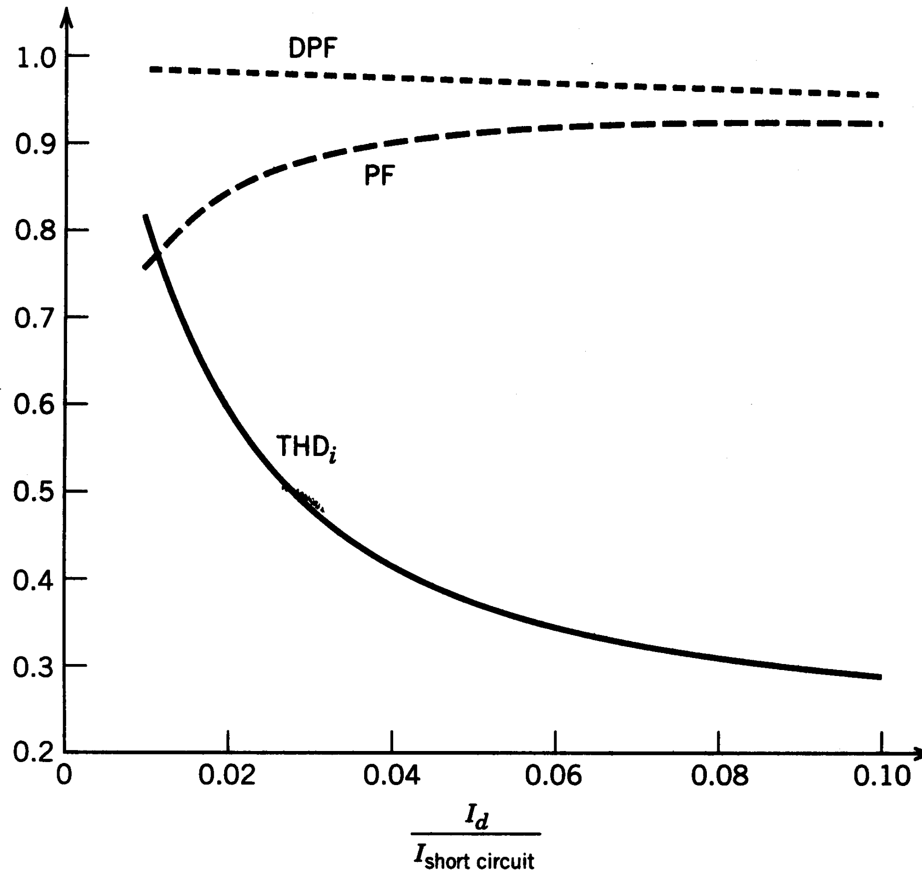

Figure 5-37 Total harmonic distortion, DPF, and PF in the rectifier of Fig. 5-36 with a constant dc voltage.

- THD, PF and DPF as functions of load current

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Crest Factor versus the Current Loading

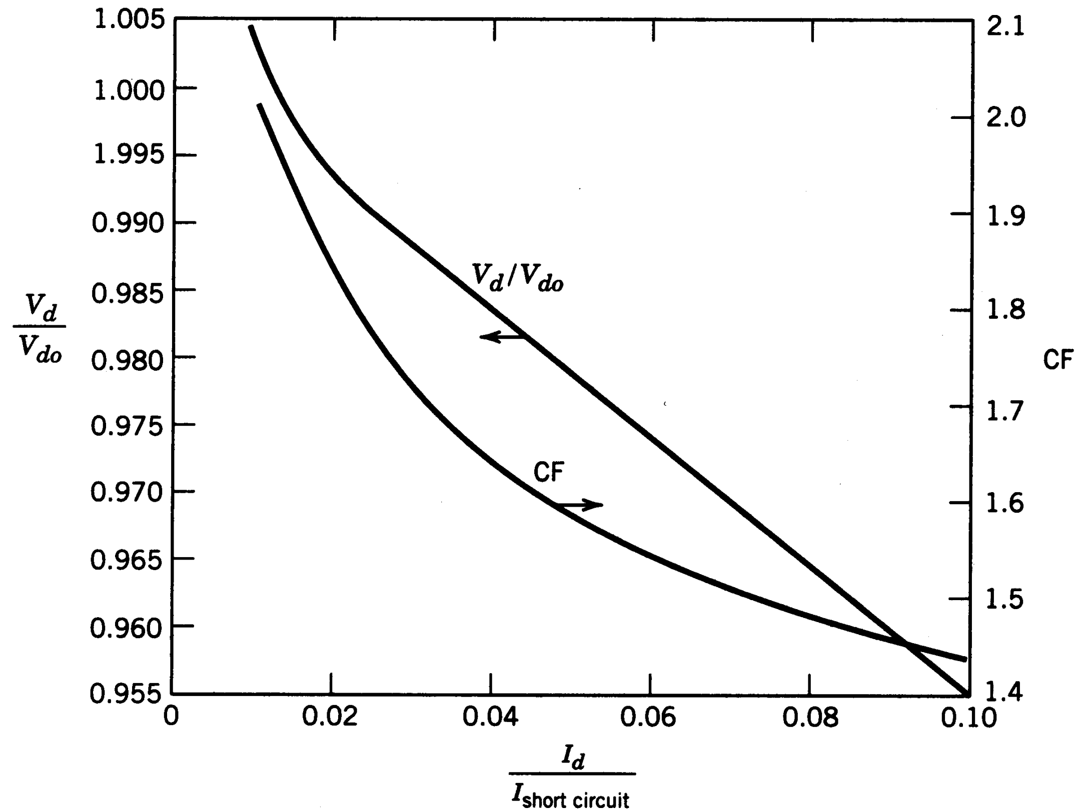

Figure 5-38 Normalized V_d and crest factor in the rectifier of Fig. 5-36 with a constant dc voltage.

- The Crest Factor is very high at low values of current

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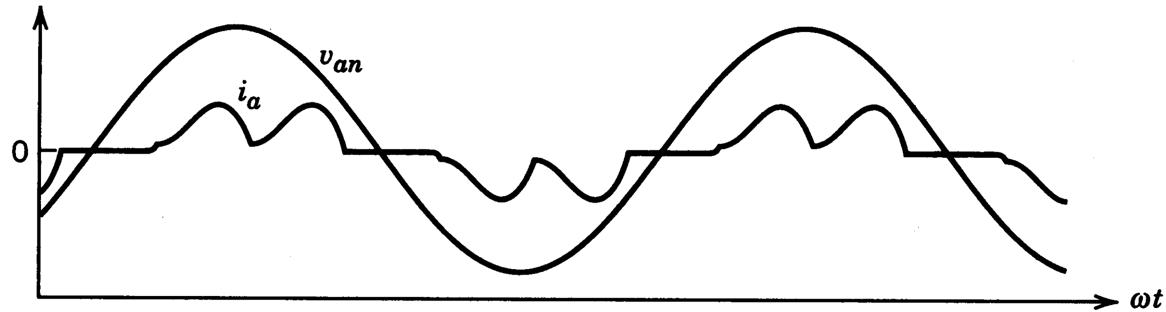
Three-Phase Rectifier Waveforms



(a)

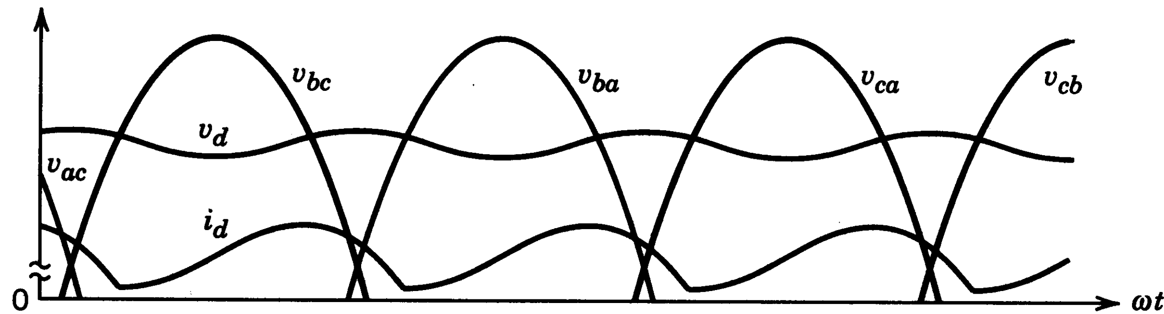


Figure 5-39 Waveforms in the rectifier of Fig. 5-30, obtained in Example 5-7.

- PSpice-based analysis

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Chapter 6

Thyristor Converters

Chapter 6 Line-Frequency Phase-Controlled Rectifiers and Inverters: Line-Frequency ac ↔ Controlled dc **121**

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6-2 Thyristor Circuits and Their Control 122
6-3 Single-Phase Converters 126
6-4 Three-Phase Converters 138
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Summary *153*
Problems *154*
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- Controlled conversion of ac into dc

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Thyristor Converters

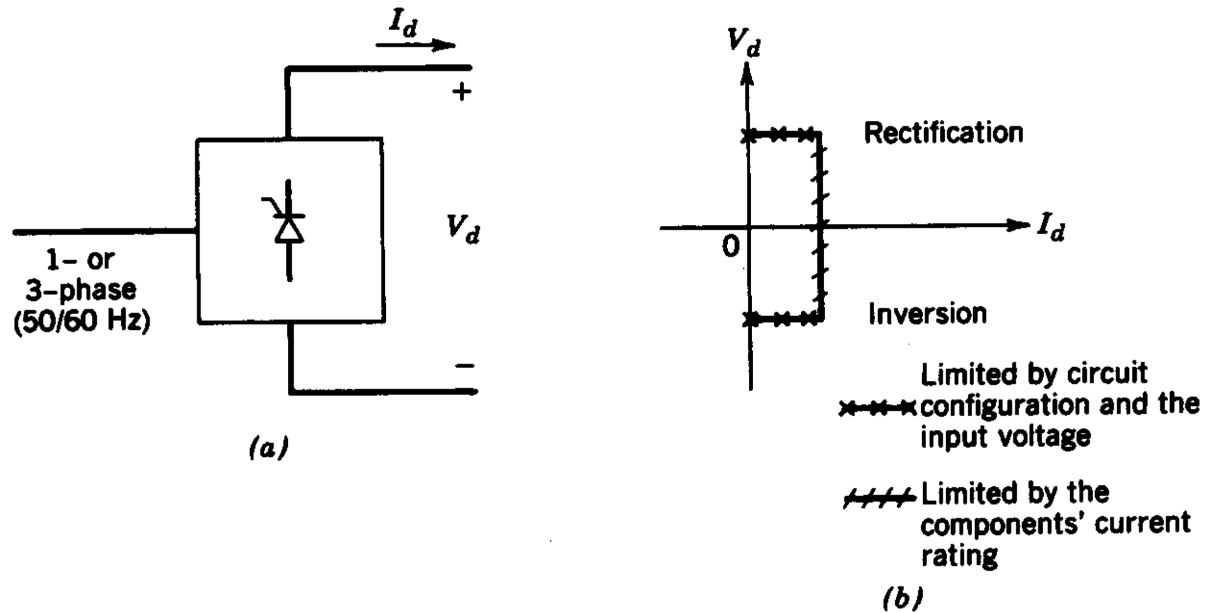

Figure 6-1 Line-frequency controlled converter.

- Two-quadrant conversion

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Primitive circuits with thyristors

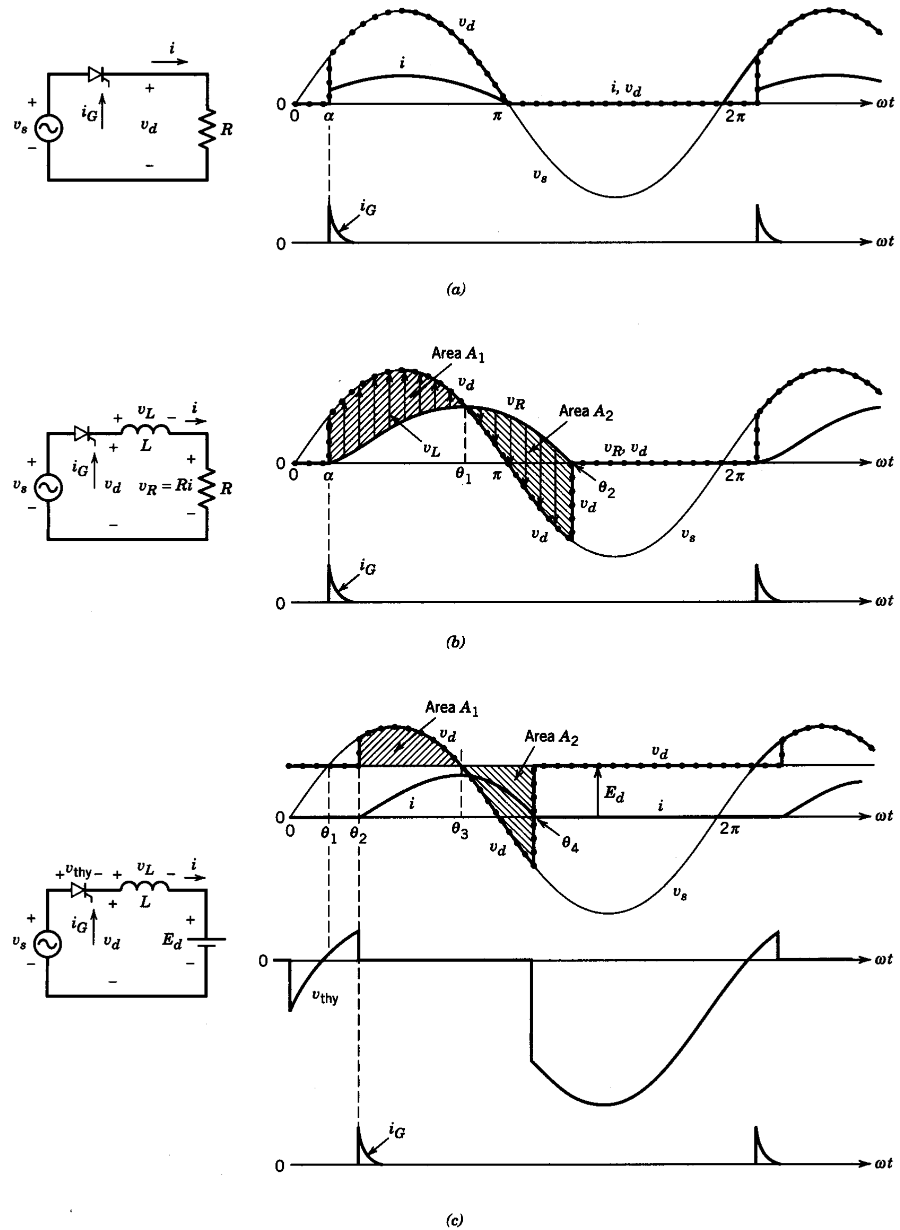

Figure 6-2 Basic thyristor converters.

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Thyristor Triggering

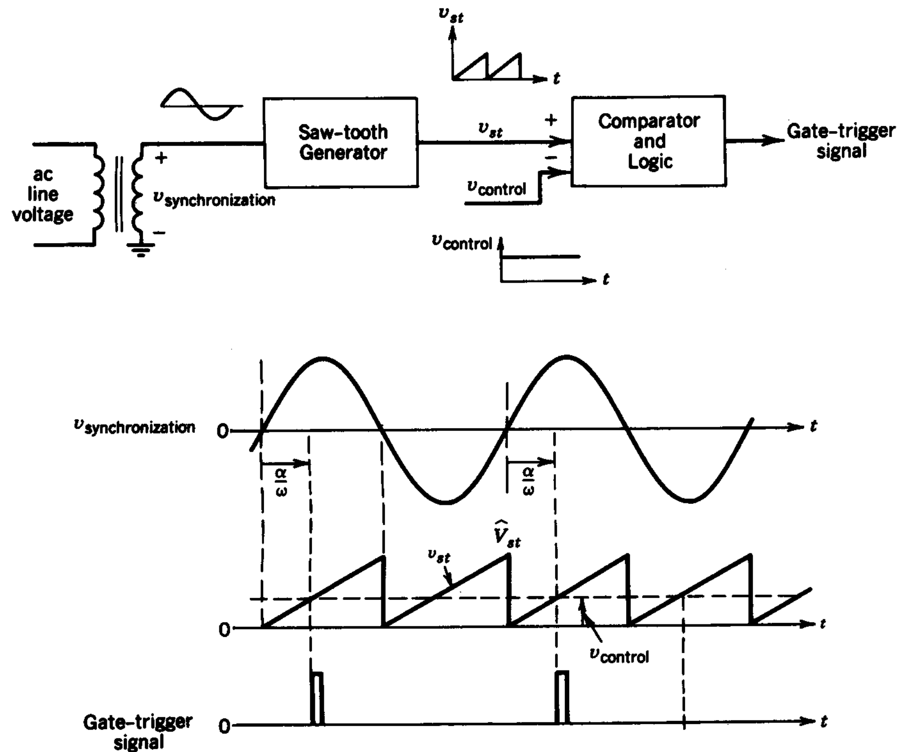

Figure 6-3 Gate trigger control circuit.

- ICs available

Full-Bridge Thyristor Converters

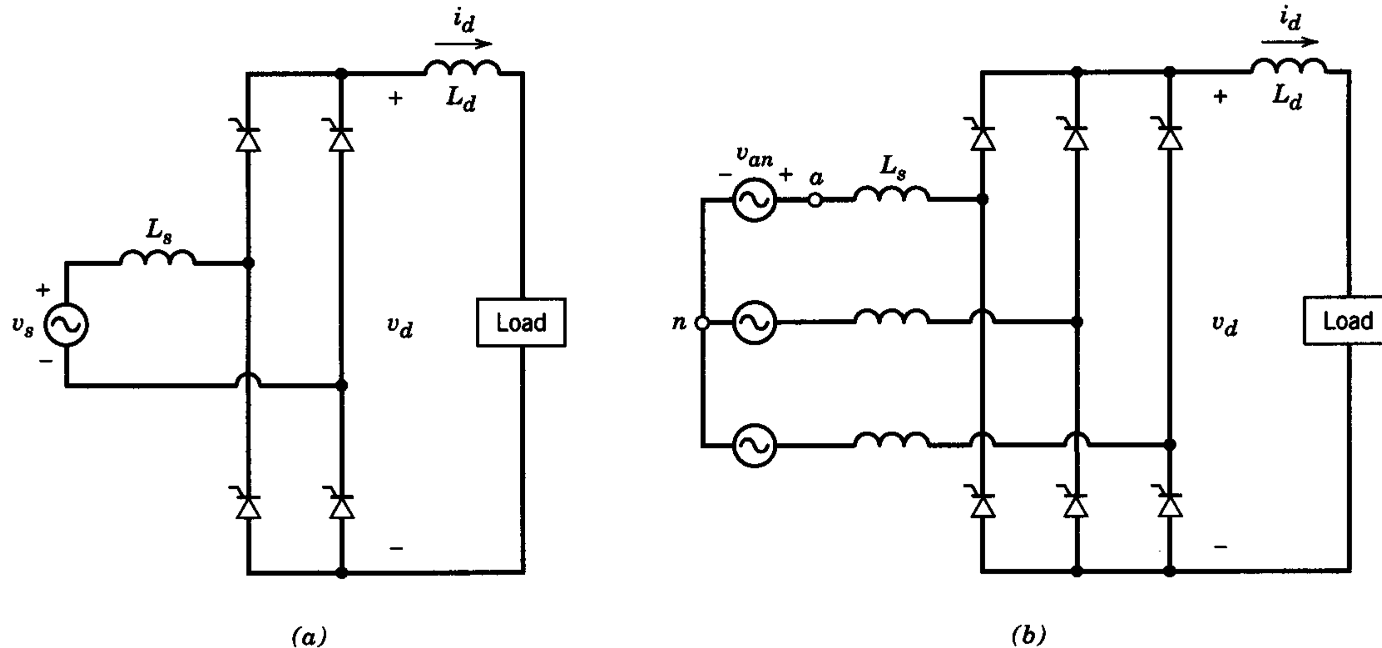

Figure 6-4 Practical thyristor converters.

- Single-phase and three-phase

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Single-Phase Thyristor Converters

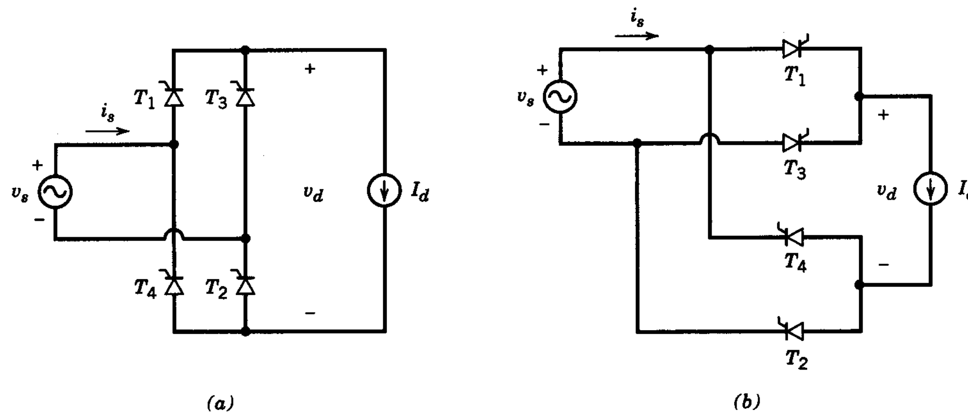

Figure 6-5 Single-phase thyristor converter with $L_s = 0$ and a constant dc current.

- Two groups with two thyristor each

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1-Phase Thyristor Converter Waveforms

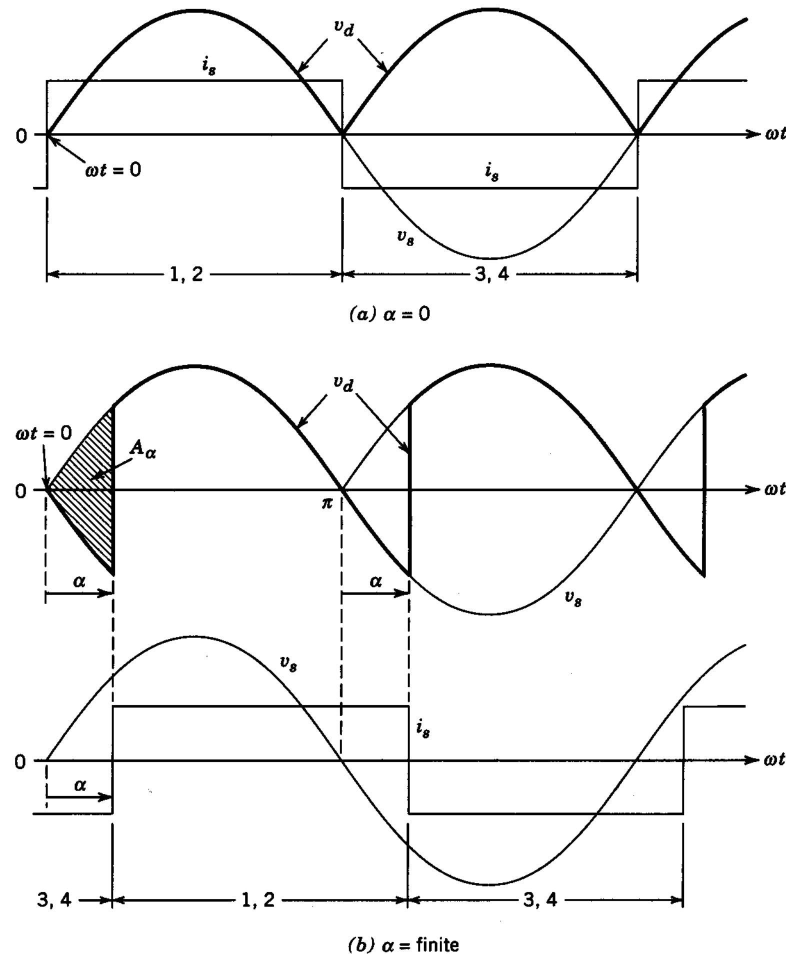

Figure 6-6 Waveforms in the converter of Fig. 6-5.

- Assuming zero ac-side inductance

Average DC Output Voltage

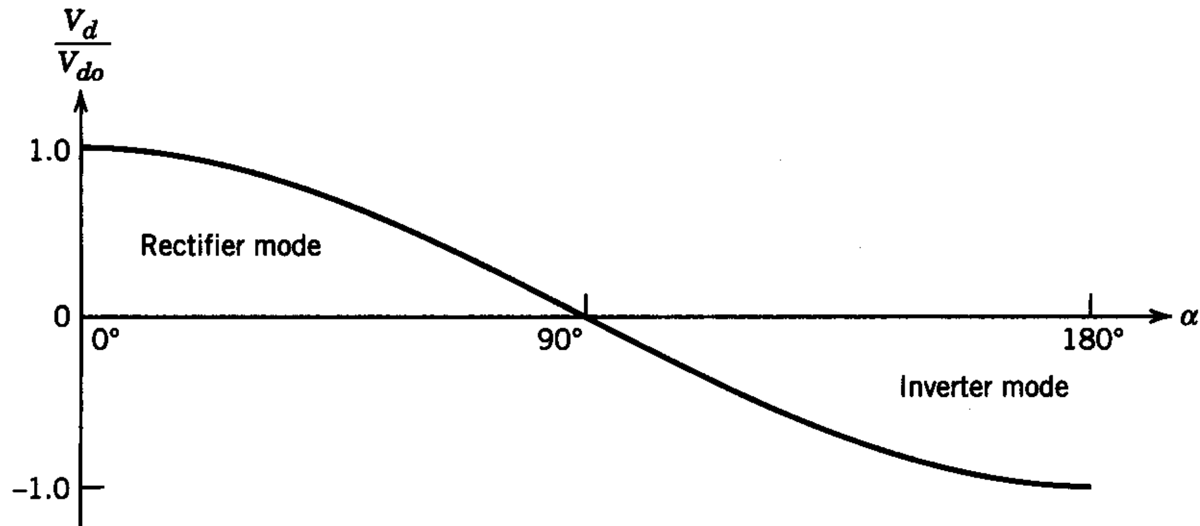

Figure 6-7 Normalized V_d as a function of α.

- Assuming zero ac-side inductance

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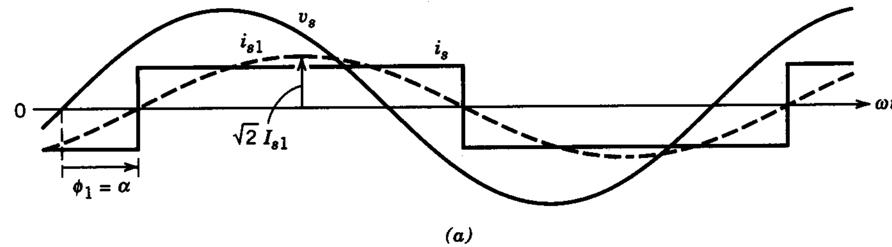
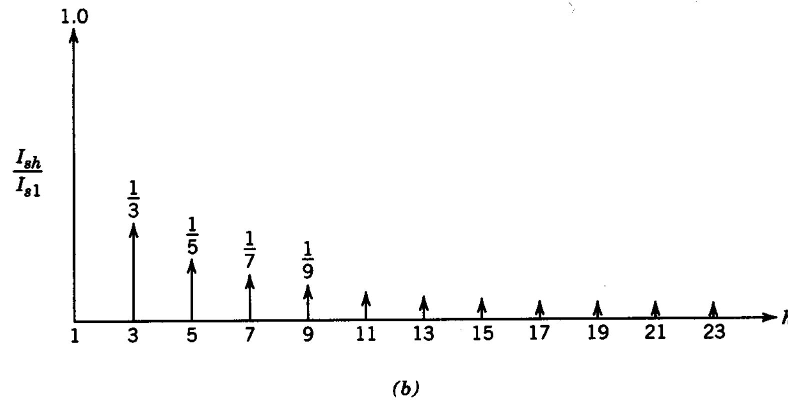
Input Line-Current Waveforms





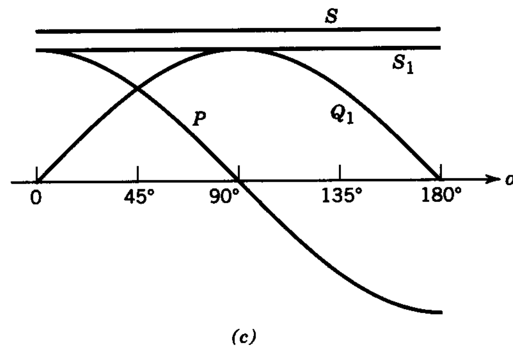


Figure 6-8 The ac-side quantities in the converter of Fig. 6-5.

- Harmonics, power and reactive power

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1-Phase Thyristor Converter

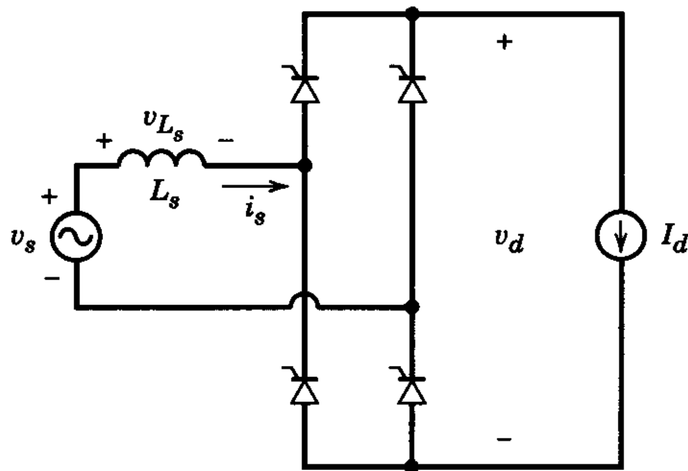

Figure 6-9 Single-phase thyristor converter with a finite L_s and a constant dc current.

- Finite ac-side inductance; constant dc output current

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Thyristor Converter Waveforms

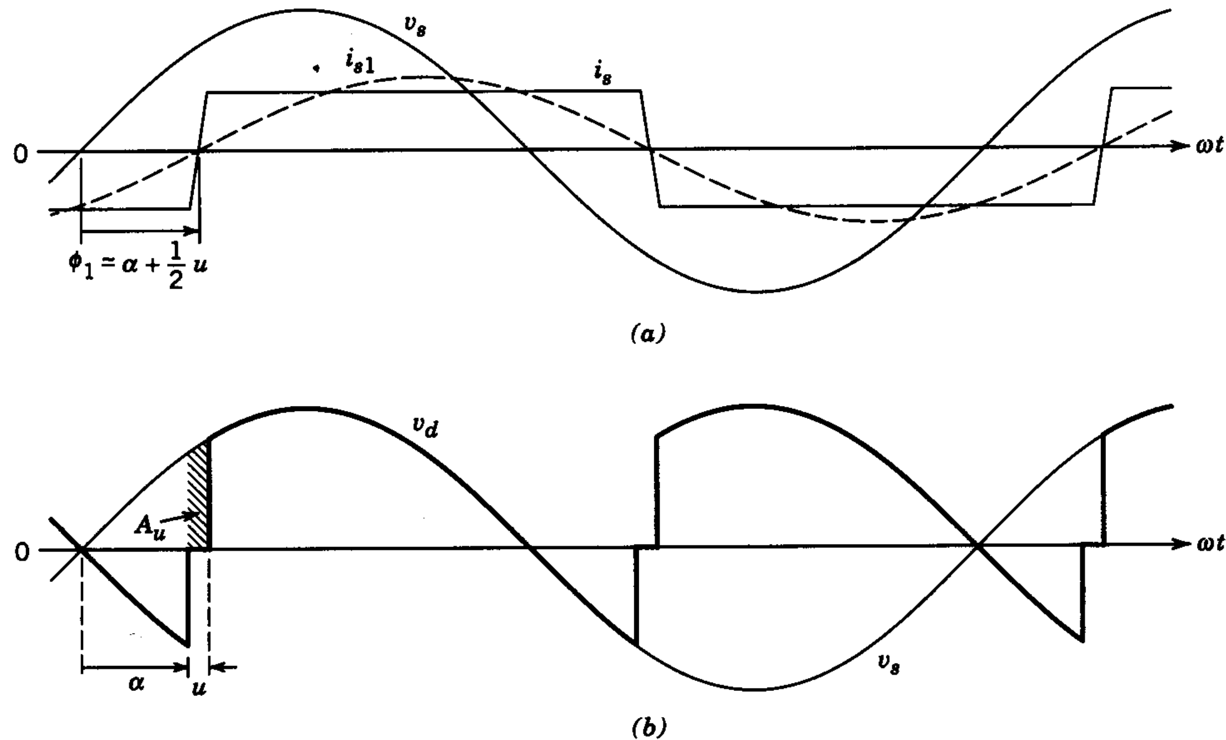

Figure 6-10 Waveforms in the converter of Fig. 6-9.

- Finite ac-side inductance

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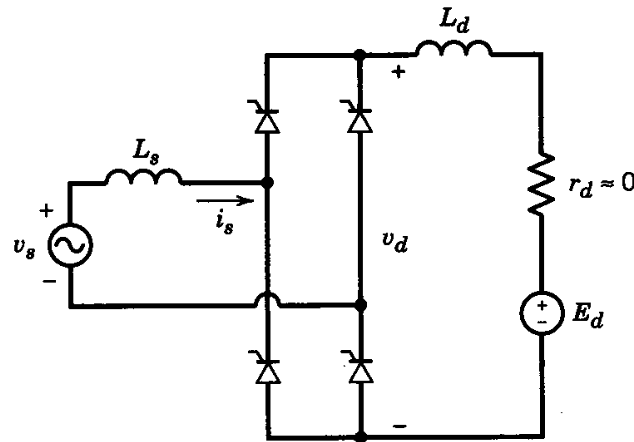
Thyristor Converter: Discontinuous Mode



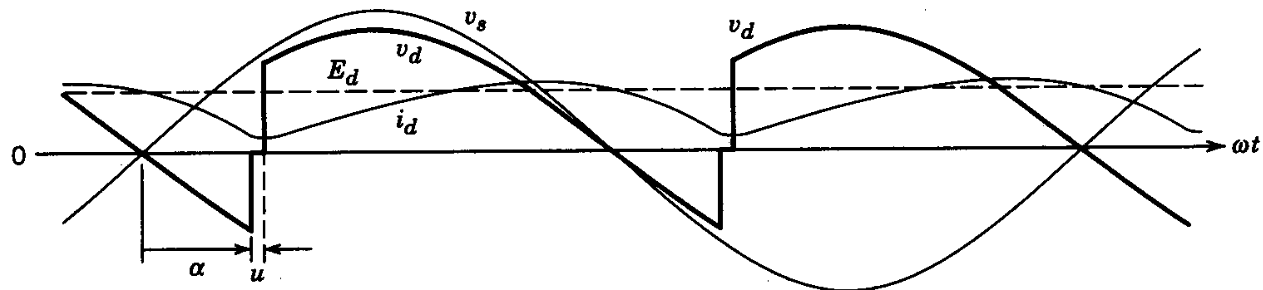


Figure 6-11 (*a*) A practical thyristor converter. (*b*) Waveforms.

- This mode can occur in a dc-drive at light loads

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Thyristor Converter Waveforms

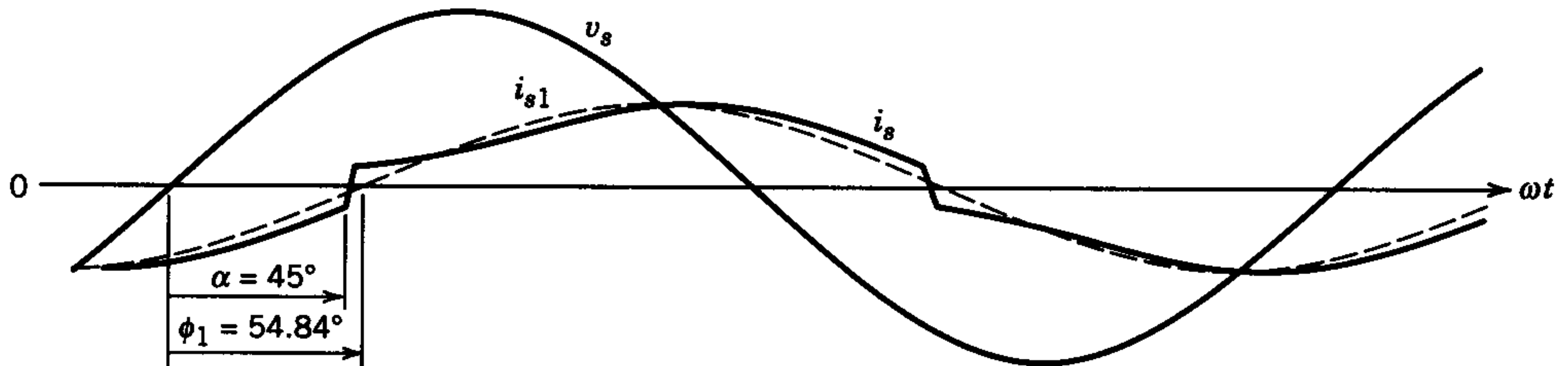

Figure 6-12 Waveforms in Example 6-2 for the circuit of Fig. 6-11*a*.

- PSpice-based simulation

Thyristor Converter Waveforms: Discontinuous Conduction Mode

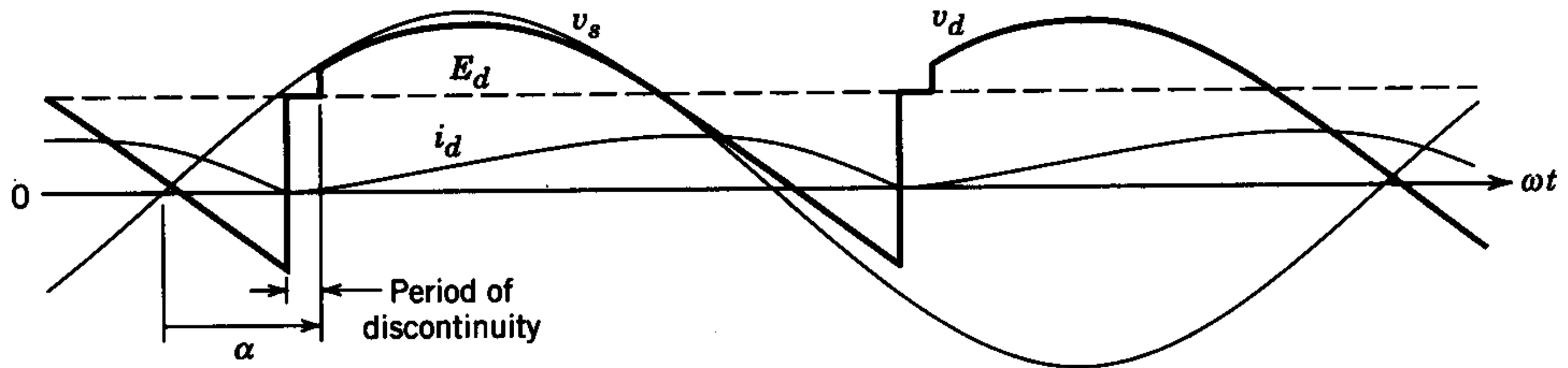

Figure 6-13 Waveforms in a discontinuous-current-conduction mode.

- PSpice-based simulation

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DC Voltage versus Load Current

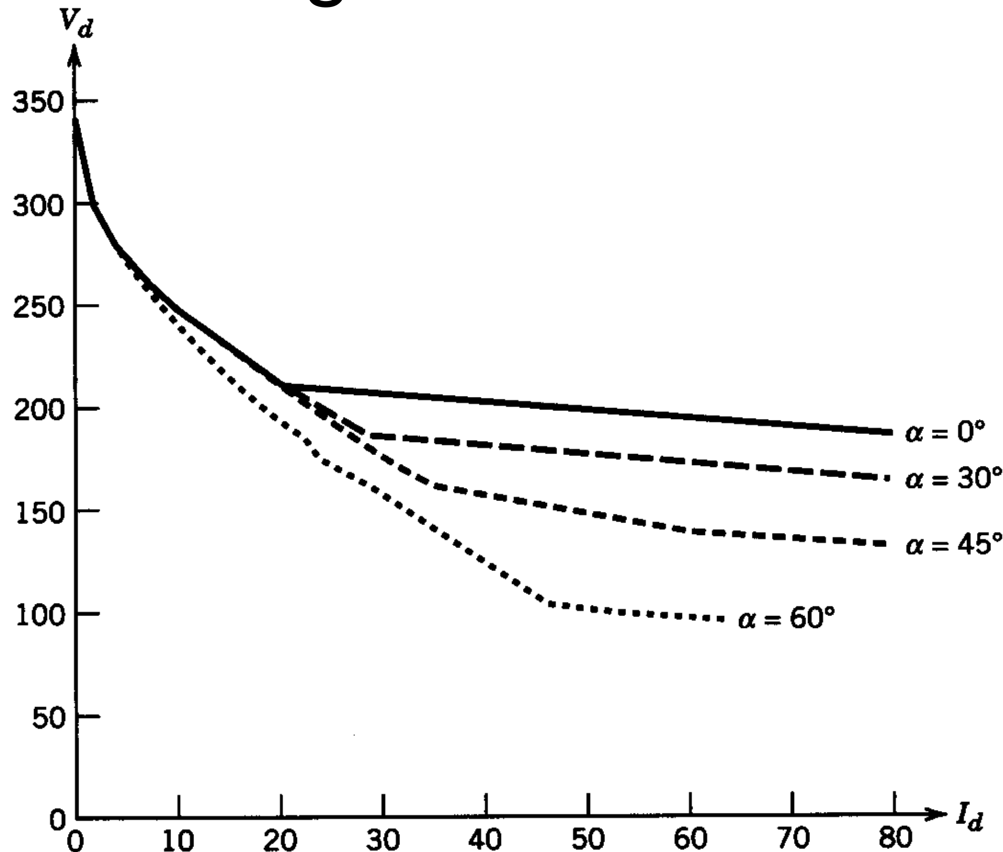

Figure 6-14 V_d versus I_d in the single-phase thyristor converter of Fig. 6-11*a*.

- Various values of delay angle

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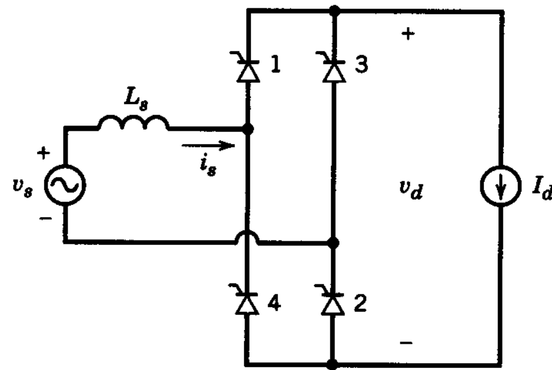
Thyristor Converters: Inverter Mode



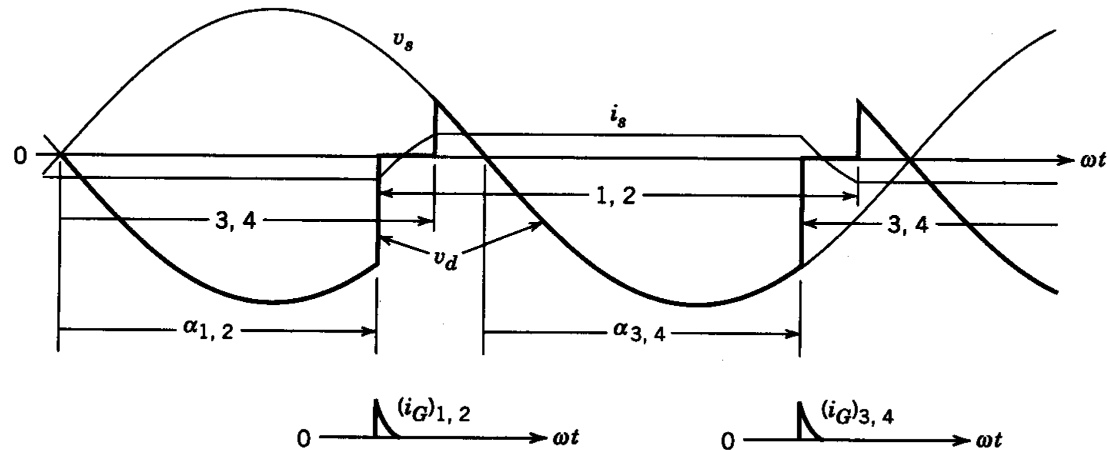


Figure 6-15 (*a*) Inverter, assuming a constant dc current. (*b*) Waveforms.

- Assuming the ac-side inductance to be zero

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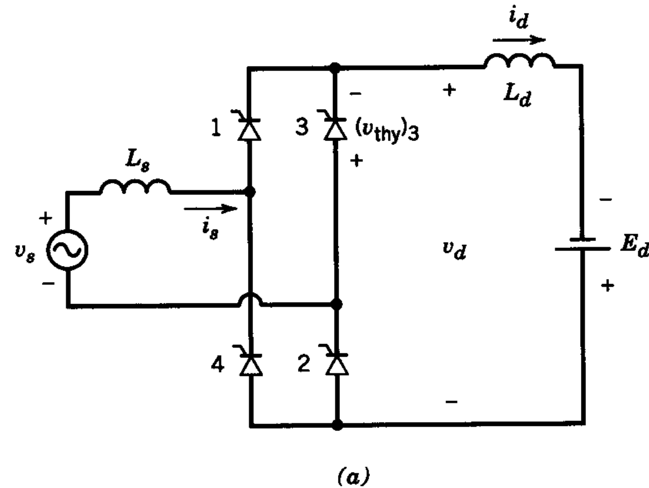
Thyristor Converters: Inverter Mode



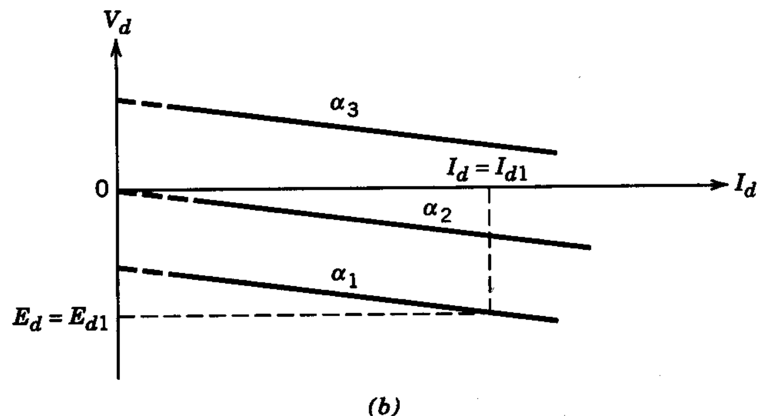


Figure 6-16 (*a*) Thyristor inverter with a dc voltage source. (*b*) $\mathbf{V_d}$ versus I_d.

- Family of curves at various values of delay angle

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Thyristor Converters: Inverter Mode

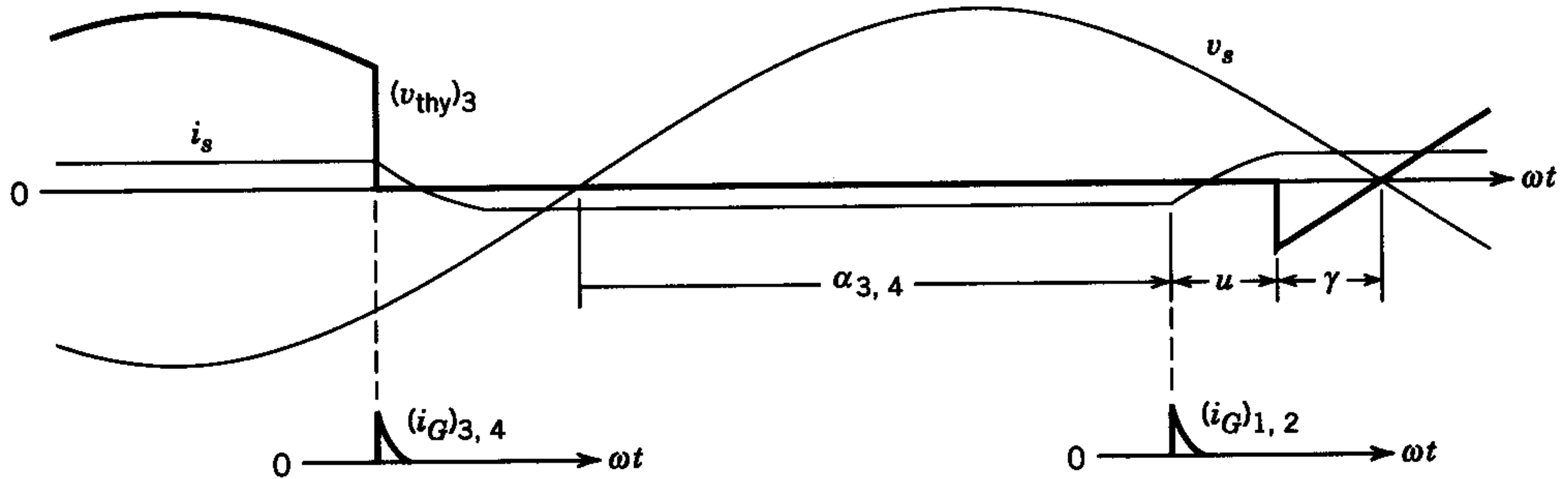

Figure 6-17 Voltage across a thyristor in the inverter mode.

- Importance of extinction angle in inverter mode

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Thyristor Converters: Inverter Mode

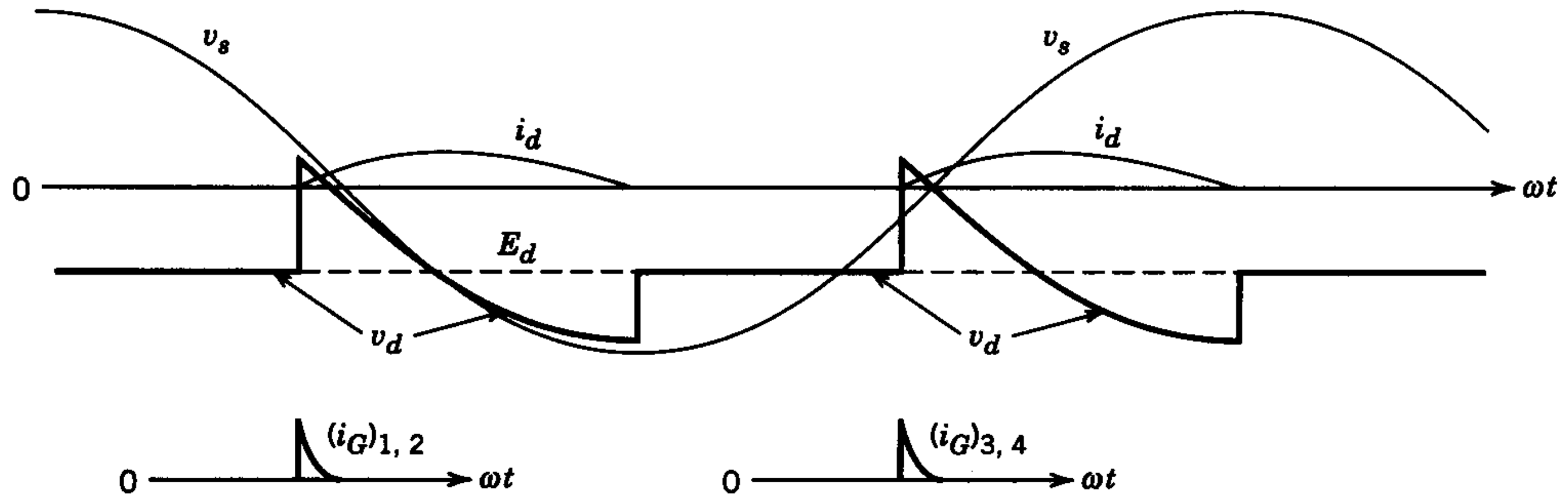

Figure 6-18 Waveforms at inverter start-up.

- Waveforms at start-up

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3-Phase Thyristor Converters

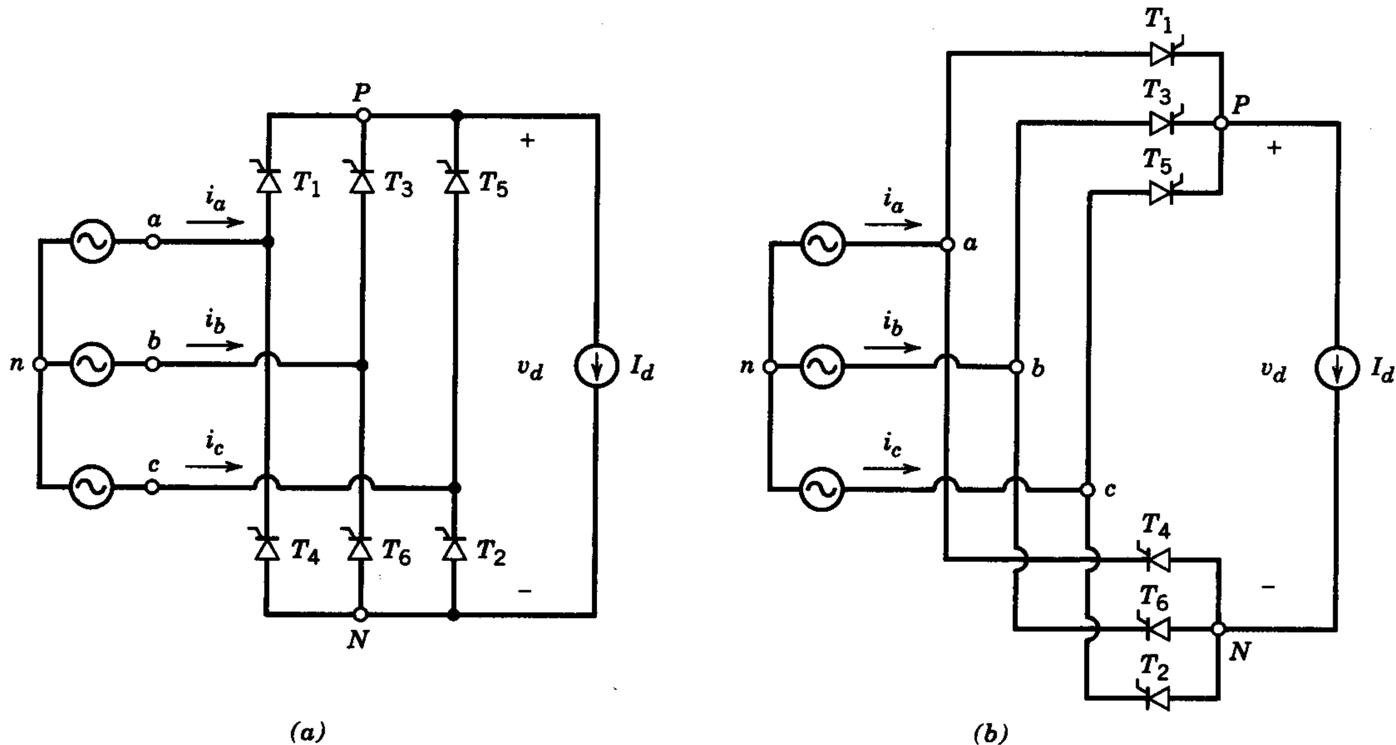

Figure 6-19 Three-phase thyristor converter with $L_s = 0$ and a constant dc current.

- Two groups of three thyristors each

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3-Phase Thyristor Converter Waveforms

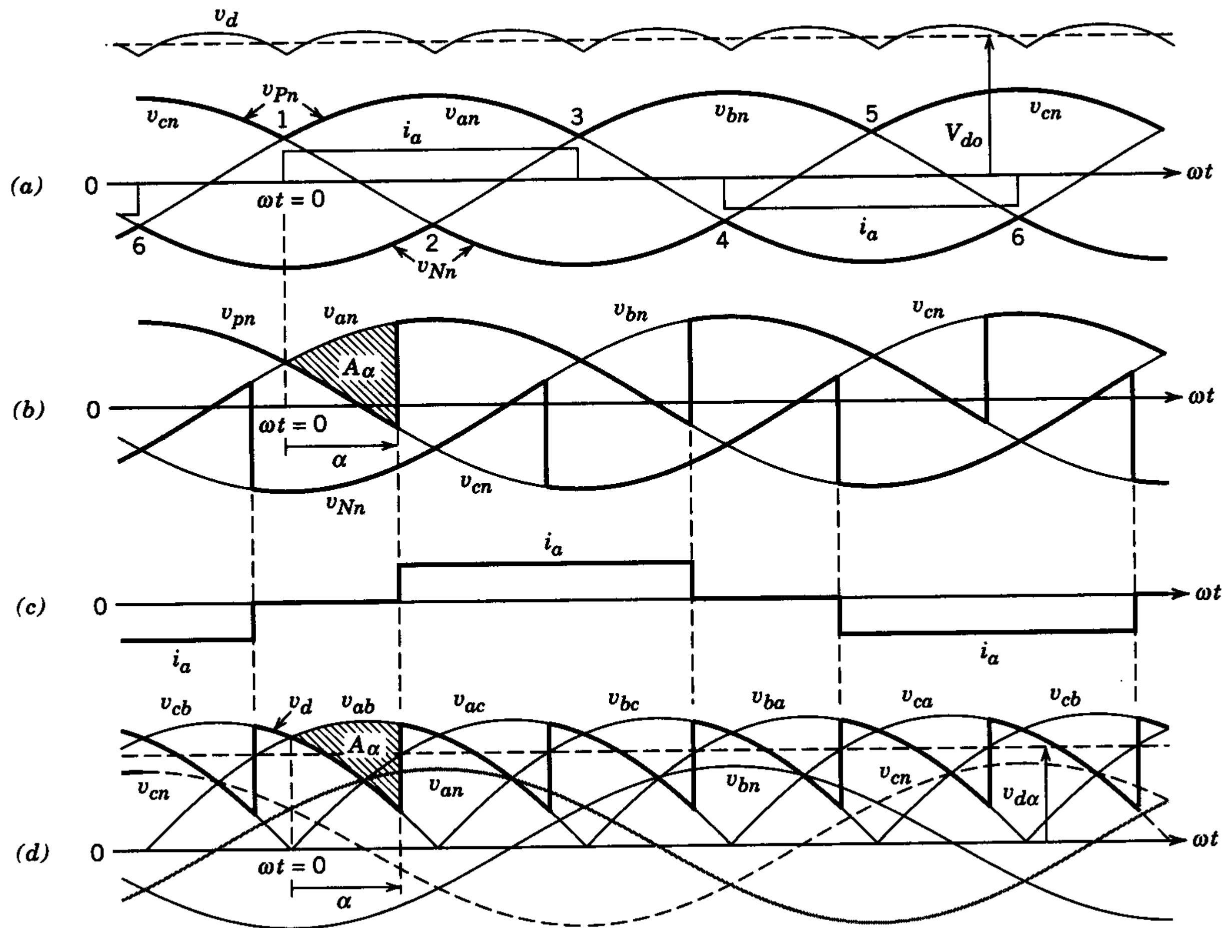

Figure 6-20 Waveforms in the converter of Fig. 6-19.

- Zero ac-side inductance; purely dc current

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DC-side voltage waveforms assuming zero ac-side inductance

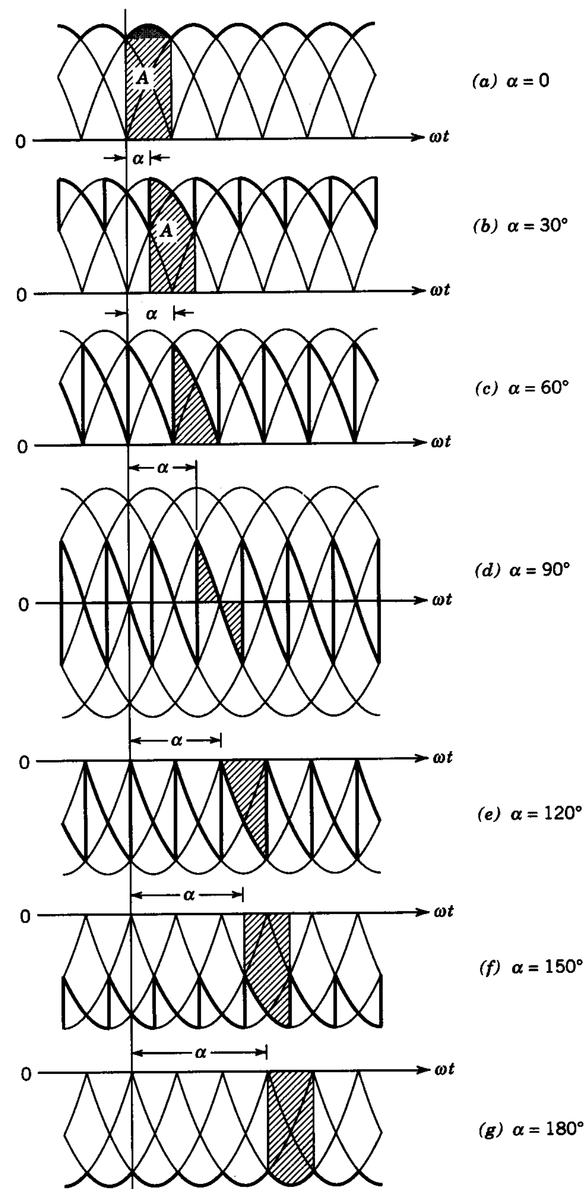

Figure 6-21 The dc-side voltage waveforms as a function of α where $V_{d\alpha} = A/(\pi/3)$. (From ref. 2 with permission.)

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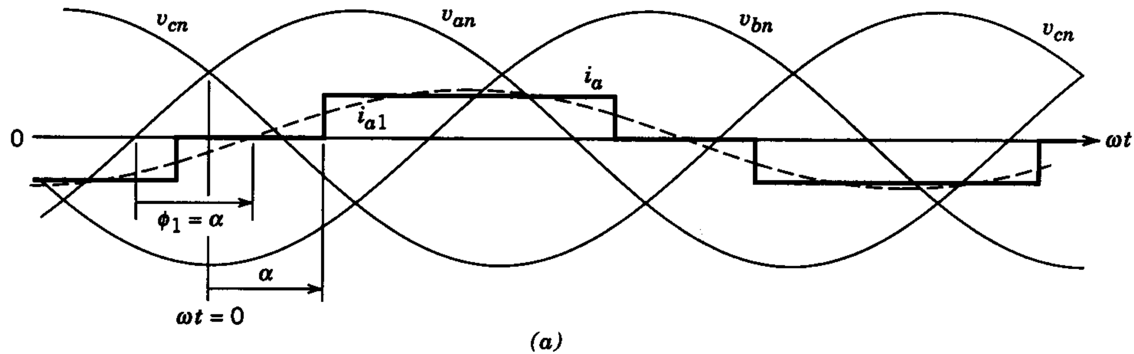
Input Line-Current Waveform



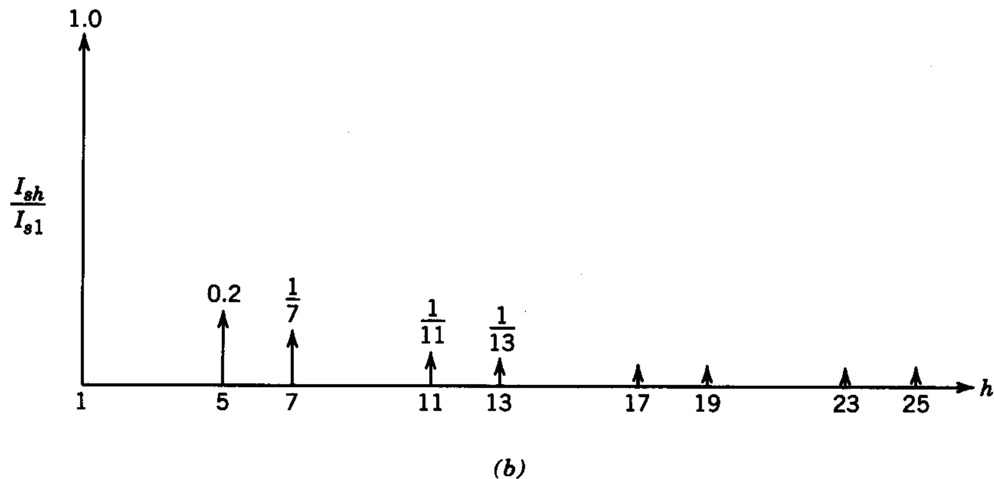


Figure 6-22 Line current in a three-phase thyristor converter of Fig. 6-19.

- Zero ac-side inductance

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Input line-current waveforms assuming zero ac-side inductance

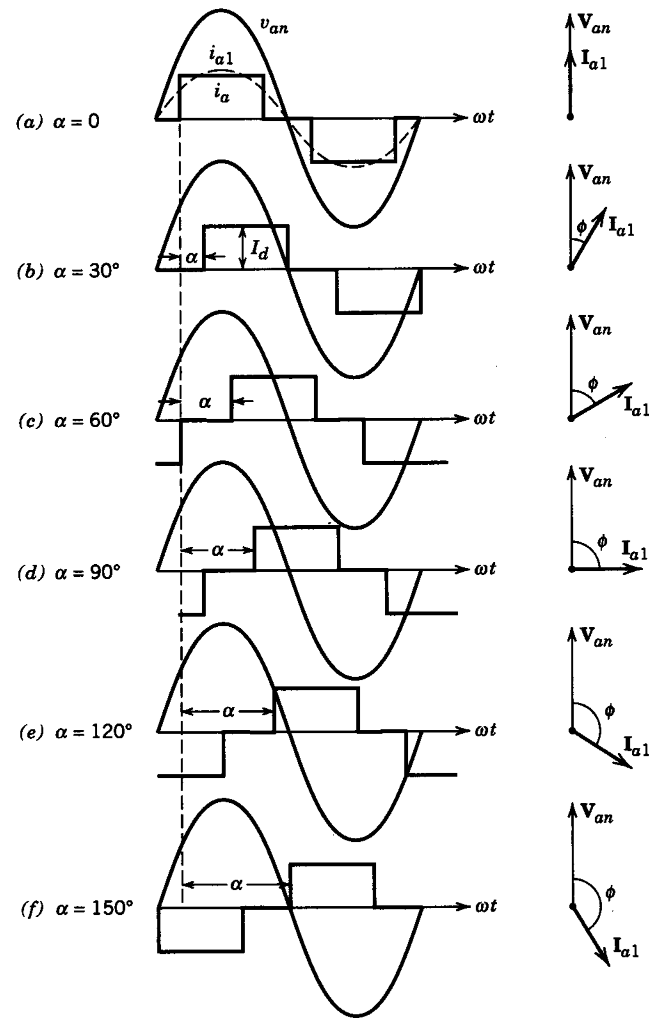

Figure 6-23 Line current as a function of α. (With permission from ref. 2.)

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Three-Phase Thyristor Converter

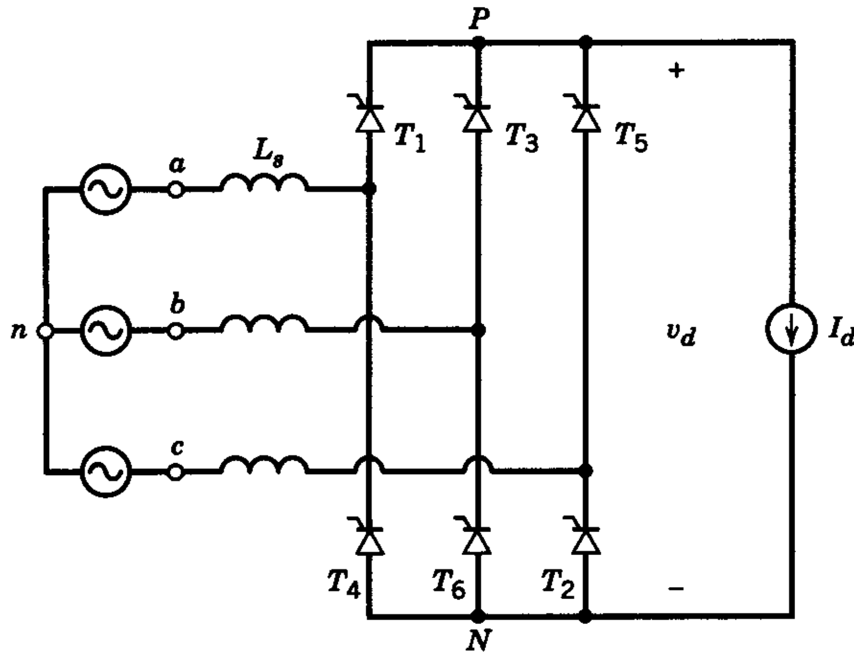

Figure 6-24 Three-phase converter with L_s and a constant dc current.

- AC-side inductance is included

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Current Commutation Waveforms

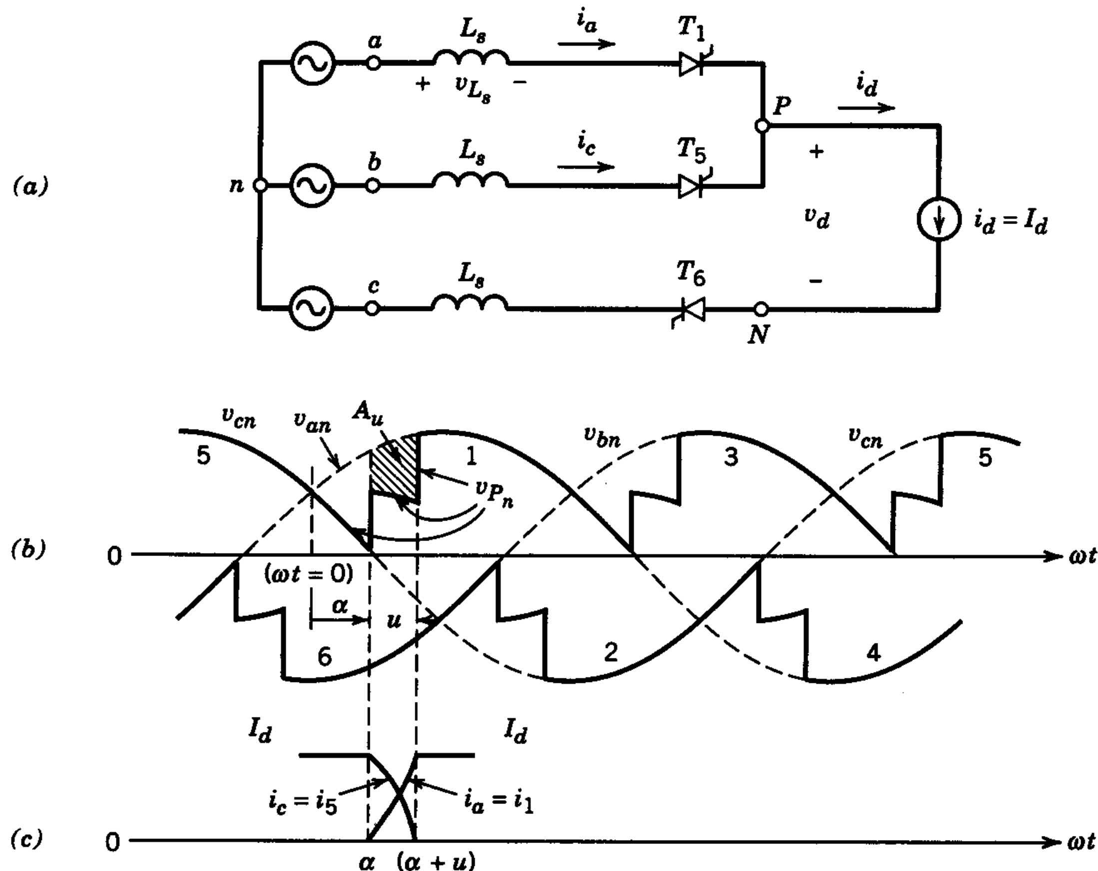

Figure 6-25 Commutation in the presence of L_s.

- Constant dc-side current

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Input Line-Current Waveform

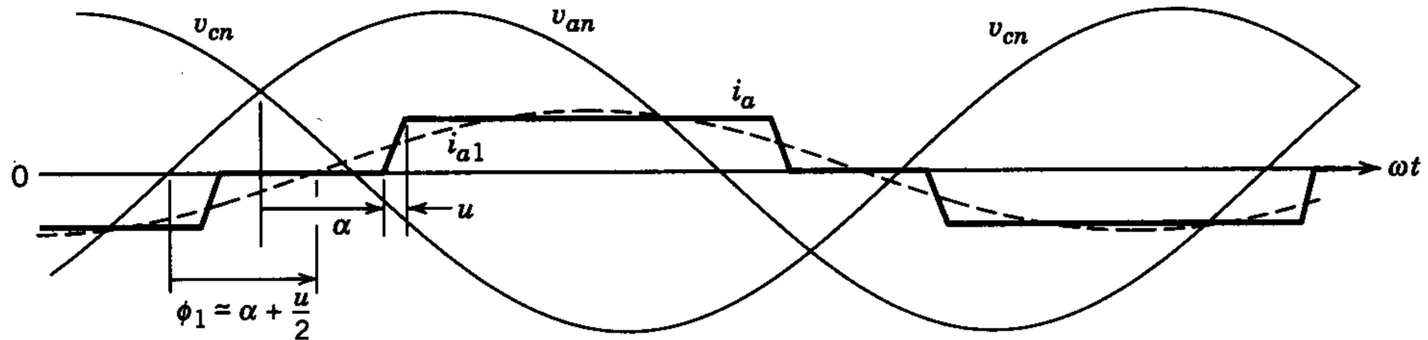

Figure 6-26 Line current in the presence of L_s.

- Finite ac-side inductance

Input Line-Current Harmonics

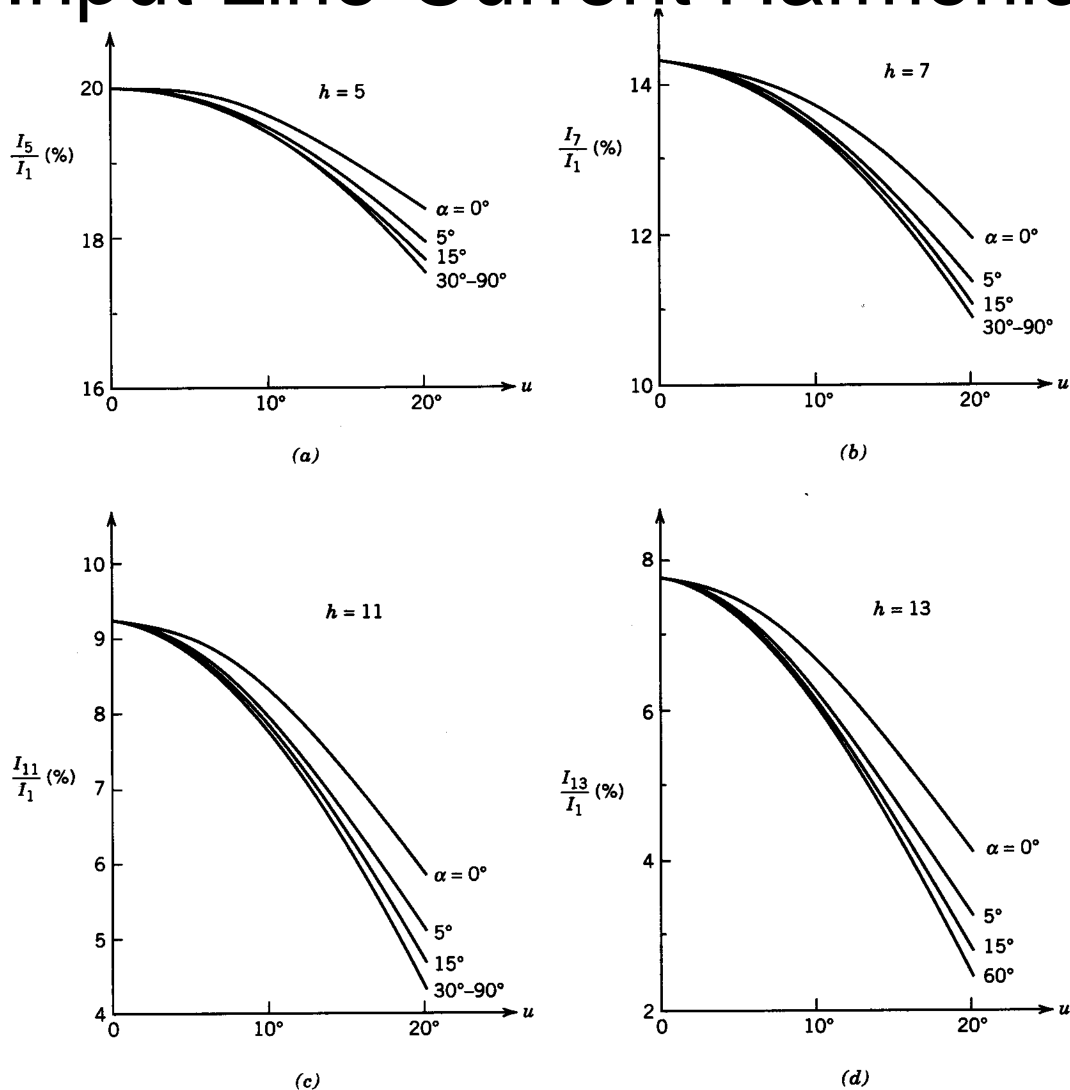

Figure 6-27 Normalized harmonic currents in the presence of L_s. (With permission from ref. 2).

- Finite ac-side inductance

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Input Line-Current Harmonics

Table 6-1 Typical and Idealized Harmonics

	h	5	7	11	13	17	19	23	25
Typical	I_h/I_1	0.17	0.10	0.04	0.03	0.02	0.01	0.01	0.01
Idealized	I_h/I_1	0.20	0.14	0.09	0.07	0.06	0.05	0.04	0.04

- Typical and idealized

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Three-Phase Thyristor Converter

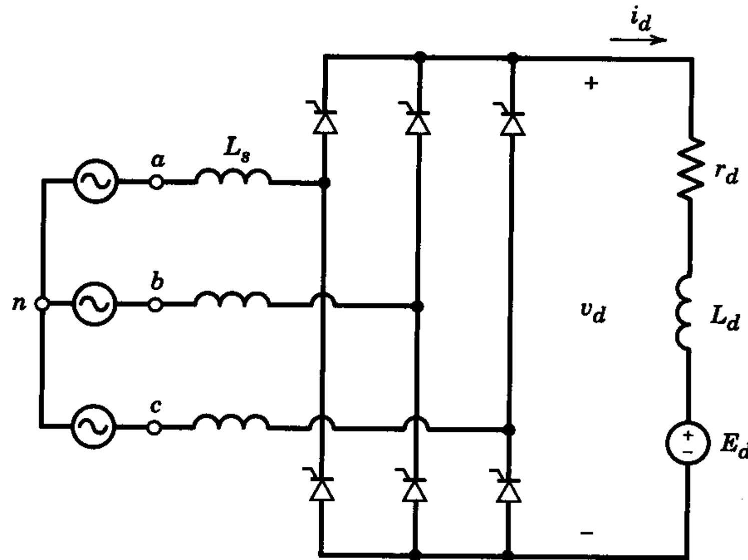

Figure 6-28 A practical thyristor converter.

- Realistic load

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Thyristor Converter Waveforms

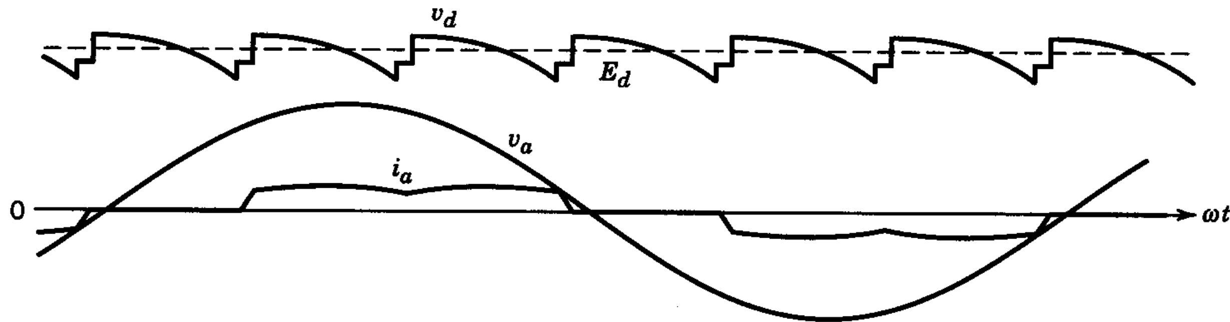

Figure 6-29 Waveforms in the converter of Fig. 6-28.

- Realistic load; continuous-conduction mode

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Thyristor Converter Waveforms

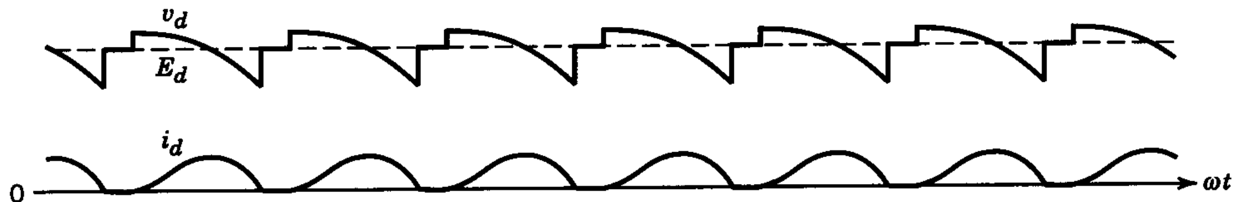

Figure 6-30 Waveforms in a discontinuous-current-conduction mode.

- Realistic load; discontinuous-conduction mode

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Thyristor Inverter

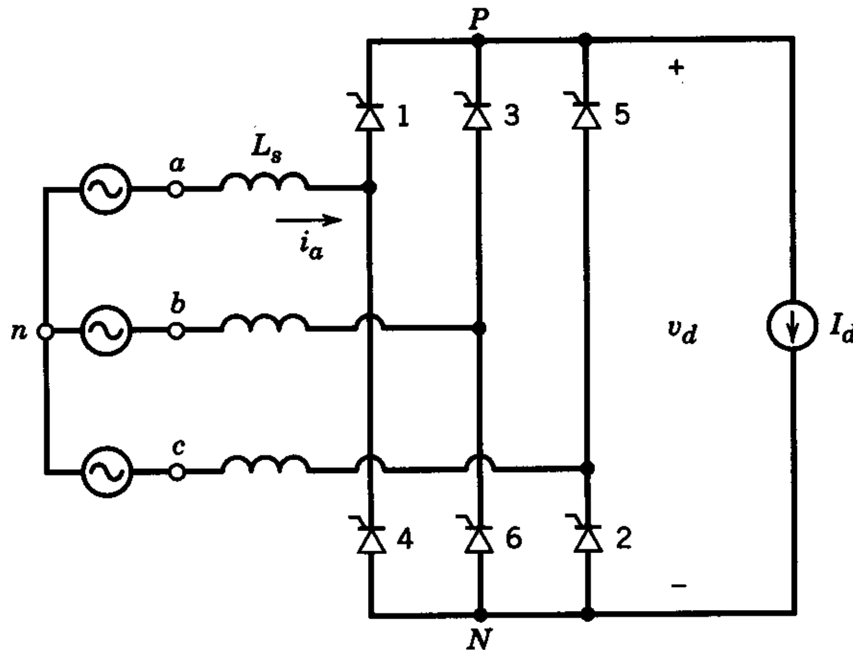

Figure 6-31 Inverter with a constant dc current.

- Constant dc current

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Thyristor Inverter Waveforms

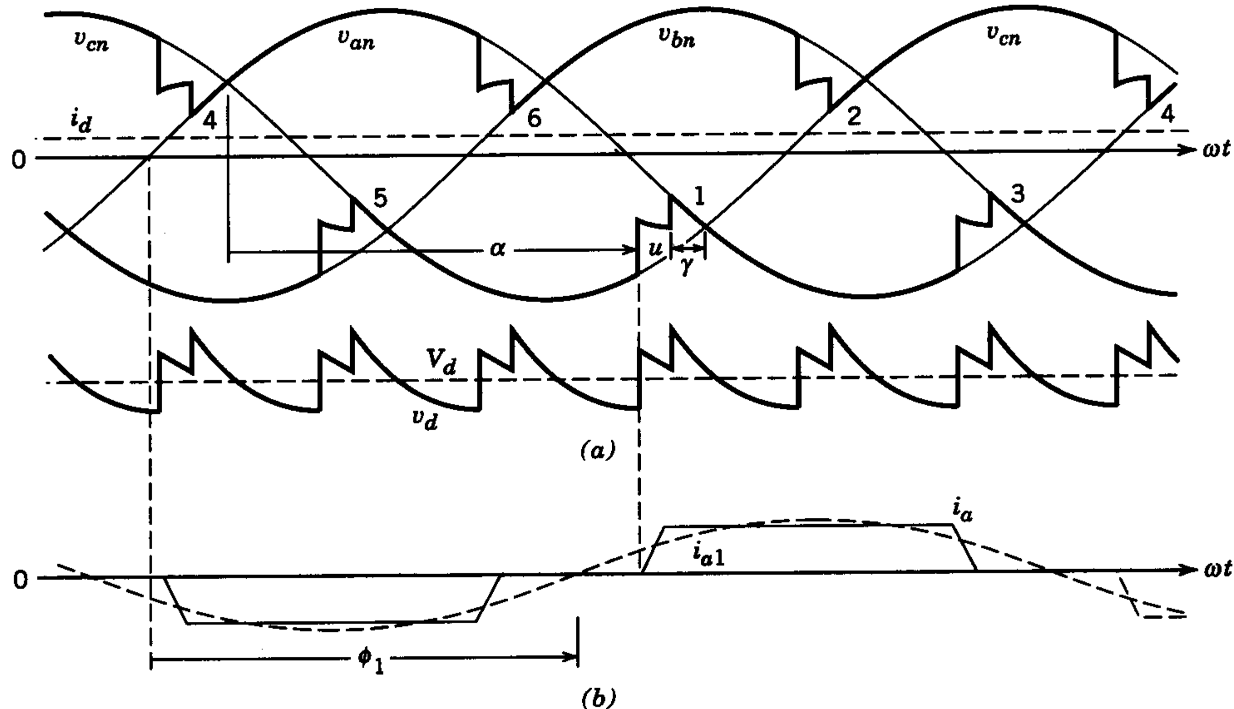

Figure 6-32 Waveforms in the inverter of Fig. 6-31.

- Finite ac-side inductance

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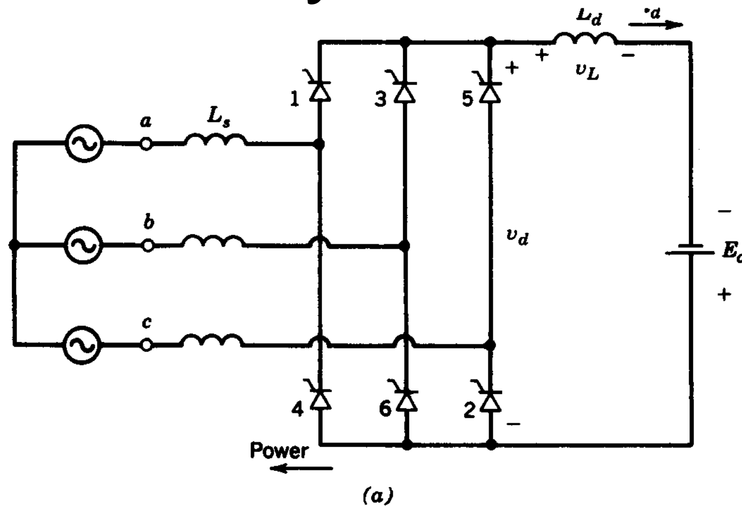
Thyristor Inverter



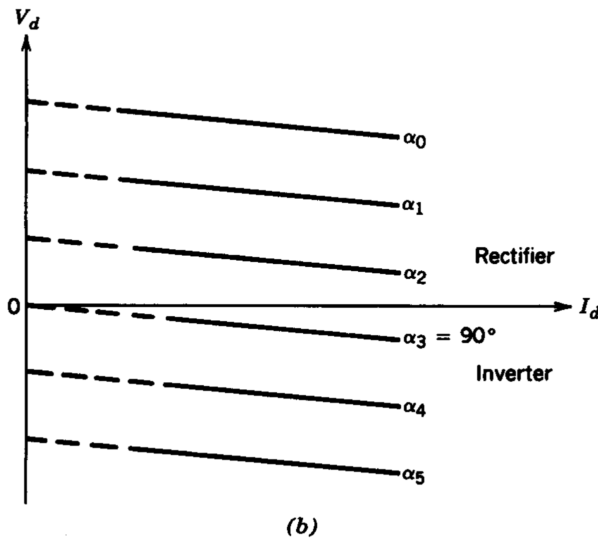


Figure 6-33 (*a*) Thyristor inverter with a dc voltage source. (*b*) V_d versus I_d.

- Family of curves at various values of delay angle

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Thyristor Inverter Operation

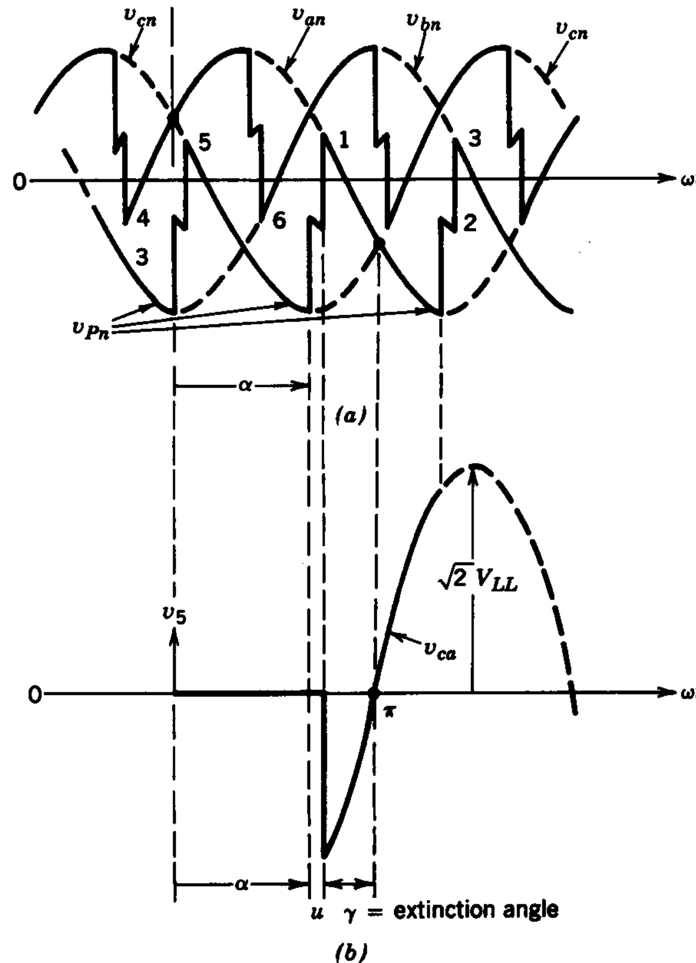

Figure 6-34 Voltage across a thyristor in the inverter mode.

- Importance of extinction angle

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Thyristor Converters: Voltage Notching

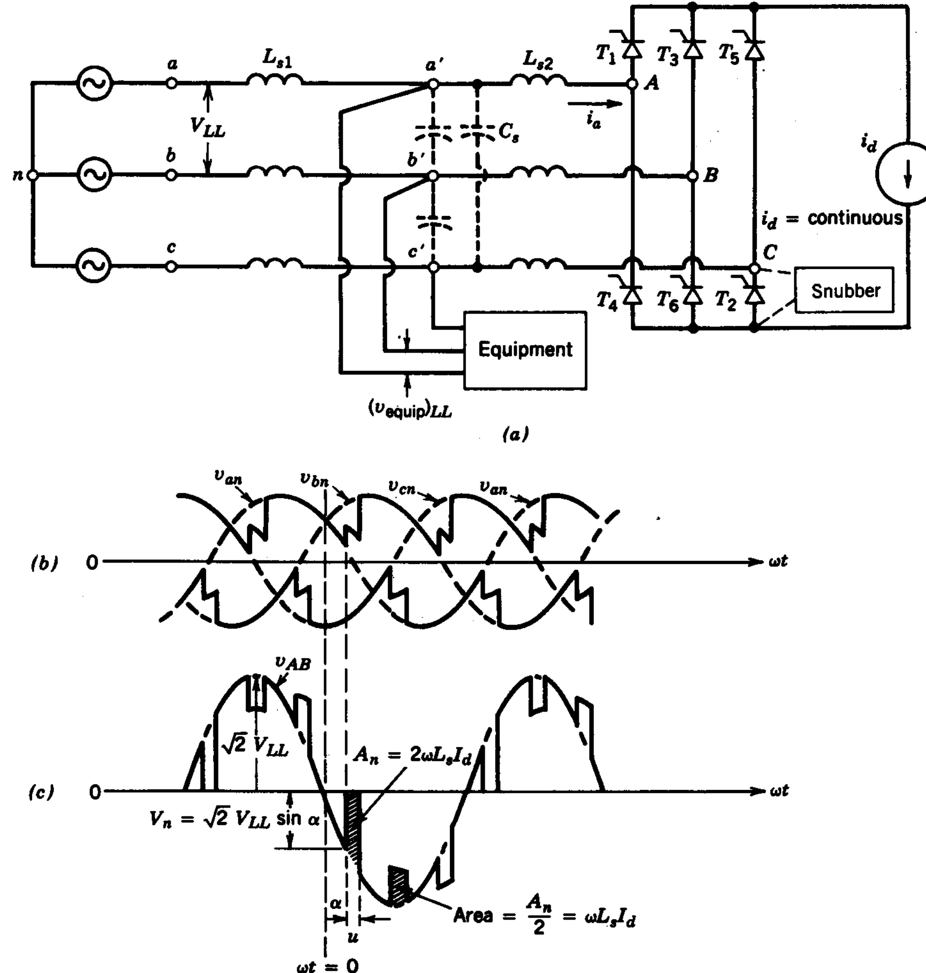

Figure 6-35 Line notching in other equipment voltage: (*a*) circuit, (*b*) phase voltages, (*c*) line-to-line voltage v_{AB}.

- Importance of external ac-side inductance

Limits on Notching and Distortion

Table 6-2 Line Notching and Distortion Limits for 460-V Systems

Class	*Line Notch Depth* ρ*(%)*	*Line Notch Area* *(V·μs)*	*Voltage Total Harmonic Distortion* *(%)*
Special applications	10	16,400	3
General system	20	22,800	5
Dedicated system	50	36,500	10

- Guidelines

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Thyristor Converter Representation

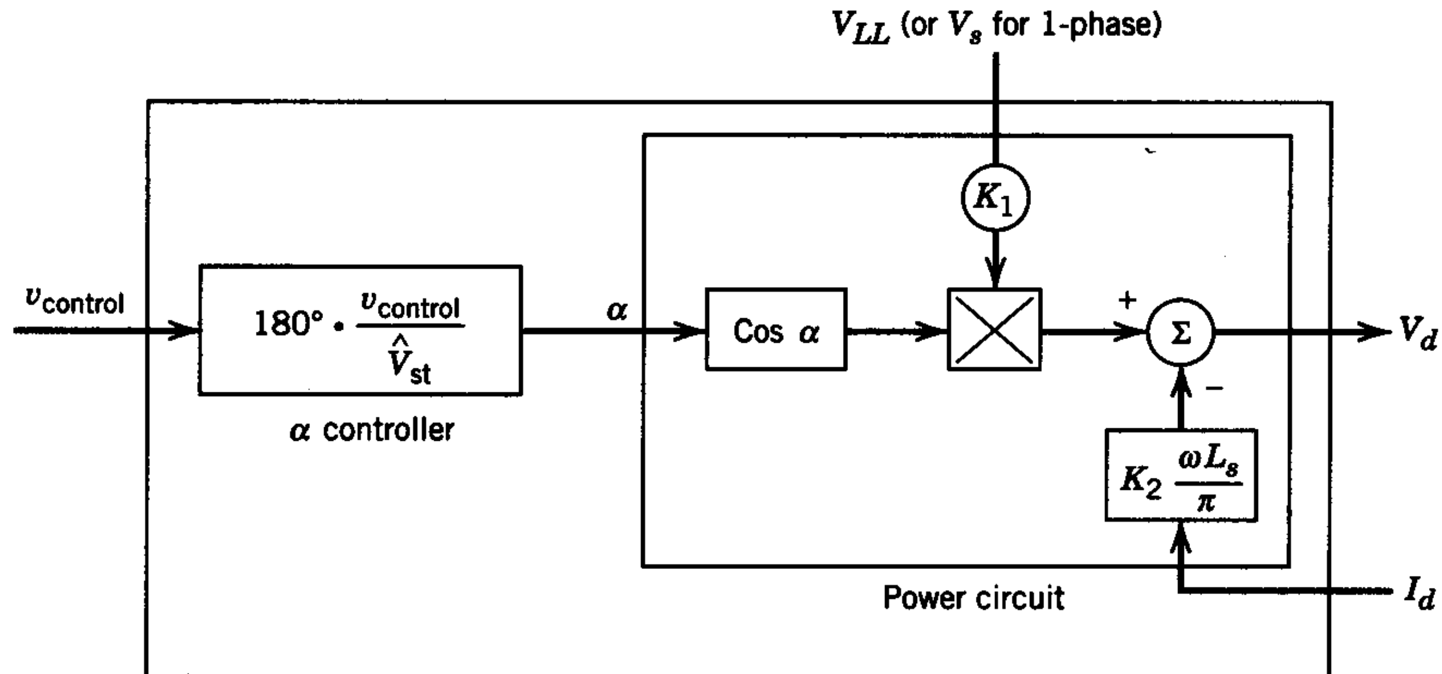

Figure 6-36 Summary of thyristor converter output voltage with a dc current I_d.

- Functional block diagram

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Chapter 7

DC-DC Switch-Mode Converters

Chapter 7 dc–dc Switch-Mode Converters **161**

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Problems *197*
References *199*

- dc-dc converters for switch-mode dc power supplies and dc-motor drives

Block Diagram of DC-DC Converters

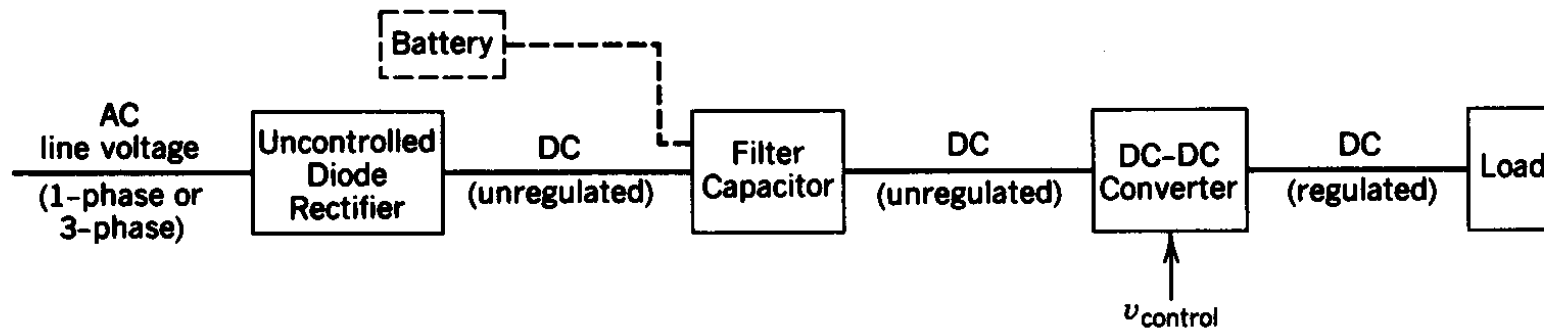

Figure 7-1 A dc–dc converter system.

- Functional block diagram

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Stepping Down a DC Voltage

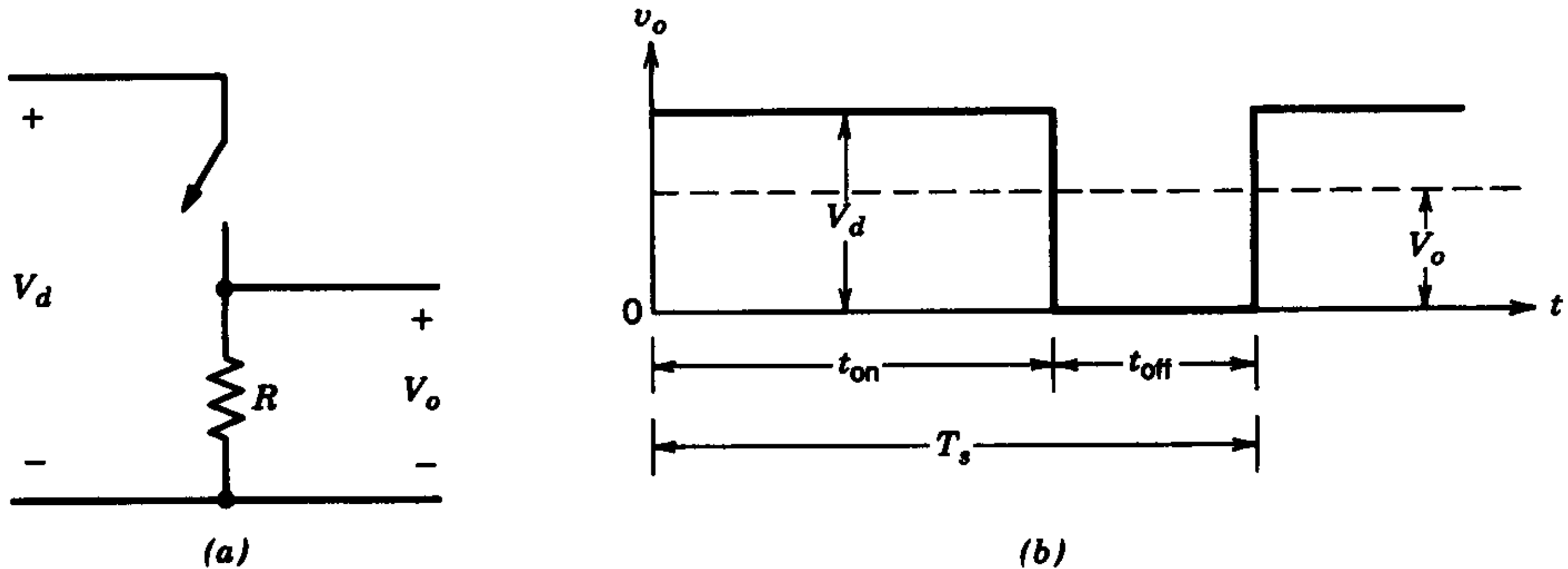

Figure 7-2 Switch-mode dc–dc conversion.

- A simple approach that shows the evolution

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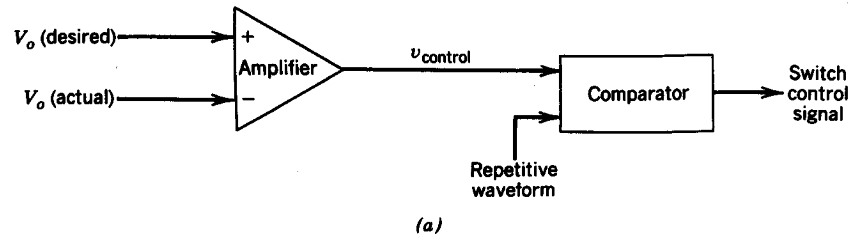
Pulse-Width Modulation in DC-DC Converters



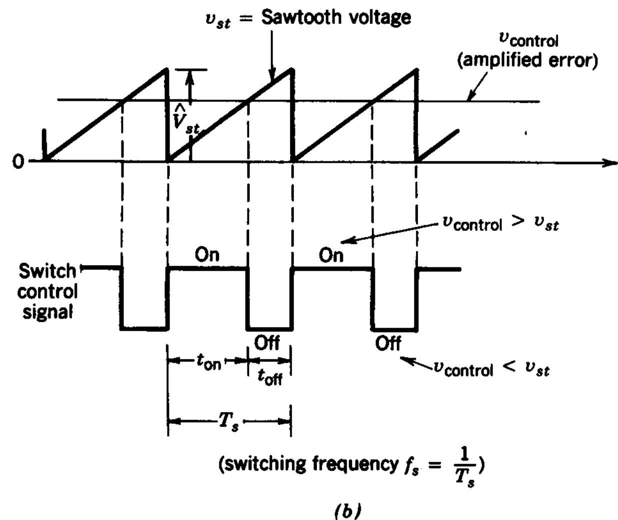


Figure 7-3 Pulse-width modulator: (*a*) block diagram; (*b*) comparator signals.

- Role of PWM

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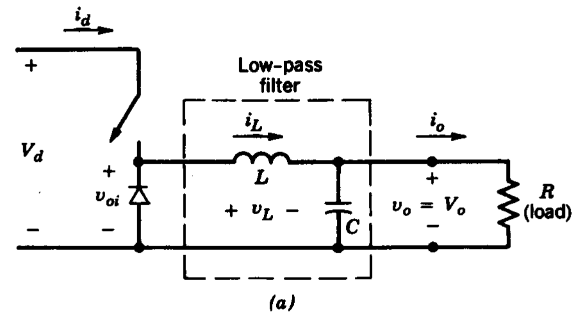
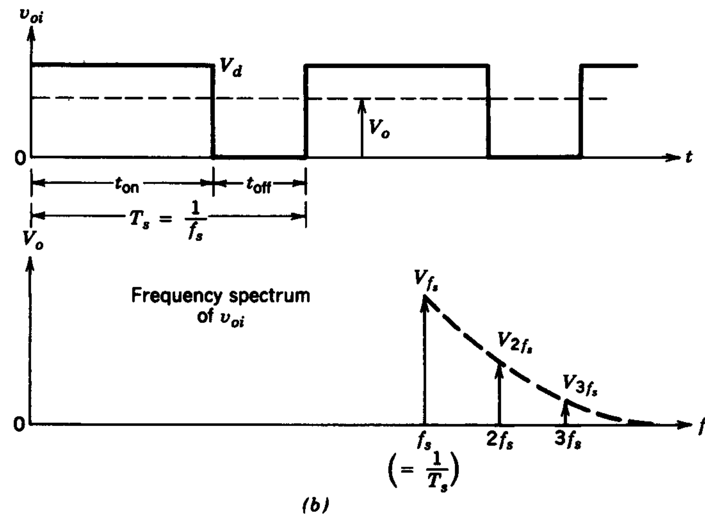
Step-Down DC-DC Converter





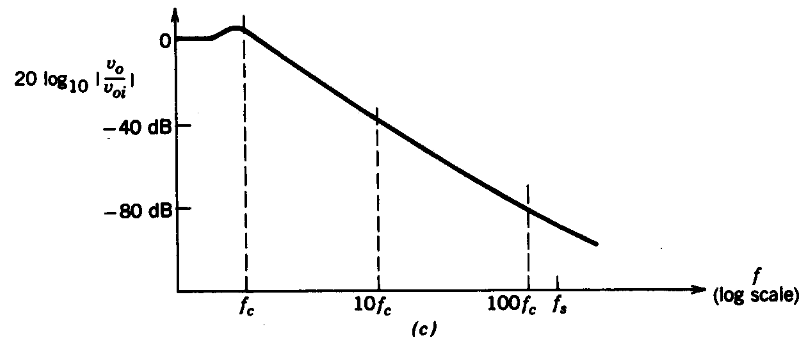


Figure 7-4 Step-down dc–dc converter.

- Pulsating input to the low-pass filter

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Step-Down DC-DC Converter: Waveforms

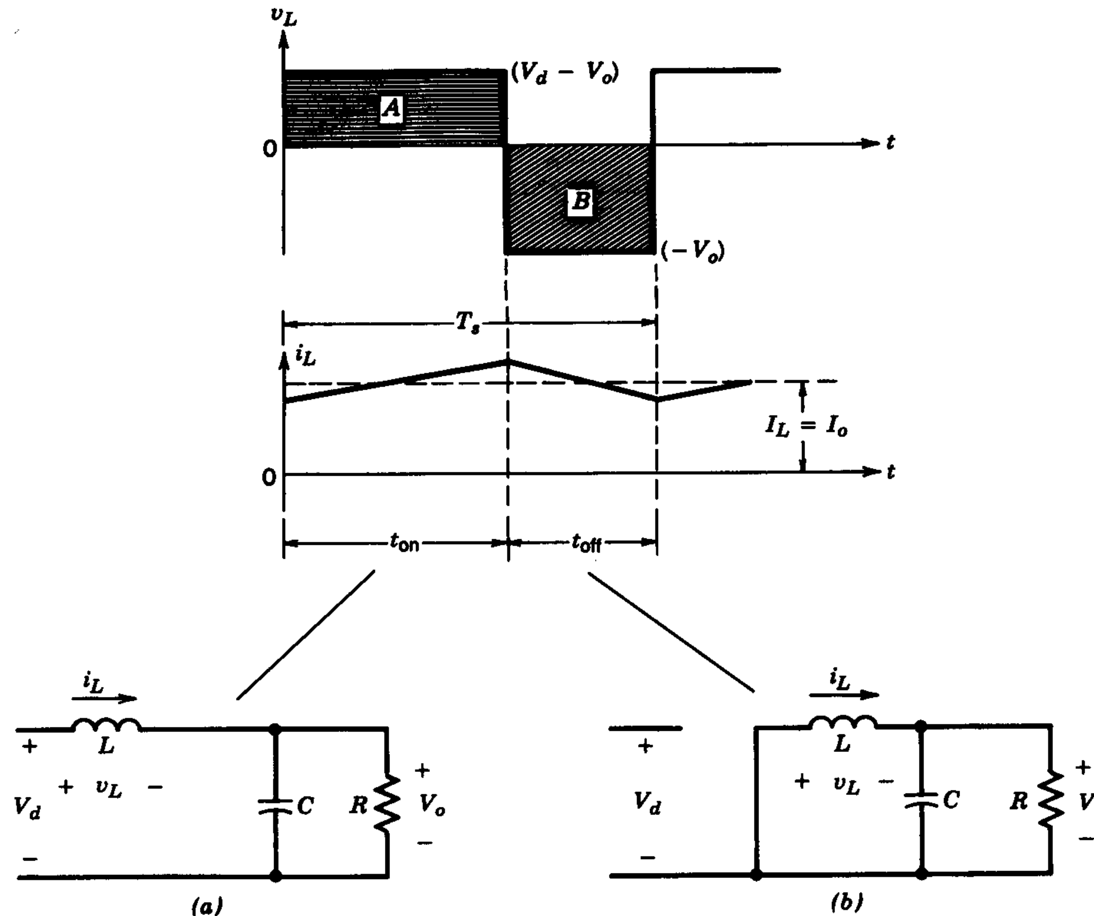

Figure 7-5 Step-down converter circuit states (assuming i_L flows continuously): (*a*) switch on; (*b*) switch off.

- Steady state; inductor current flows continuously

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Step-Down DC-DC Converter: Waveforms at the boundary of Cont./Discont. Conduction

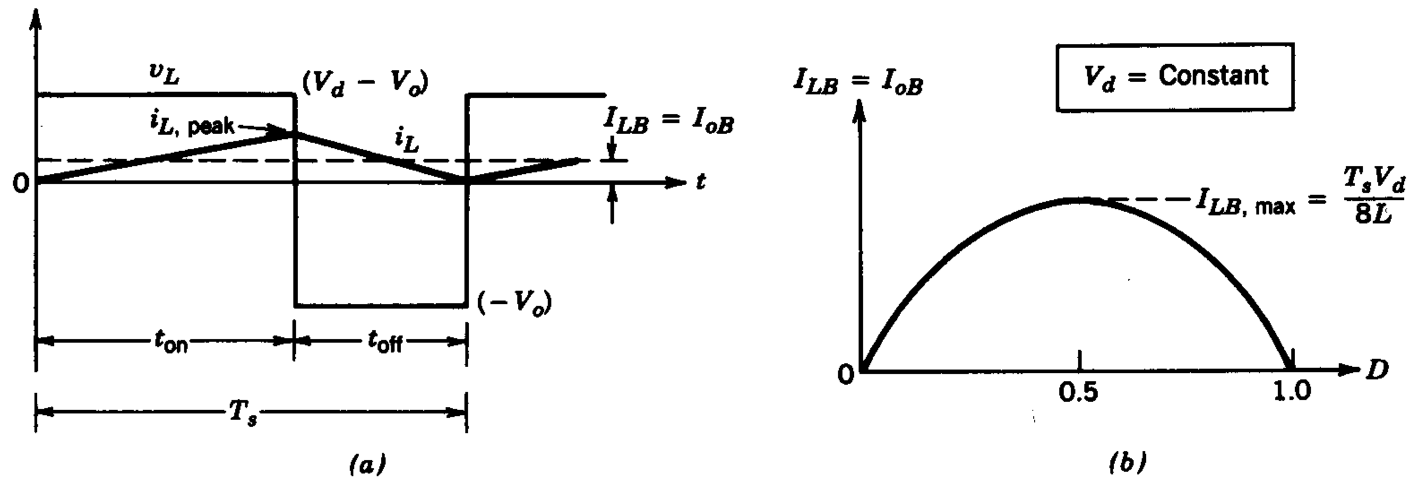

Figure 7-6 Current at the boundary of continuous–discontinuous conduction: (*a*) current waveform; (*b*) I_{LB} versus D keeping V_d constant.

- Critical current below which inductor current becomes discontinuous

Step-Down DC-DC Converter: Discontinuous Conduction Mode

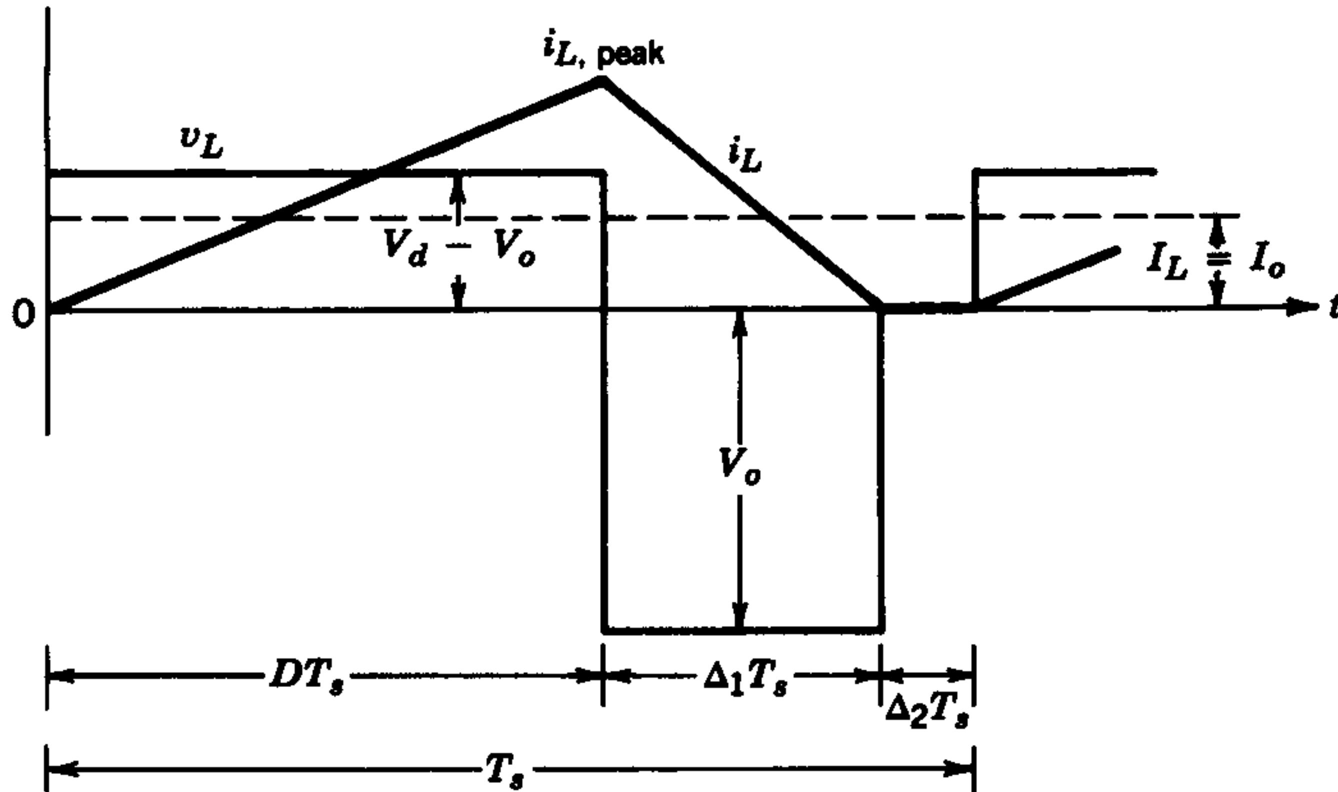

Figure 7-7 Discontinuous conduction in step-down converter.

- Steady state; inductor current discontinuous

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Step-Down DC-DC Converter: Limits of Cont./Discont. Conduction

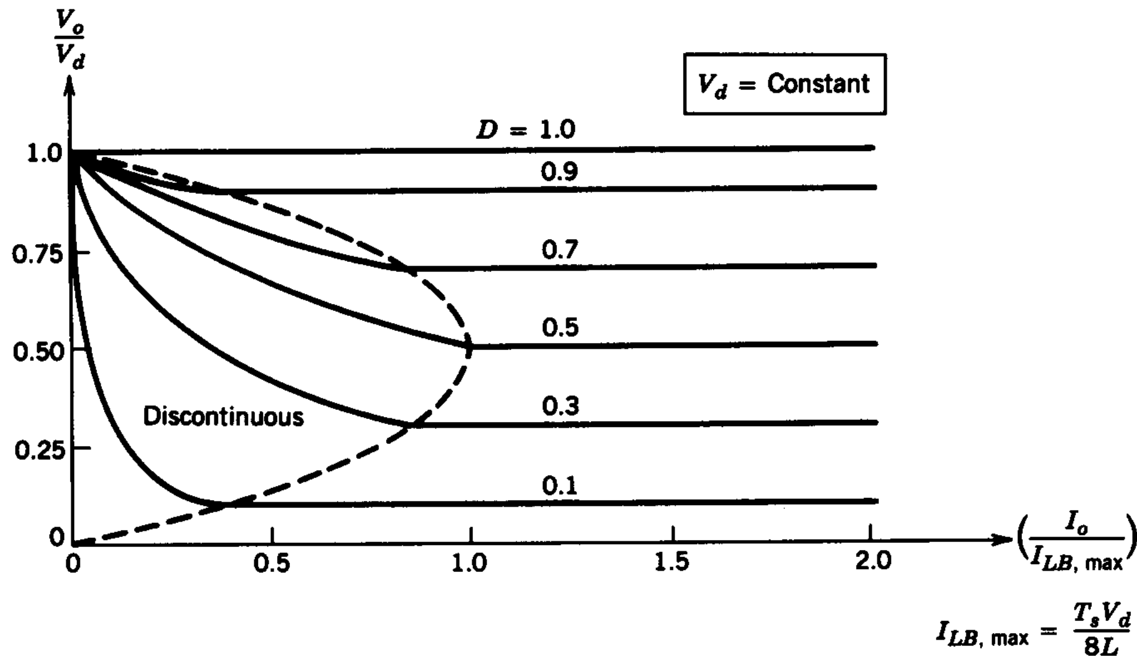

Figure 7-8 Step-down converter characteristics keeping V_d constant.

- The duty-ratio of 0.5 has the highest value of the critical current

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Step-Down DC-DC Converter: Limits of Cont./Discont. Conduction

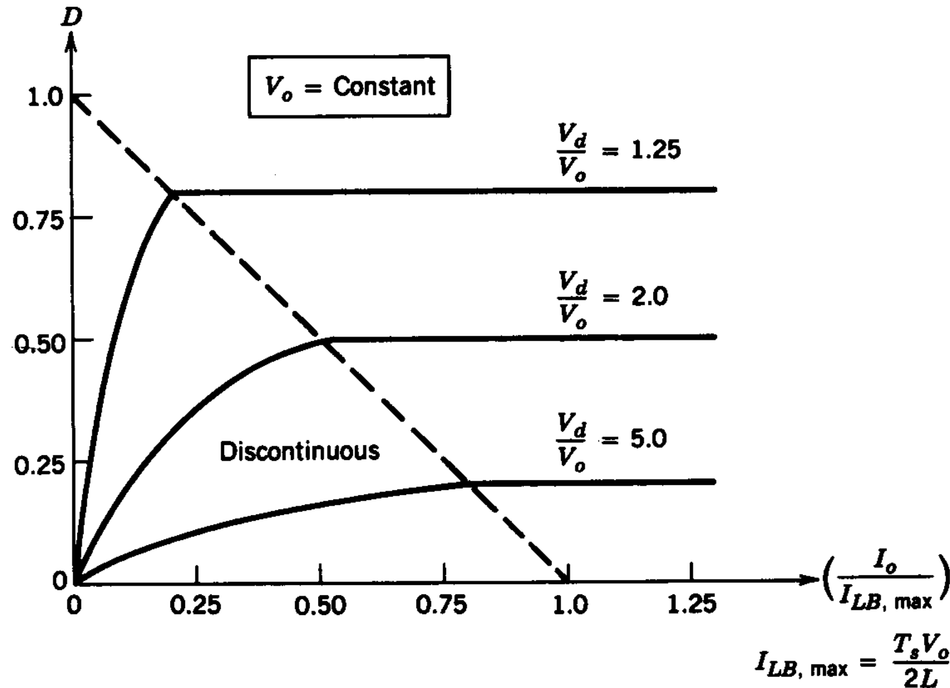

Figure 7-9 Step-down converter characteristics keeping V_o constant.

- Output voltage is kept constant

Step-Down Conv.: Output Voltage Ripple

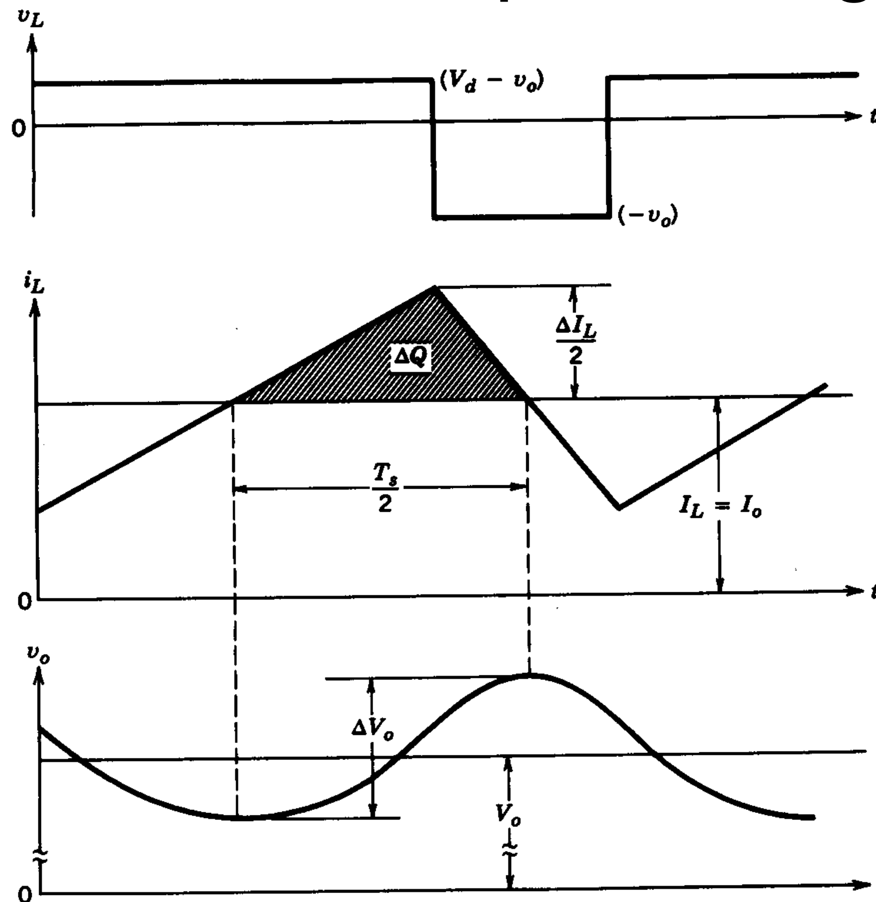

Figure 7-10 Output voltage ripple in a step-down converter.

- ESR is assumed to be zero

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Step-Up DC-DC Converter

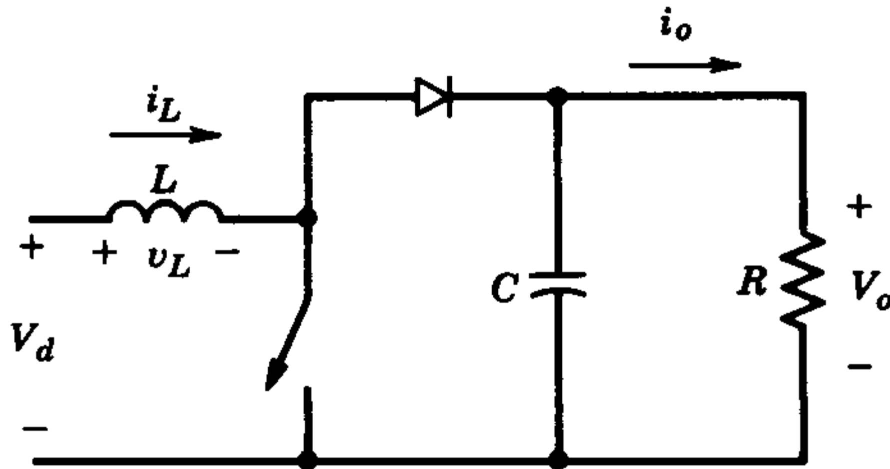

Figure 7-11 Step-up dc–dc converter.

- Output voltage must be greater than the input

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Step-Up DC-DC Converter Waveforms

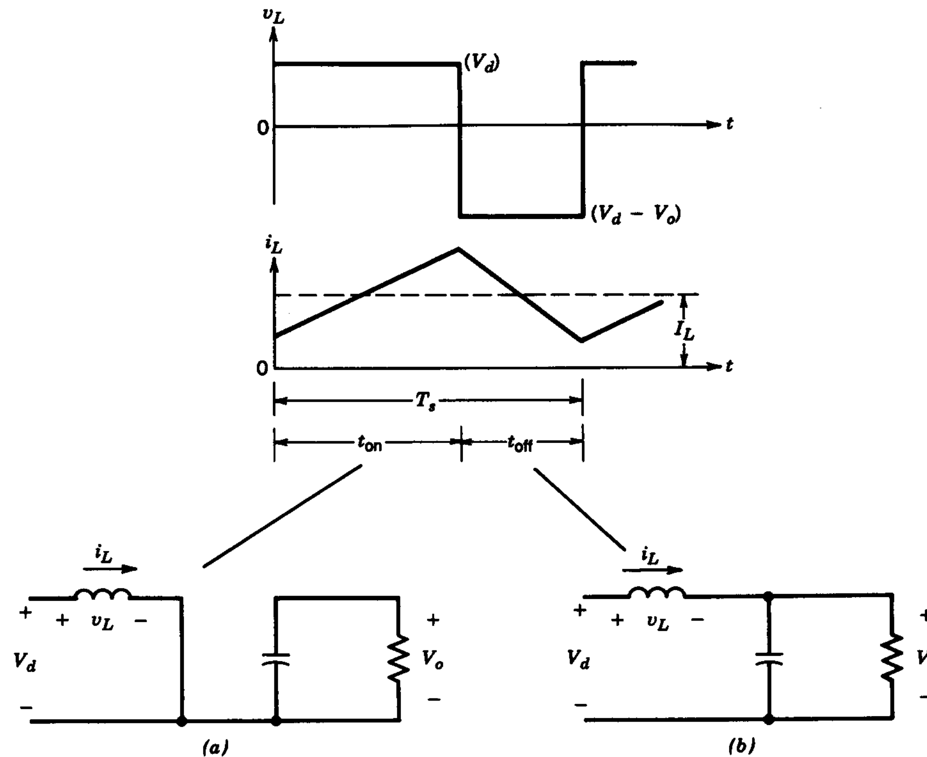

Figure 7-12 Continuous-conduction mode: (*a*) switch on; (*b*) switch off.

- Continuous current conduction mode

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Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

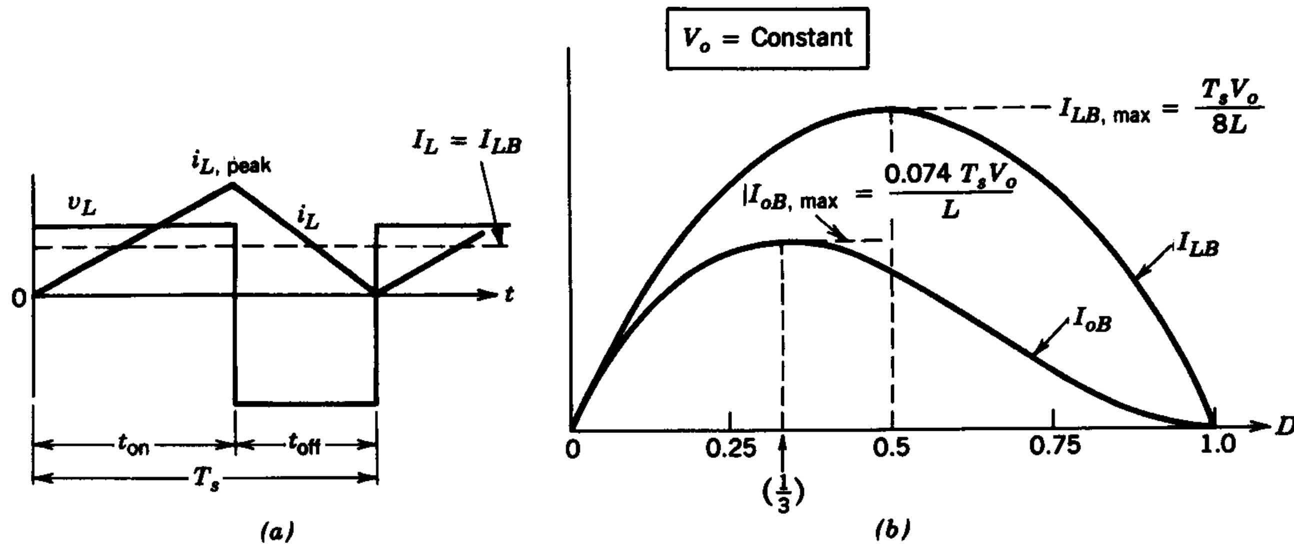

Figure 7-13 Step-up dc–dc converter at the boundary of continuous–discontinuous conduction.

- The output voltage is held constant

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Step-Up DC-DC Converter: Discont. Conduction

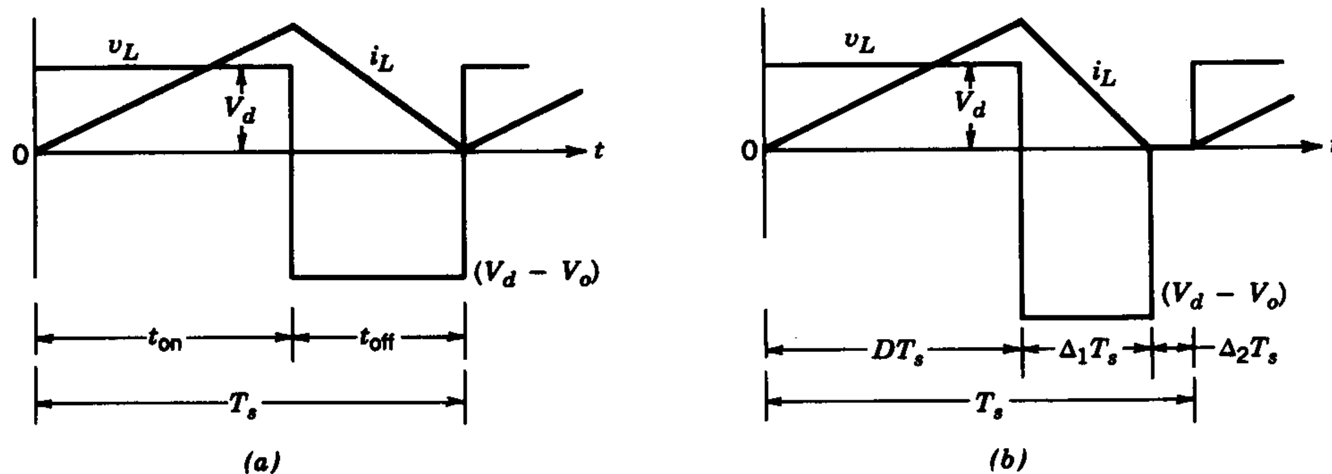

Figure 7-14 Step-up converter waveforms: (*a*) at the boundary of continuous–discontinuous conduction; (*b*) at discontinuous conduction.

- Occurs at light loads

Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

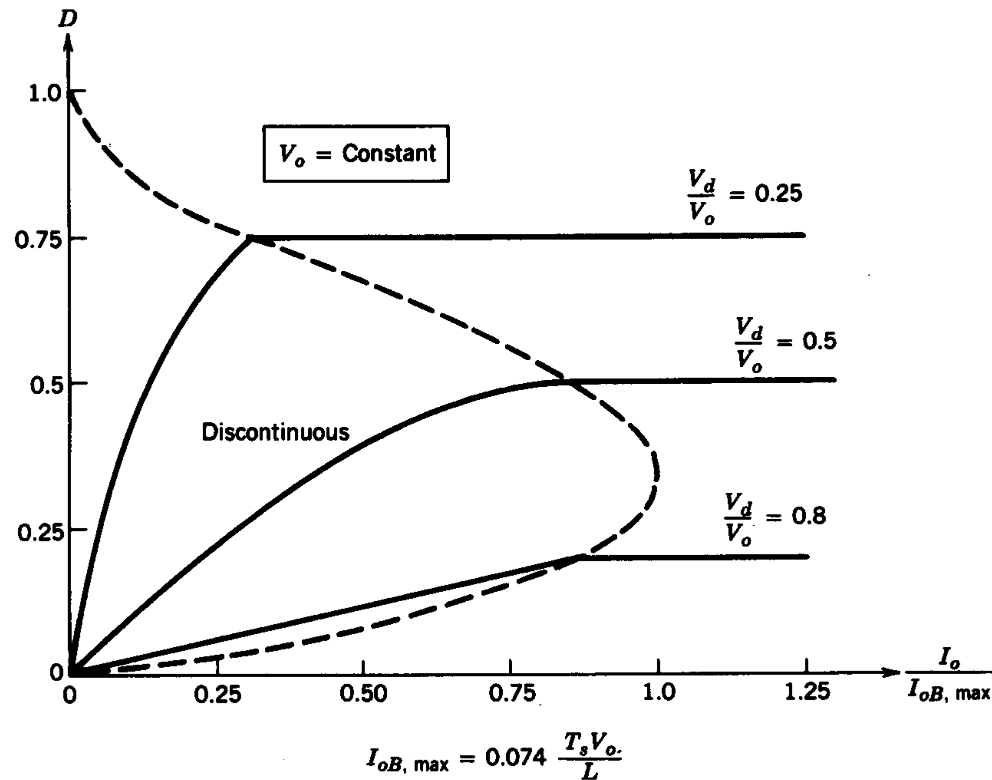

Figure 7-15 Step-up converter characteristics keeping V_o constant.

- The output voltage is held constant

Step-Up DC-DC Converter: Effect of Parasitics

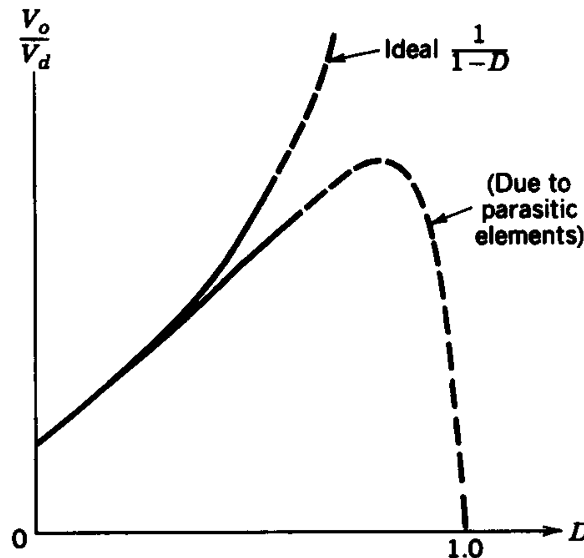

Figure 7-16 Effect of parasitic elements on voltage conversion ratio (step-up converter).

- The duty-ratio is generally limited before the parasitic effects become significant

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Step-Up DC-DC Converter Output Ripple

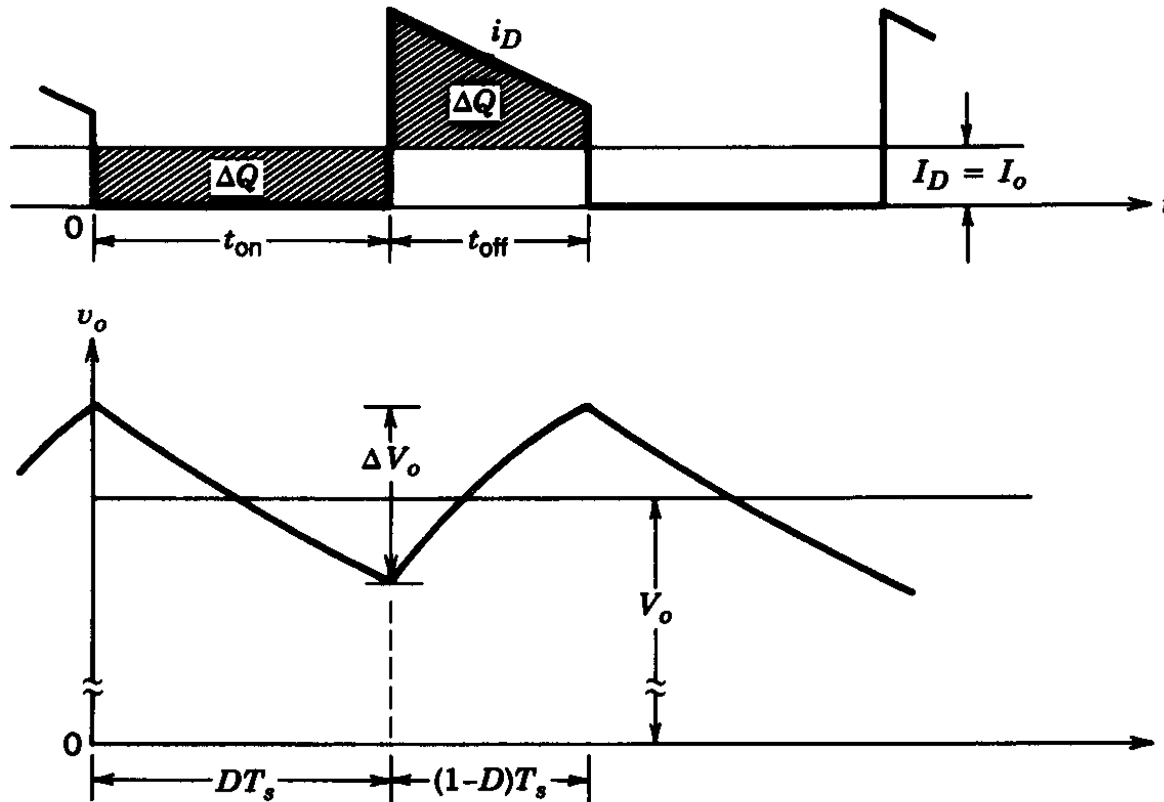

Figure 7-17 Step-up converter output voltage ripple.

- ESR is assumed to be zero

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Step-Down/Up DC-DC Converter

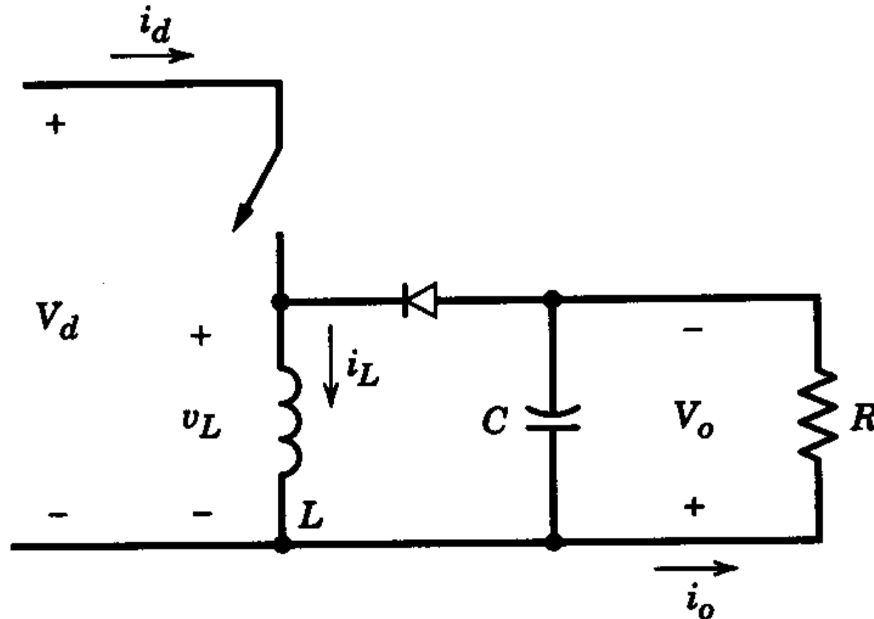

Figure 7-18 **Buck–boost converter.**

- The output voltage can be higher or lower than the input voltage

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Step-Up DC-DC Converter: Waveforms

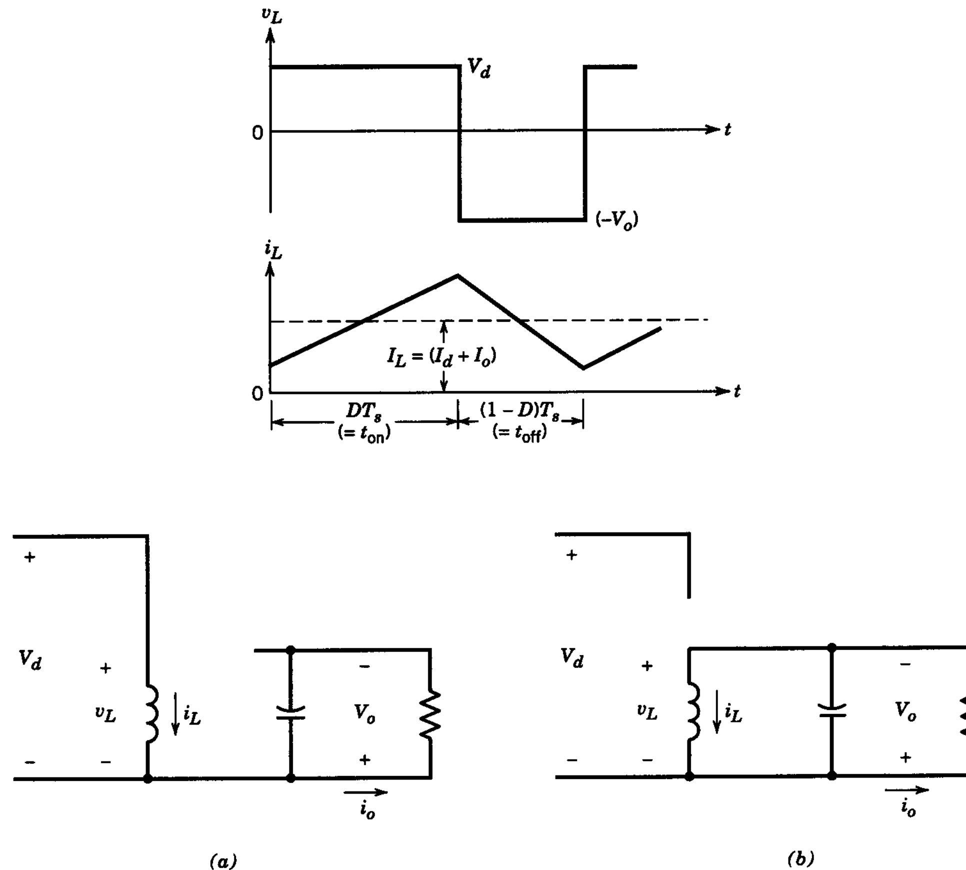

Figure 7-19 Buck–boost converter ($i_L > 0$): (a) switch on; (b) switch off.

- Continuation conduction mode

Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

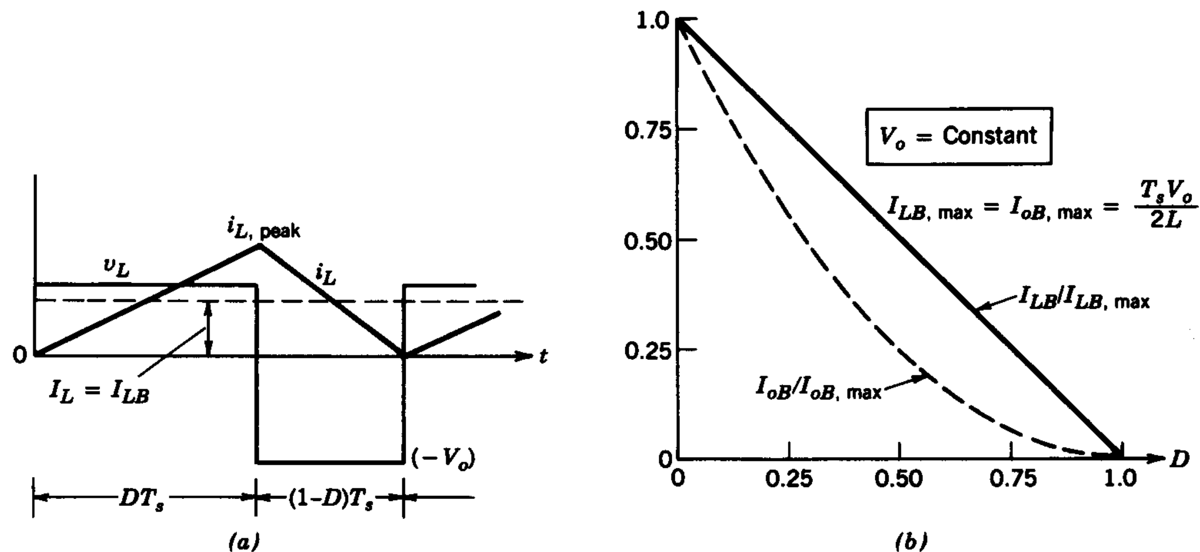

Figure 7-20 Buck–boost converter: boundary of continuous–discontinuous conduction.

- The output voltage is held constant

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Step-Up DC-DC Converter: Discontinuous Conduction Mode

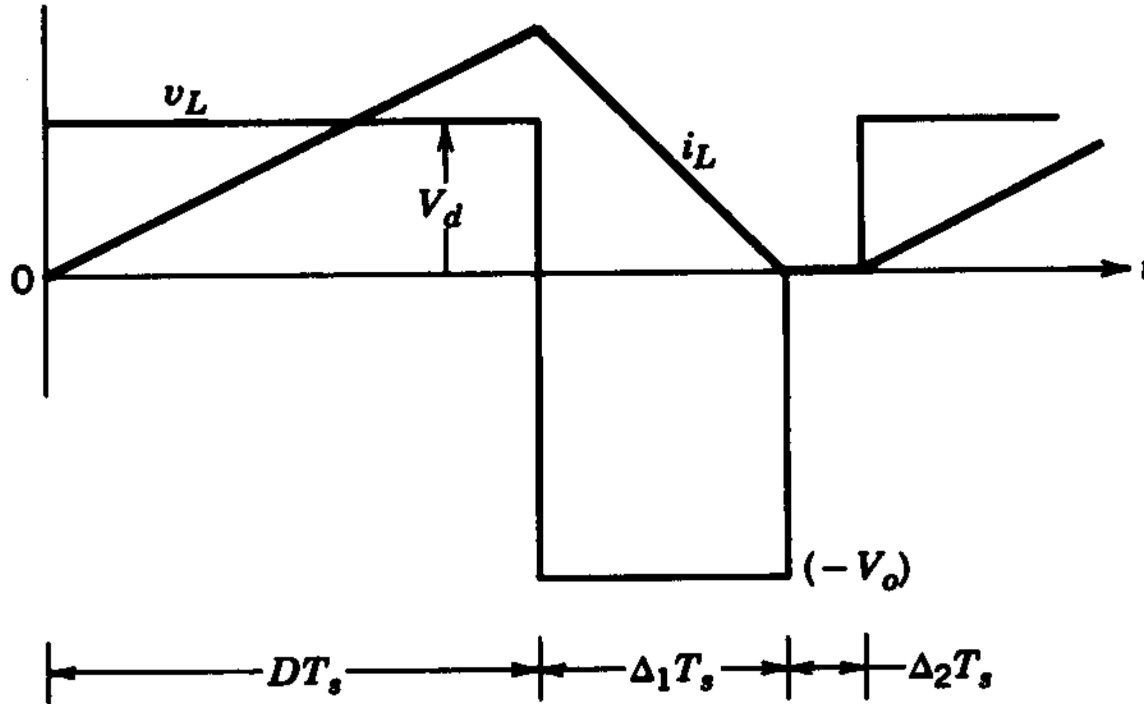

Figure 7-21 Buck–boost converter waveforms in a discontinuous-conduction mode.

- This occurs at light loads

Step-Up DC-DC Converter: Limits of Cont./Discont. Conduction

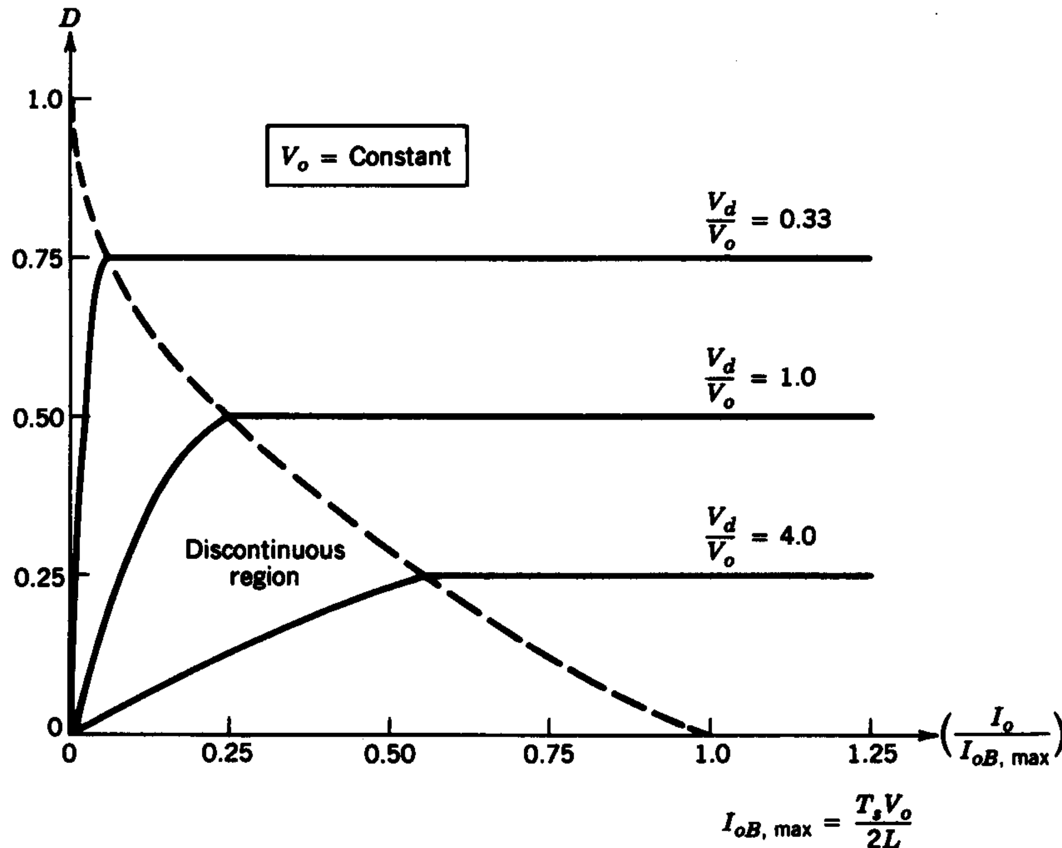

Figure 7-22 Buck–boost converter characteristics keeping V_o constant.

- The output voltage is held constant

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Step-Up DC-DC Converter: Effect of Parasitics

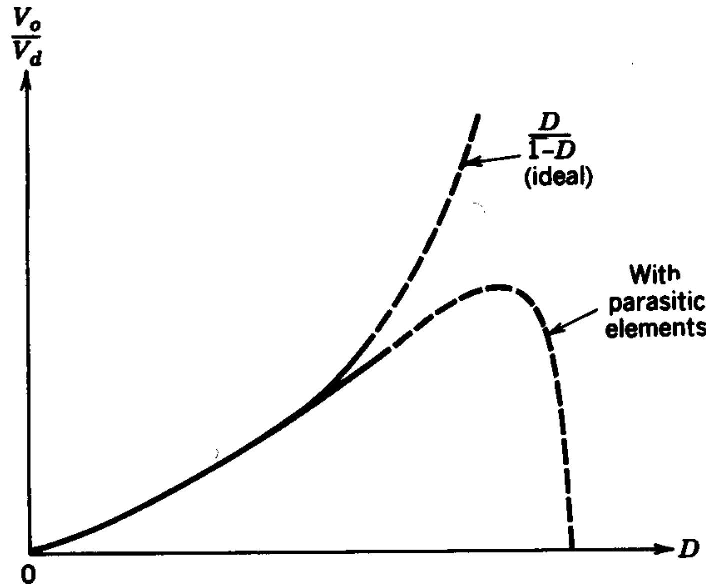

Figure 7-23 Effect of parasitic elements on the voltage conversion ratio in a buck–boost converter.

- The duty-ratio is limited to avoid these parasitic effects from becoming significant

Step-Up DC-DC Converter: Output Voltage Ripple

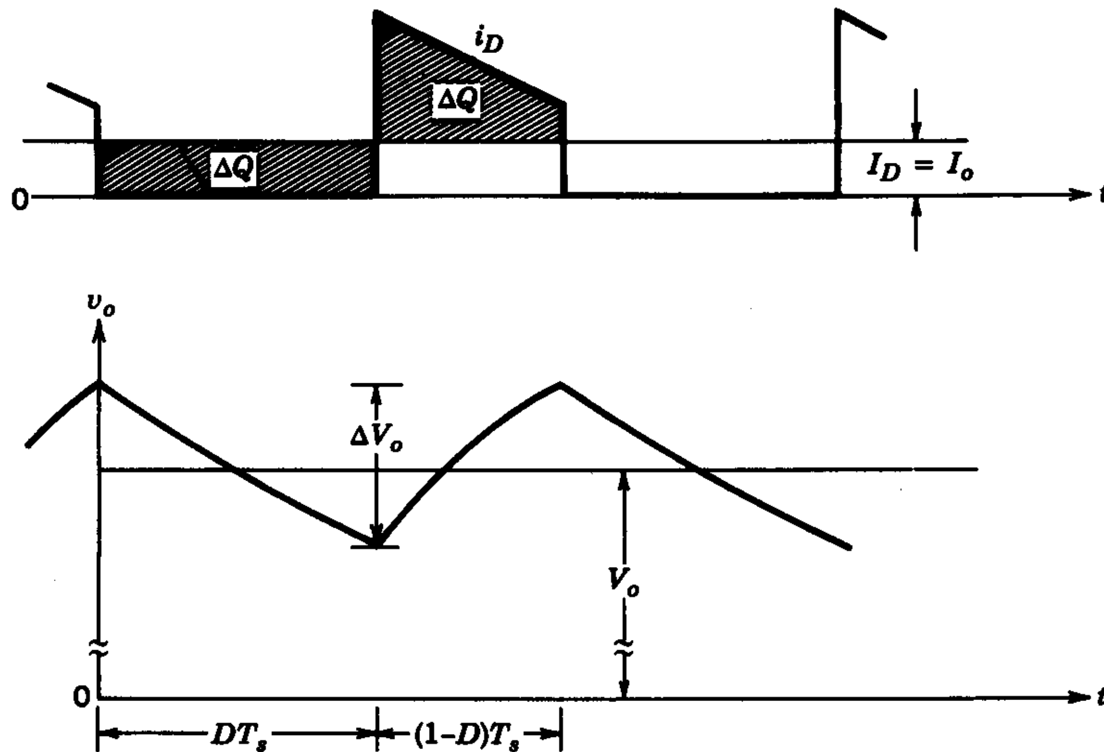

Figure 7-24 Output voltage ripple in a buck–boost converter.

- ESR is assumed to be zero

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Cuk DC-DC Converter

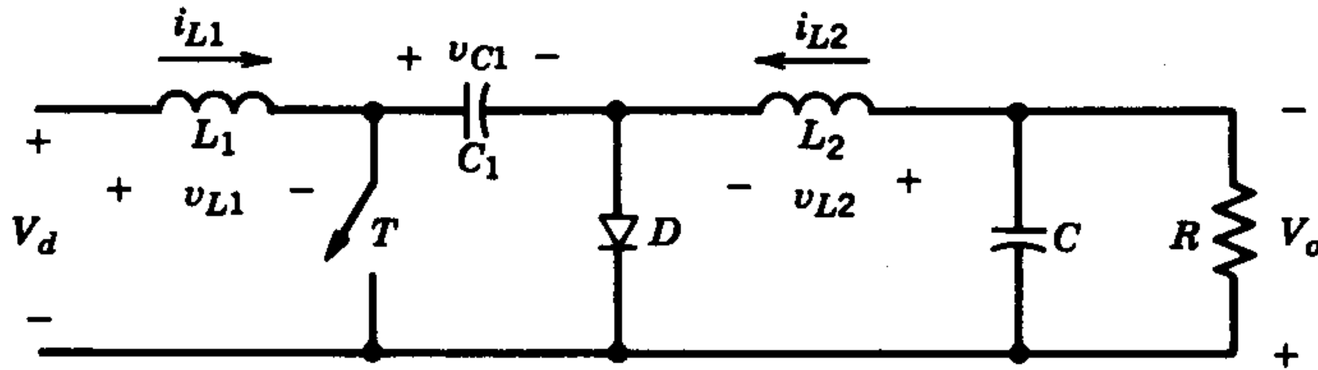

Figure 7-25 Cúk converter.

• The output voltage can be higher or lower than the input voltage

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Cuk DC-DC Converter: Waveforms

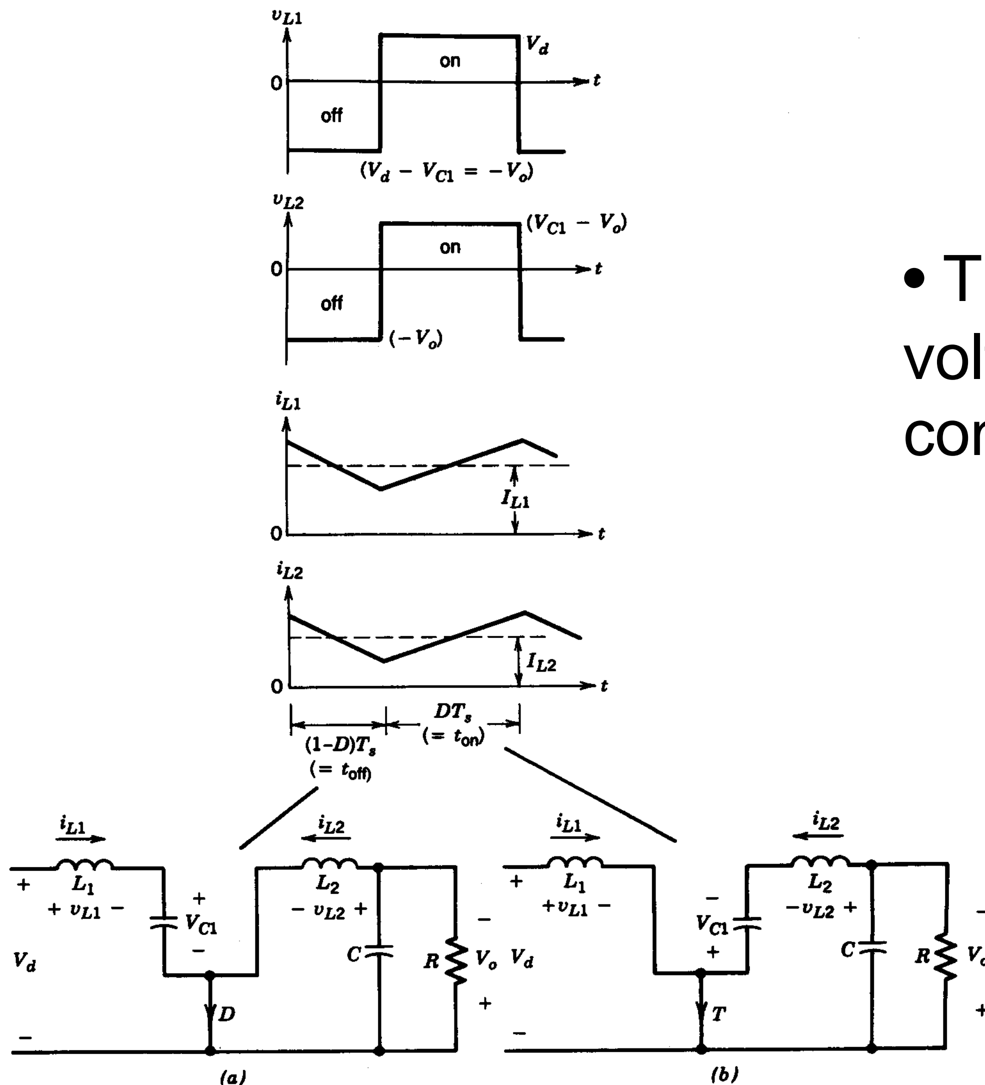

Figure 7-26 Cúk converter waveforms: (*a*) switch off; (*b*) switch on.

- The capacitor voltage is assumed constant

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Converter for DC-Motor Drives

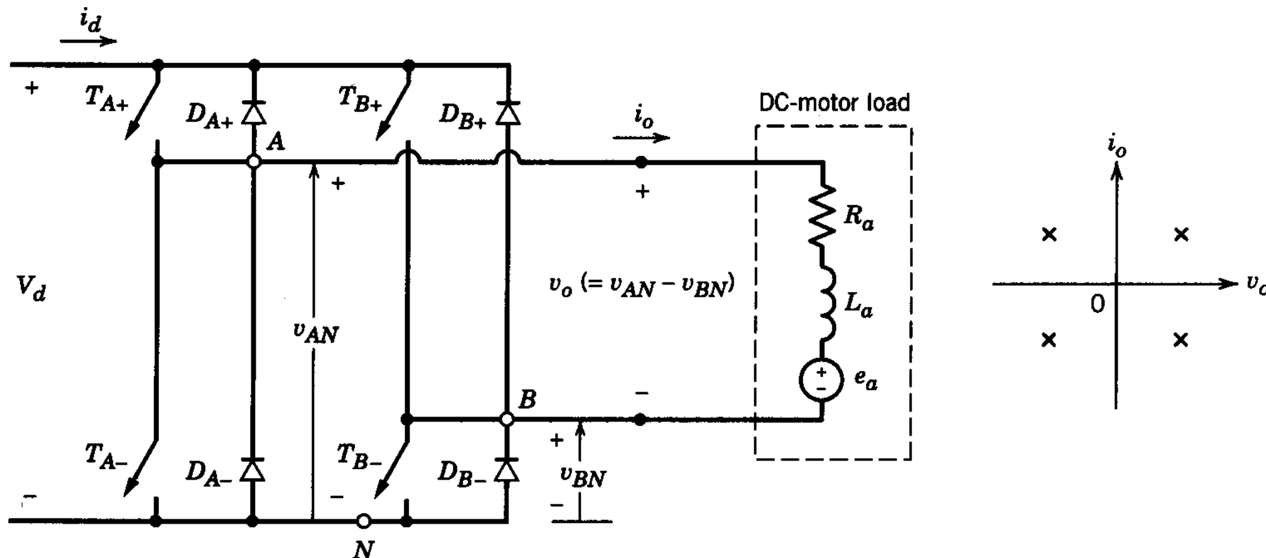

Figure 7-27 Full-bridge dc−dc converter.

- Four quadrant operation is possible

Converter Waveforms

- Bi-polar voltage switching

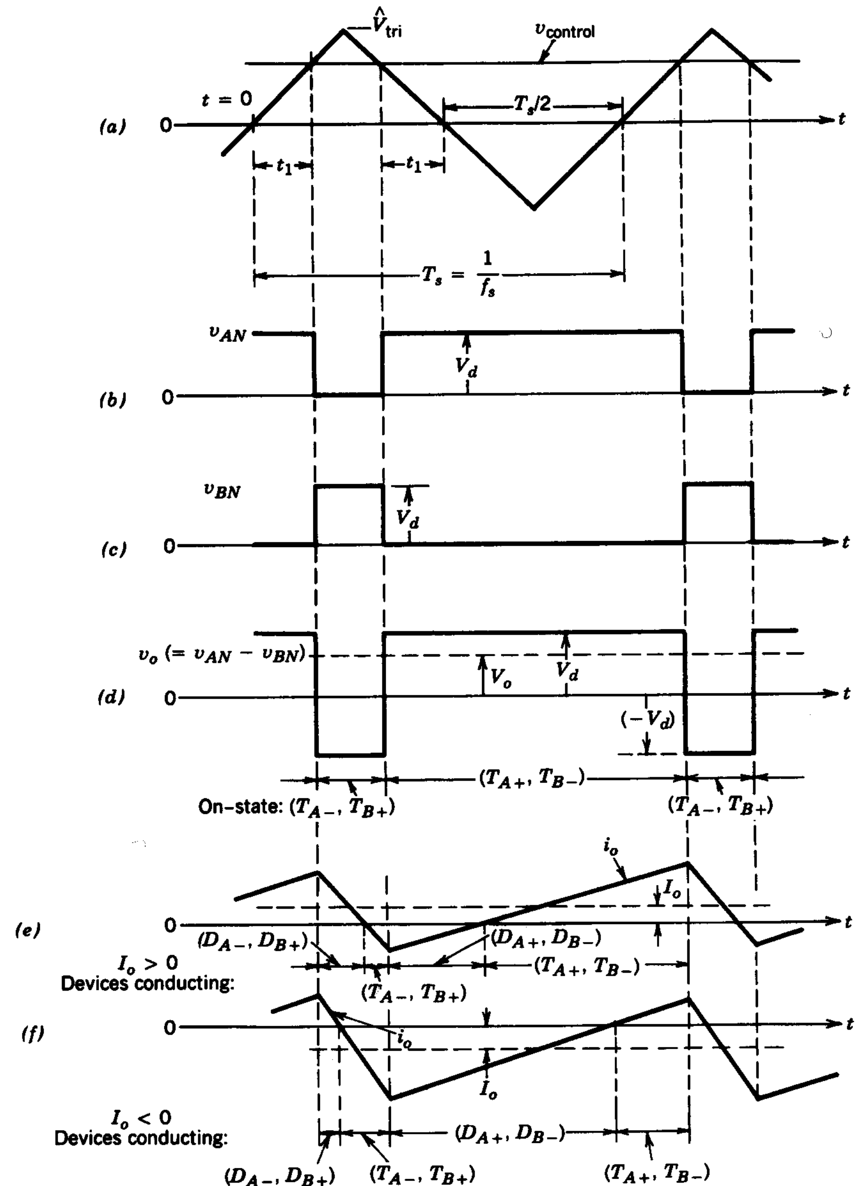

Figure 7-28 PWM with bipolar voltage switching.

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Converter Waveforms

- Uni-polar voltage switching

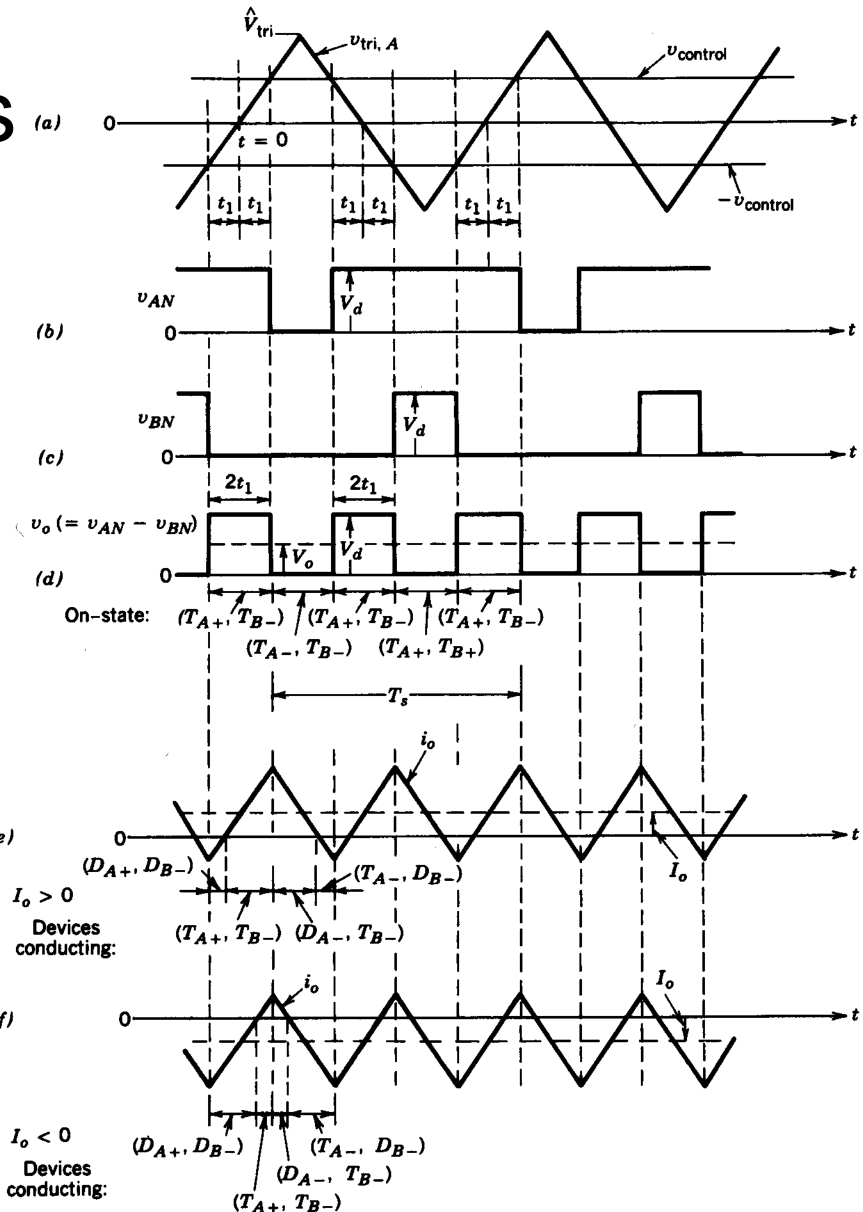

Figure 7-29 PWM with unipolar voltage switching.

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Output Ripple in Converters for DC-Motor Drives

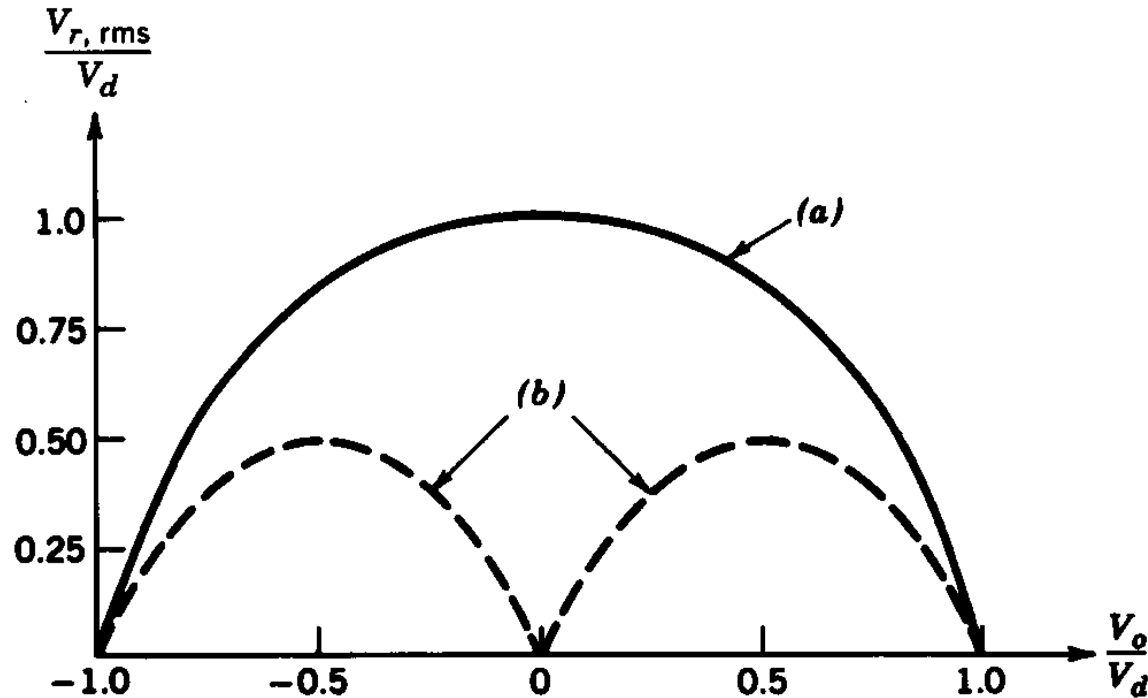

Figure 7-30 $V_{r,\text{rms}}$ in a full-bridge converter using PWM: (*a*) with bipolar voltage switching; (*b*) with unipolar voltage switching.

- bi-polar and uni-polar voltage switching

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Switch Utilization in DC-DC Converters

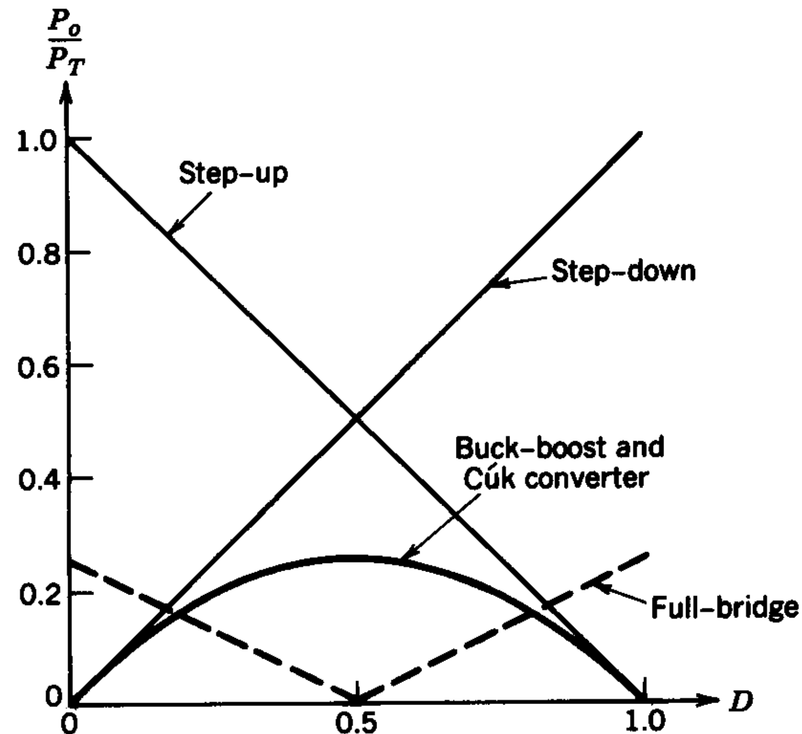

Figure 7-31 Switch utilization in dc–dc converters.

- It varies significantly in various converters

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Equivalent Circuits in DC-DC Converters

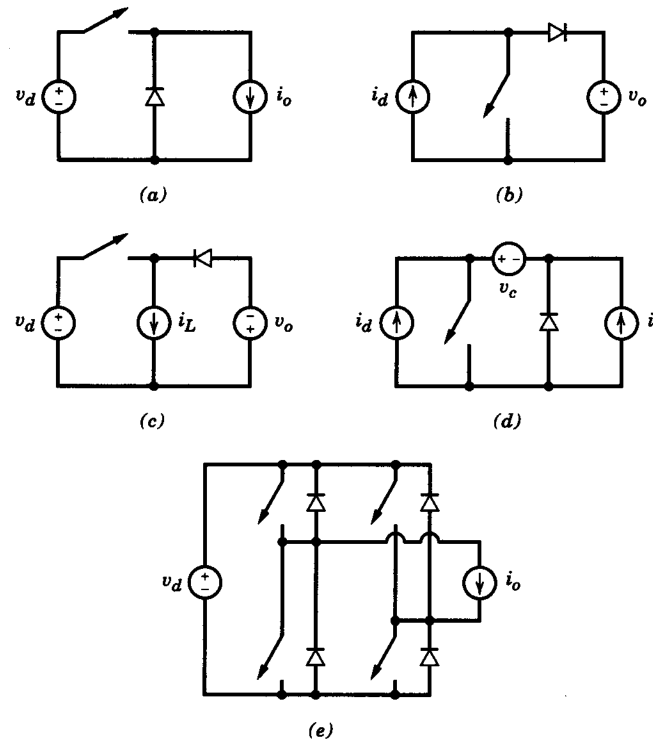

Figure 7-32 Converter equivalent circuits: (*a*) step-down; (*b*) step-up; (*c*) step-down/step-up; (*d*) Cúk; (*e*) full-bridge.

- replacing inductors and capacitors by current and voltage sources, respectively

Reversing the Power Flow in DC-DC Conv.

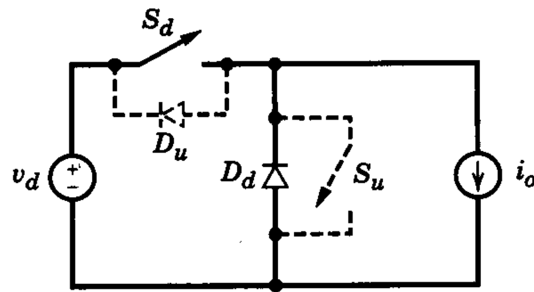

Figure 7-33 Reversible power flow with reversible direction of the output current i_o.

- For power flow from right to left, the input current direction should also reverse

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Chapter 8

Switch-Mode DC-AC Inverters

Chapter 8 Switch-Mode dc–ac Inverters: dc ↔ Sinusoidal ac **200**

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- converters for ac motor drives and uninterruptible power supplies

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Switch-Mode DC-AC Inverter

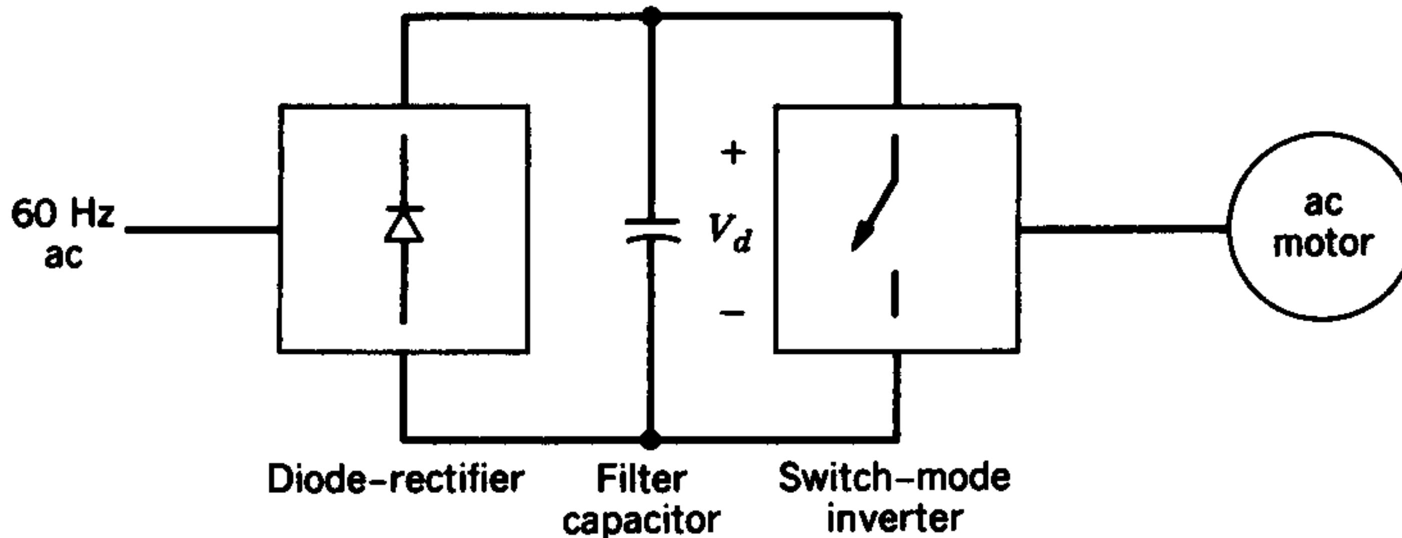

Figure 8-1 Switch-mode inverter in ac motor drive.

- Block diagram of a motor drive where the power flow is unidirectional

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Switch-Mode DC-AC Inverter

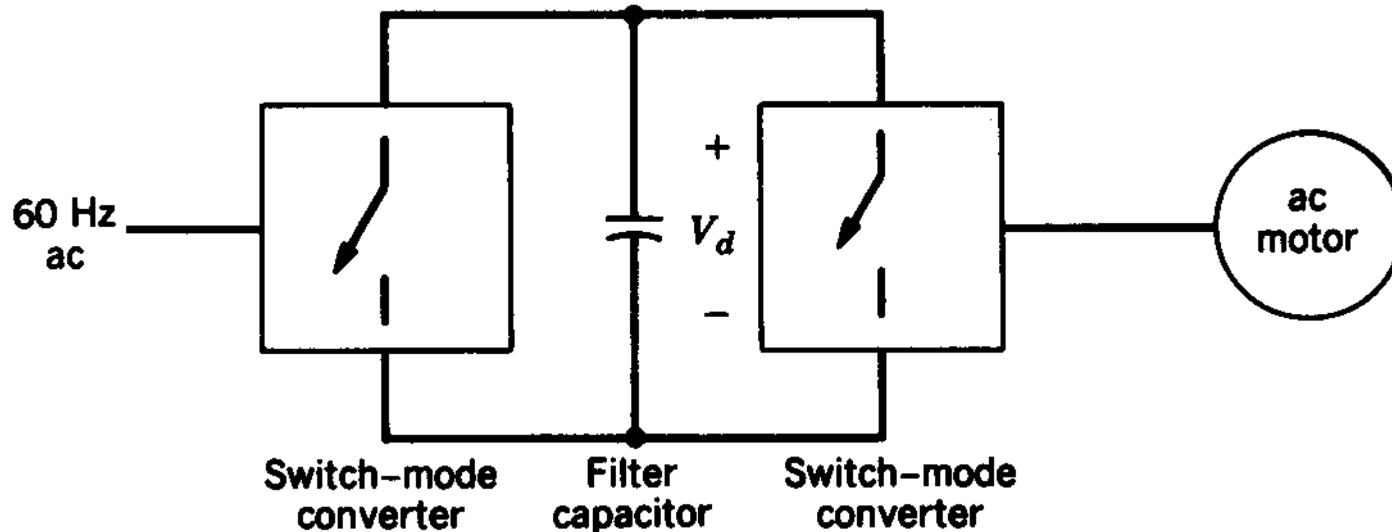

Figure 8-2 Switch-mode converters for motoring and regenerative braking in ac motor drive.

- Block diagram of a motor drive where the power flow can be bi-directional

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Switch-Mode DC-AC Inverter

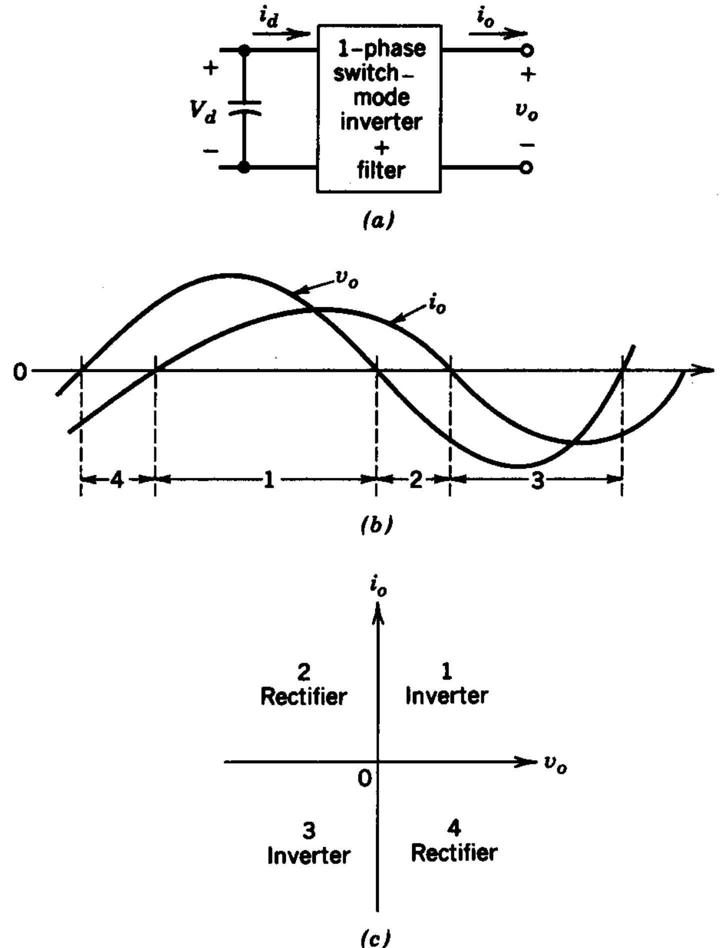

Figure 8-3 Single-phase switch-mode inverter.

- Four quadrants of operation

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One Leg of a Switch-Mode DC-AC Inverter

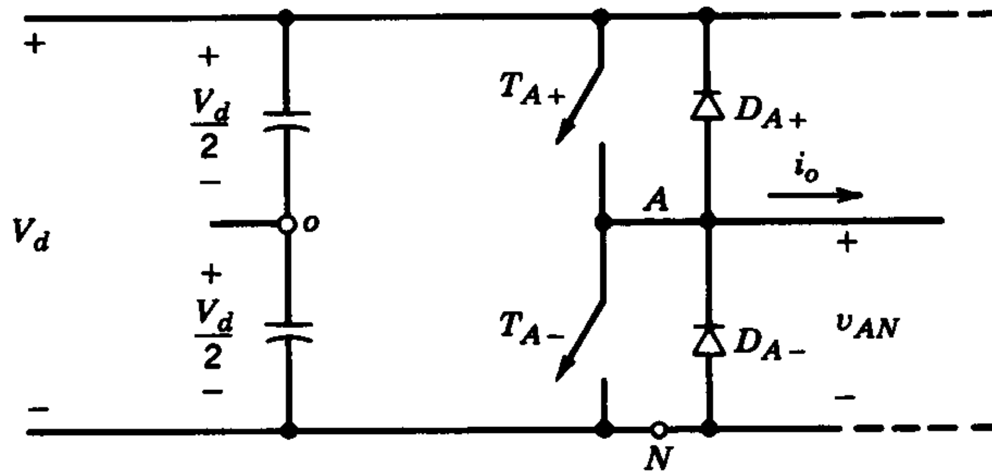

Figure 8-4 One-leg switch-mode inverter.

- The mid-point shown is fictitious

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Synthesis of a Sinusoidal Output by PWM

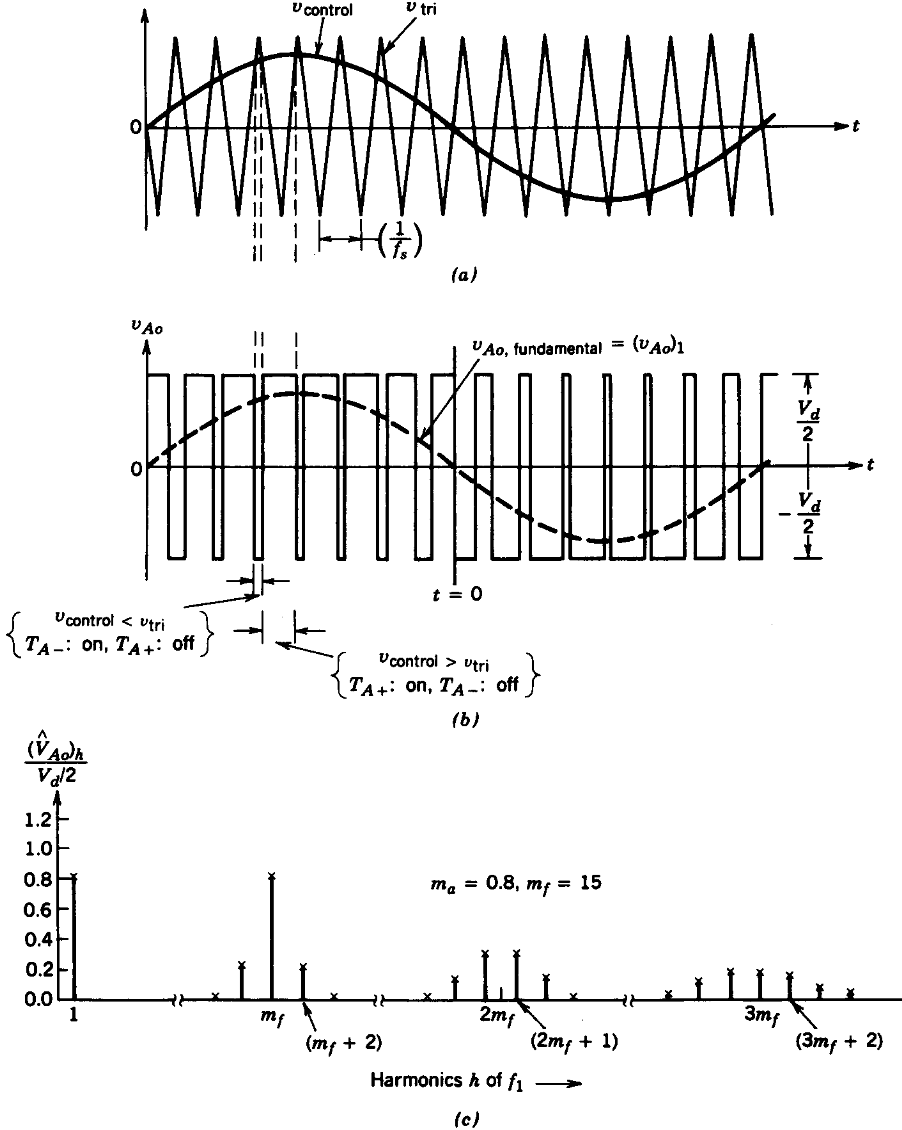

Figure 8-5 Pulse-width modulation.

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Details of a Switching Time Period

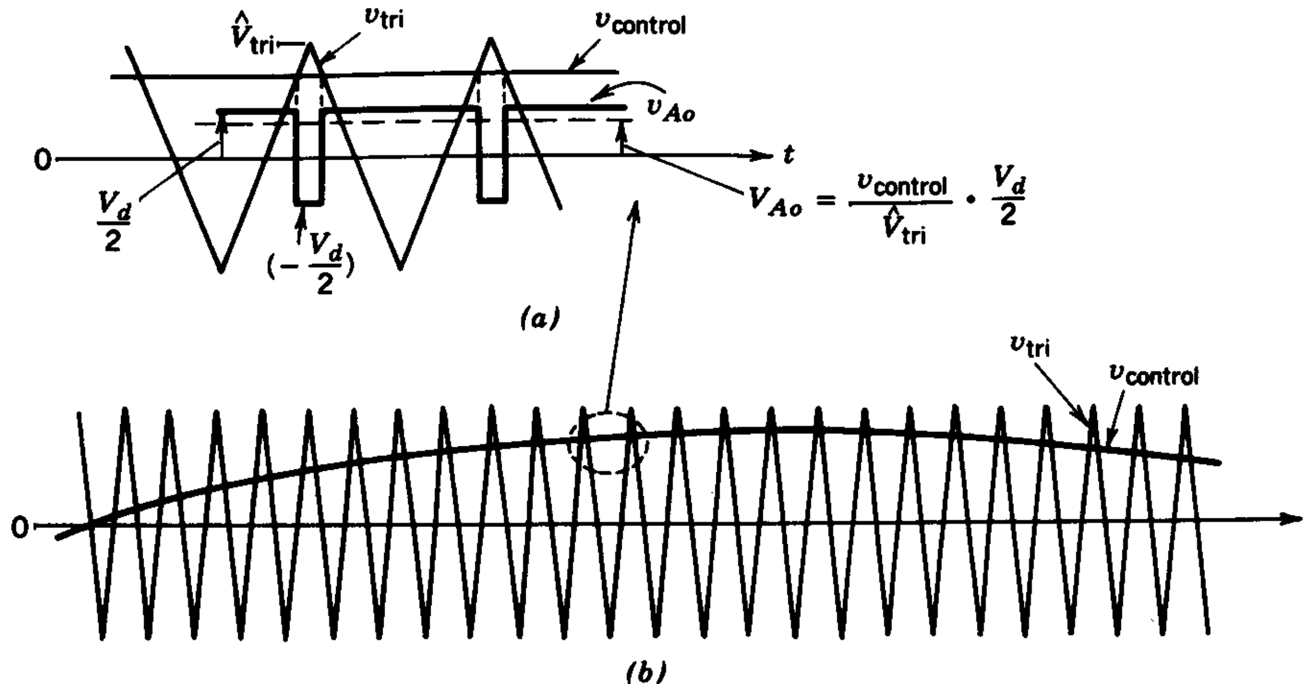

Figure 8-6 Sinusoidal PWM.

- Control voltage can be assumed constant during a switching time-period

Harmonics in the DC-AC Inverter Output Voltage

Table 8-1 Generalized Harmonics of v_{Ao} for a Large m_f.

h \ m_a	0.2	0.4	0.6	0.8	1.0
1 Fundamental	0.2	0.4	0.6	0.8	1.0
m_f	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.008	0.105	0.068
$4m_f \pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.050

Note: $(\hat{V}_{Ao})_h / \frac{1}{2}V_d$ [$= (\hat{V}_{AN})_h / \frac{1}{2}V_d$] is tabulated as a function of m_a.

- Harmonics appear around the carrier frequency and its multiples

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Harmonics due to Over-modulation

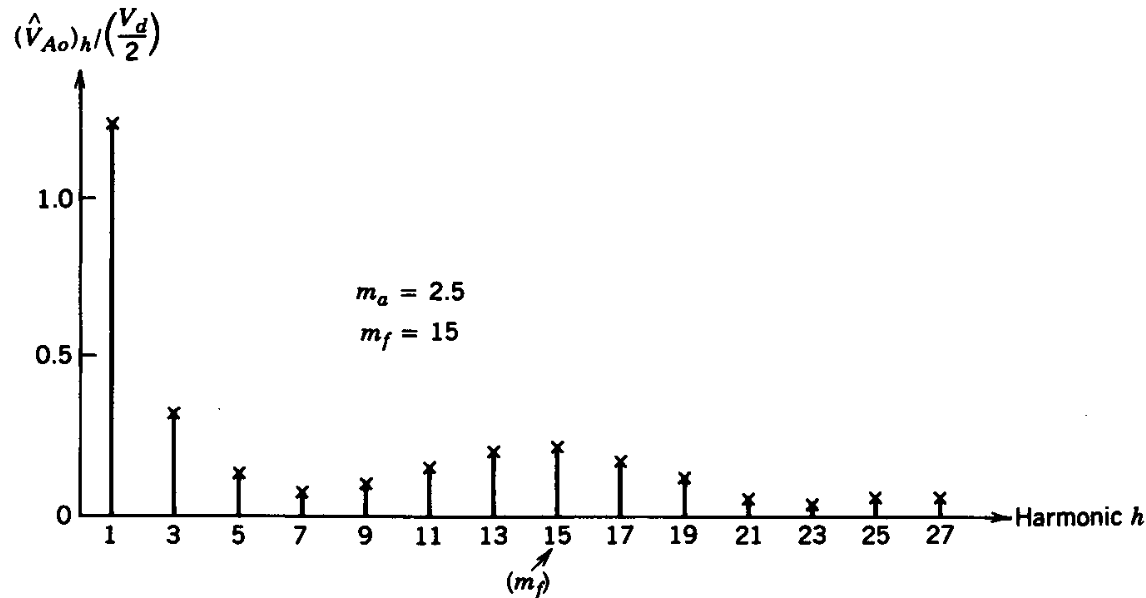

Figure 8-7 Harmonics due to overmodulation; drawn for $m_a = 2.5$ and $m_f = 15$.

- These are harmonics of the fundamental frequency

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Output voltage Fundamental as a Function of the Modulation Index

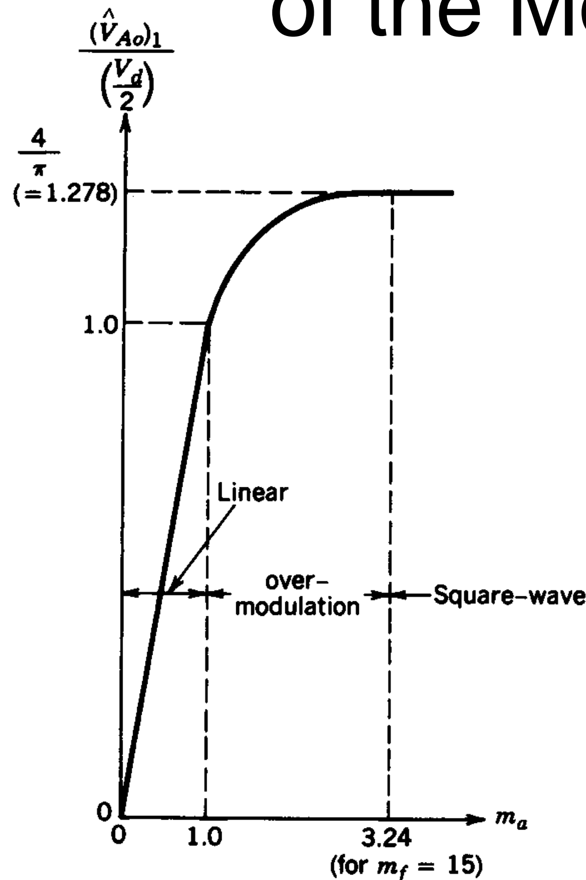

Figure 8-8 Voltage control by varying m_a.

- Shows the linear and the over-modulation regions; square-wave operation in the limit

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Square-Wave Mode of Operation

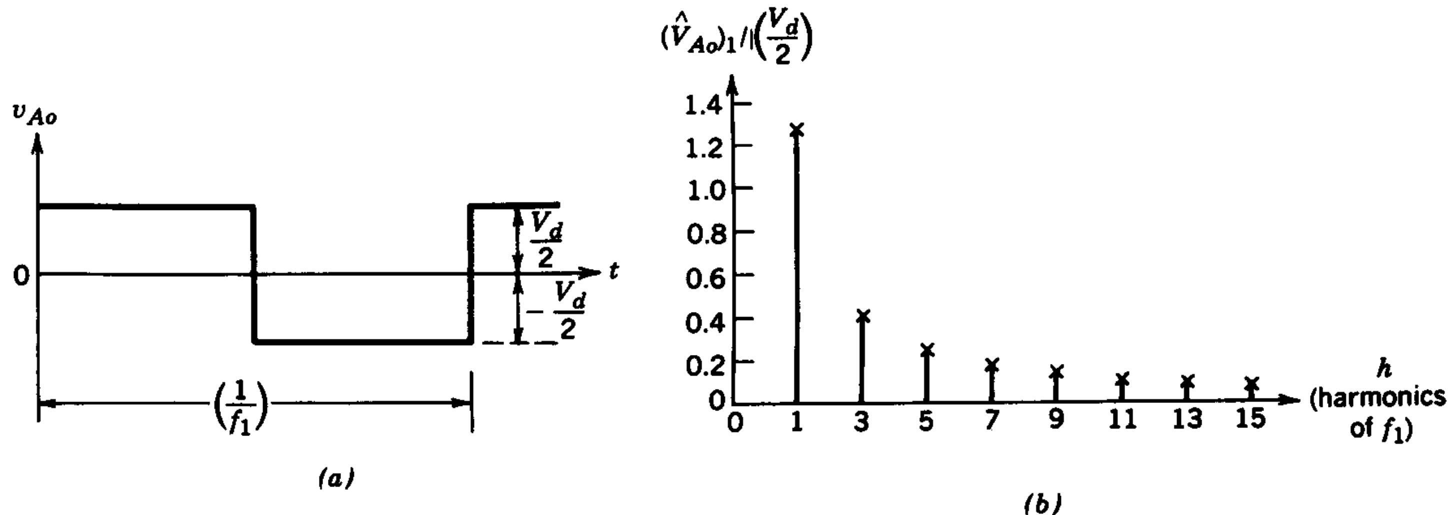

Figure 8-9 Square-wave switching.

- Harmonics are of the fundamental frequency

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Half-Bridge Inverter

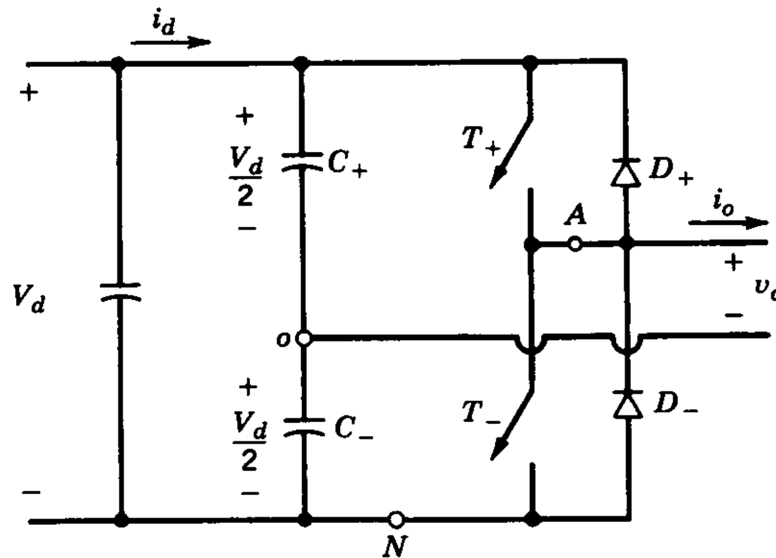

Figure 8-10 Half-bridge inverter.

- Capacitors provide the mid-point

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Single-Phase Full-Bridge DC-AC Inverter

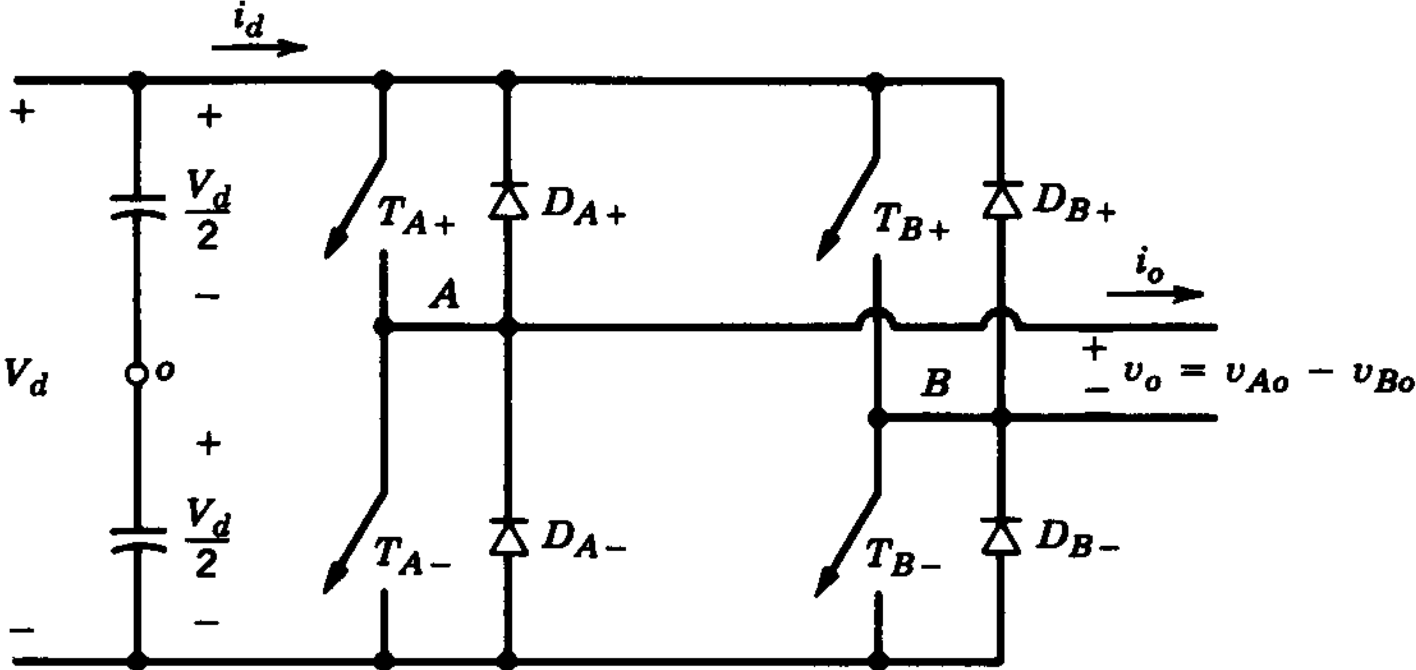

Figure 8-11 Single-phase full-bridge inverter.

- Consists of two inverter legs

PWM to Synthesize Sinusoidal Output

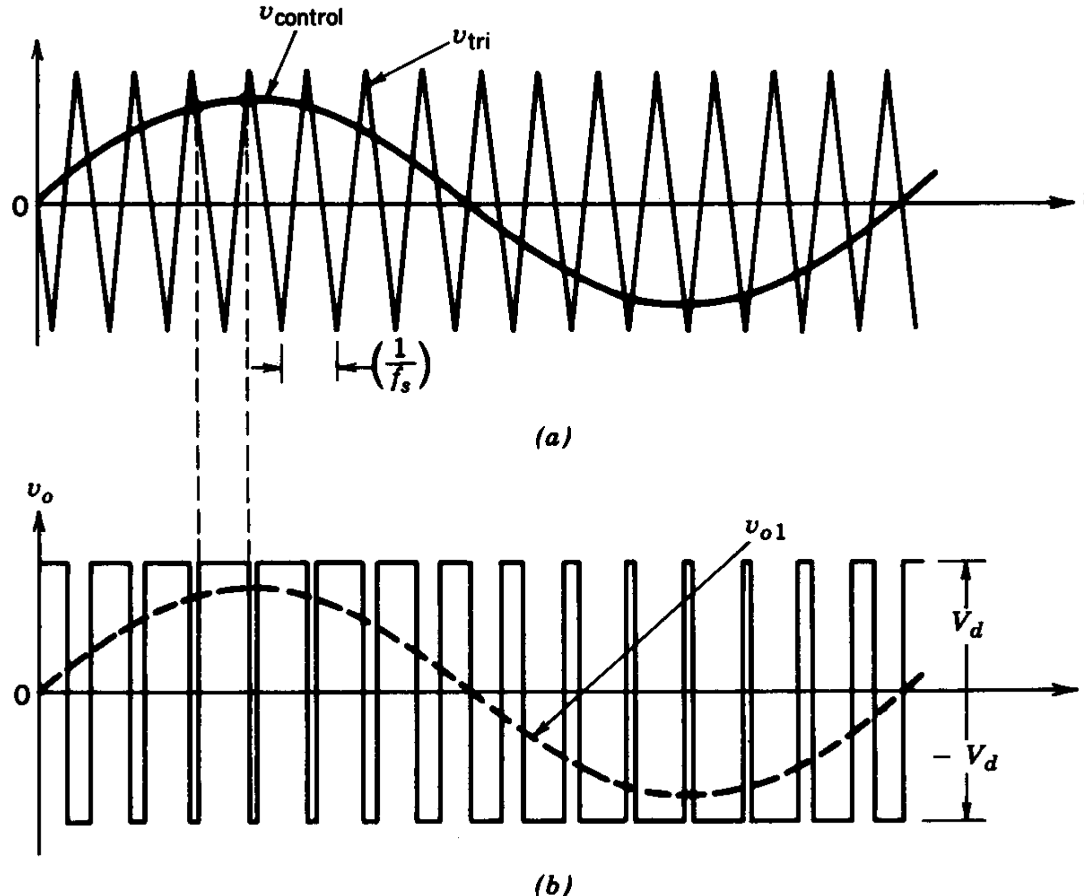

Figure 8-12 PWM with bipolar voltage switching.

- The dotted curve is the desired output; also the fundamental frequency

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Analysis assuming Fictitious Filters

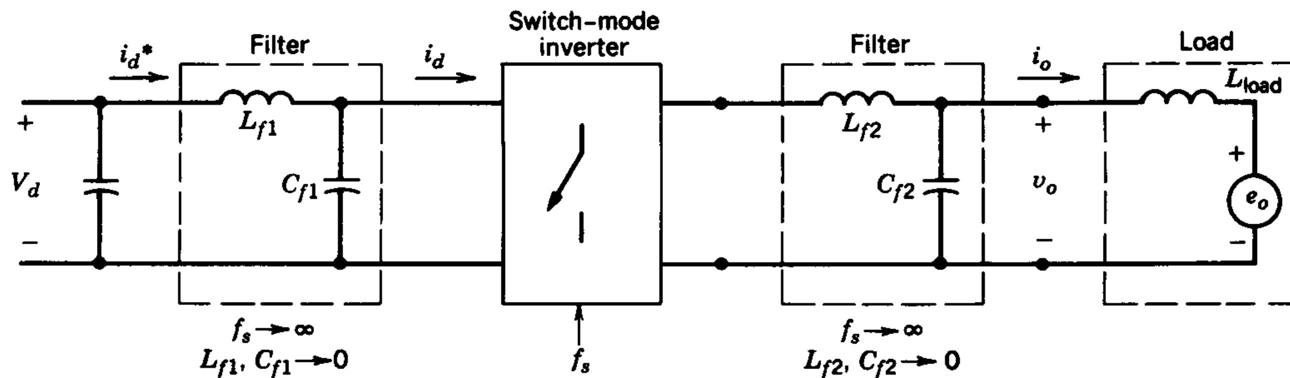

Figure 8-13 Inverter with "fictitious" filters.

- Small fictitious filters eliminate the switching-frequency related ripple

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DC-Side Current

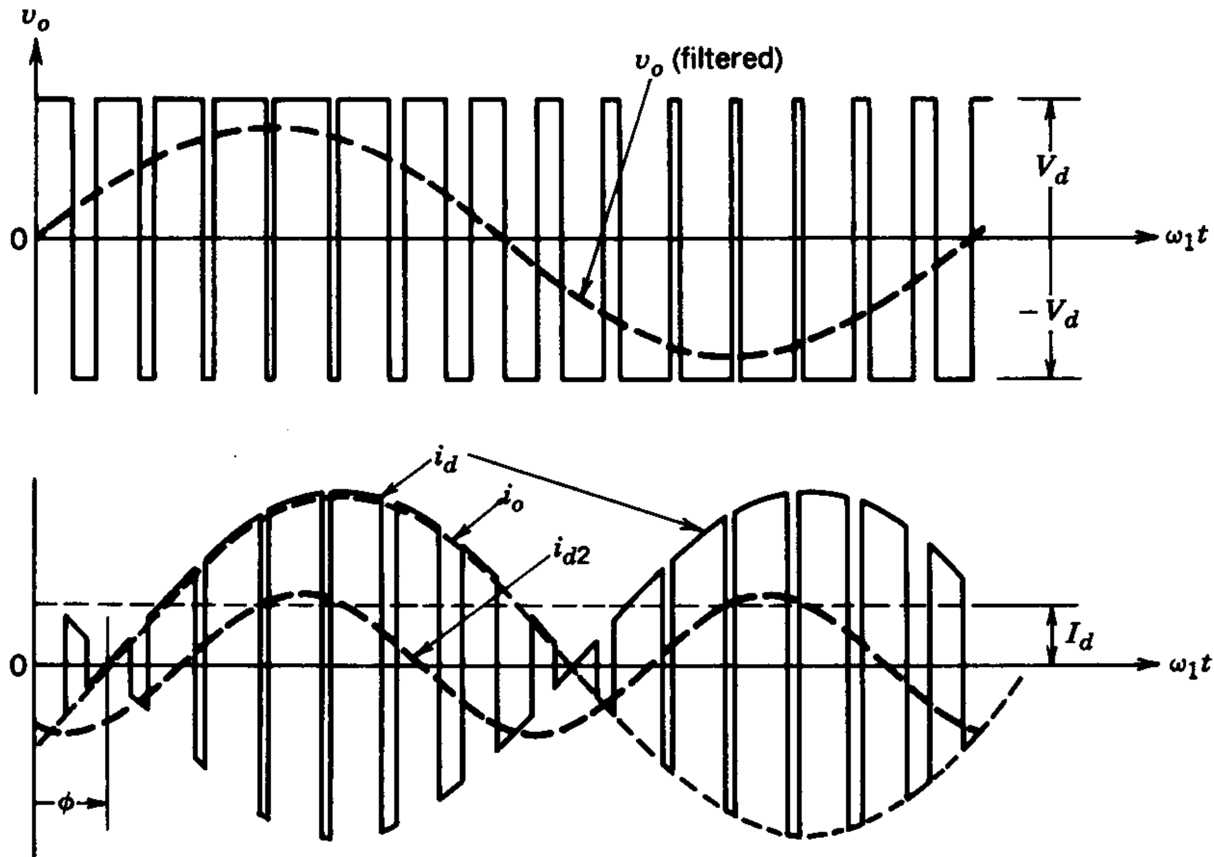

Figure 8-14 The dc-side current in a single-phase inverter with PWM bipolar voltage switching.

- Bi-Polar Voltage switching

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Output Waveforms: Uni-polar Voltage Switching

- Harmonic components around the switching frequency are absent

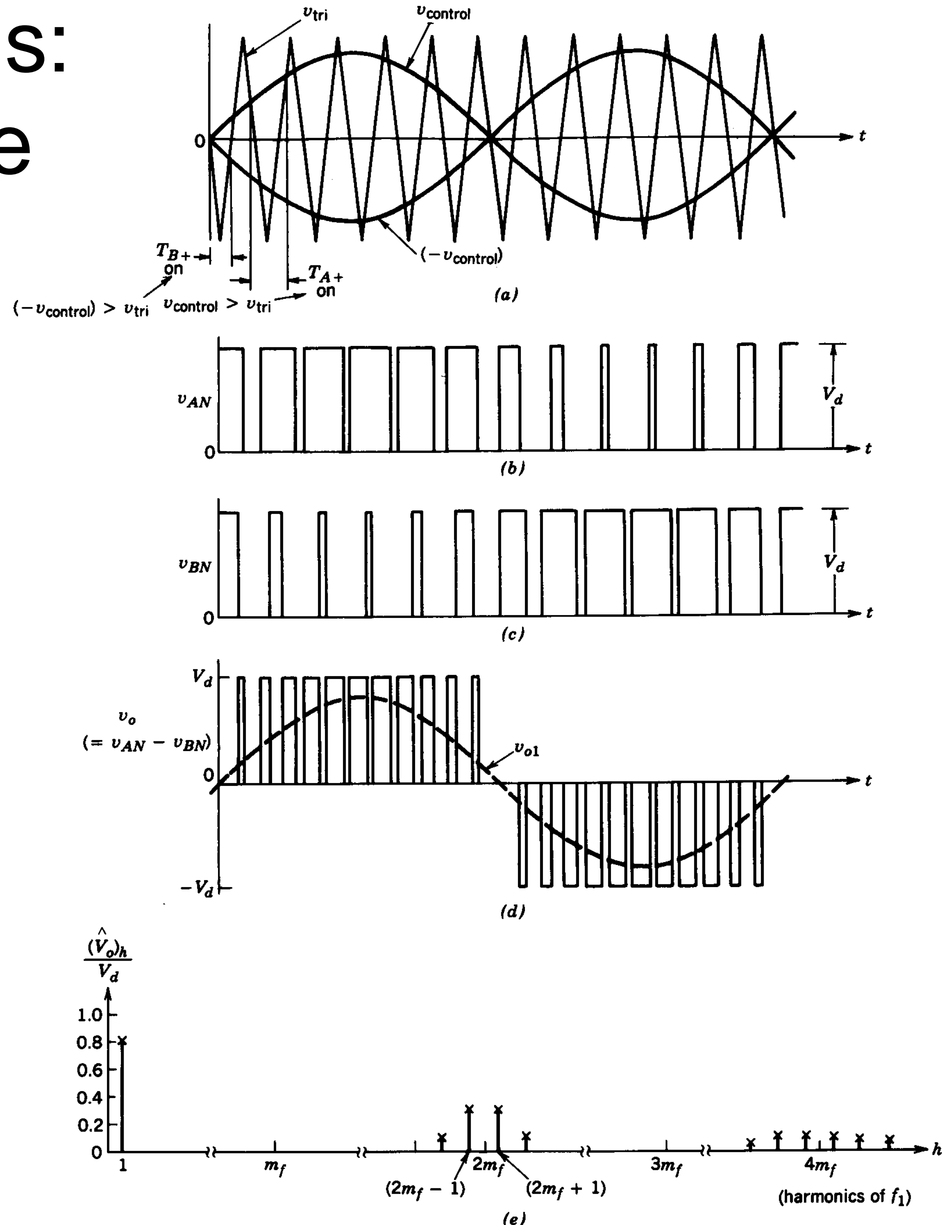

Figure 8-15 PWM with unipolar voltage switching (single phase).

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DC-Side Current in a Single-Phase Inverter

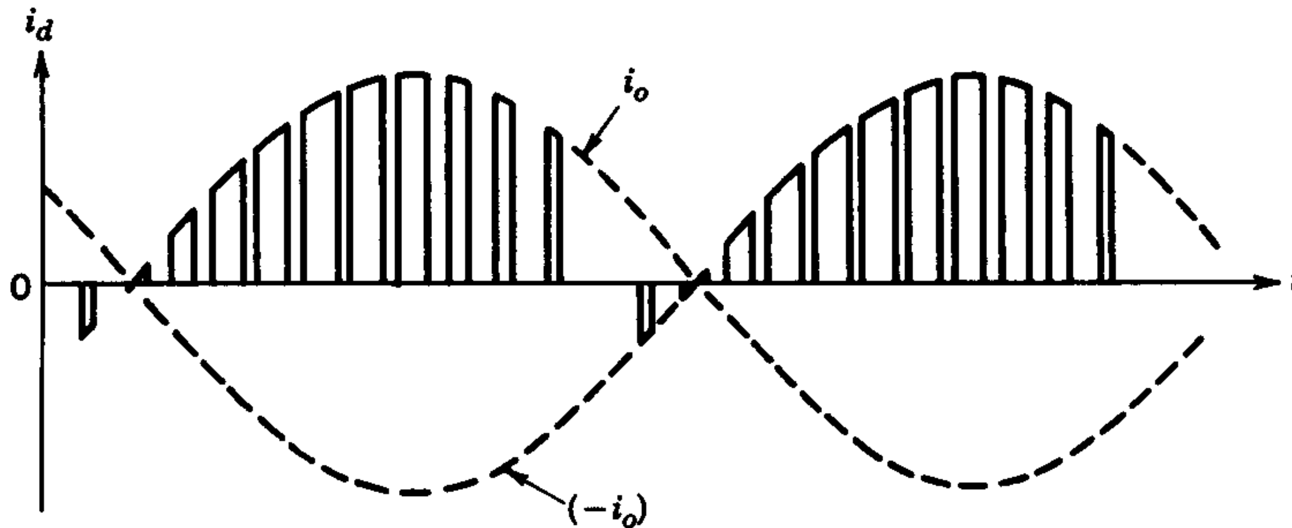

Figure 8-16 The dc-side current in a single-phase inverter with PWM unipolar voltage switching.

- Uni-polar voltage switching

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Sinusoidal Synthesis by Voltage Shift

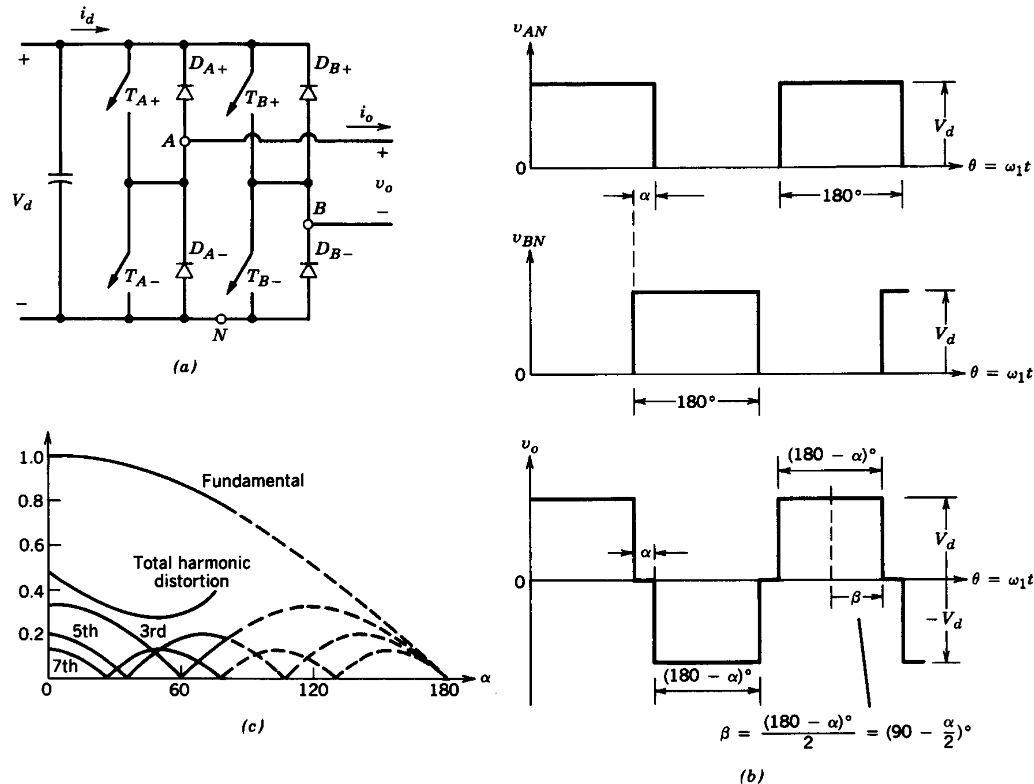

Figure 8-17 Full-bridge, single-phase inverter control by voltage cancellation: (*a*) power circuit; (*b*) waveforms; (*c*) normalized fundamental and harmonic voltage output and total harmonic distortion as a function of α.

- Phase shift allows voltage cancellation to synthesize a 1-Phase sinusoidal output

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Single-Phase Inverter

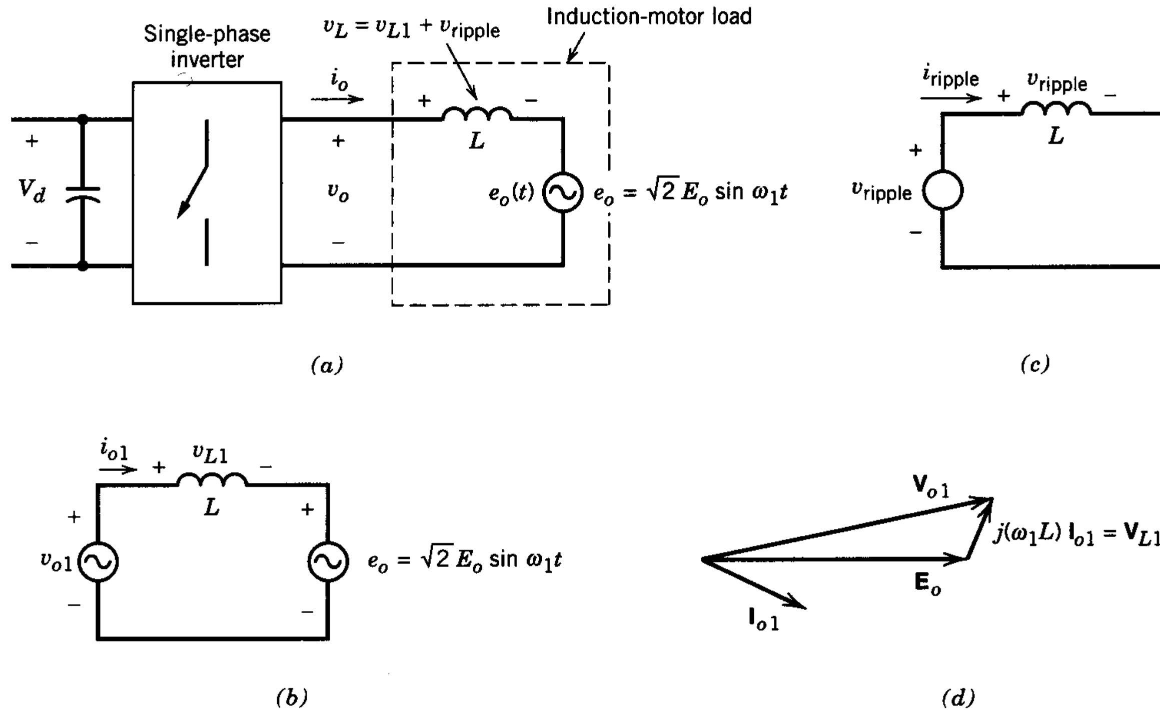

Figure 8-18 Single-phase inverter: (*a*) circuit; (*b*) fundamental-frequency components; (*c*) ripple frequency components; (*d*) fundamental-frequency phasor diagram.

- Analysis at the fundamental frequency

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Square-Wave and PWM Operation

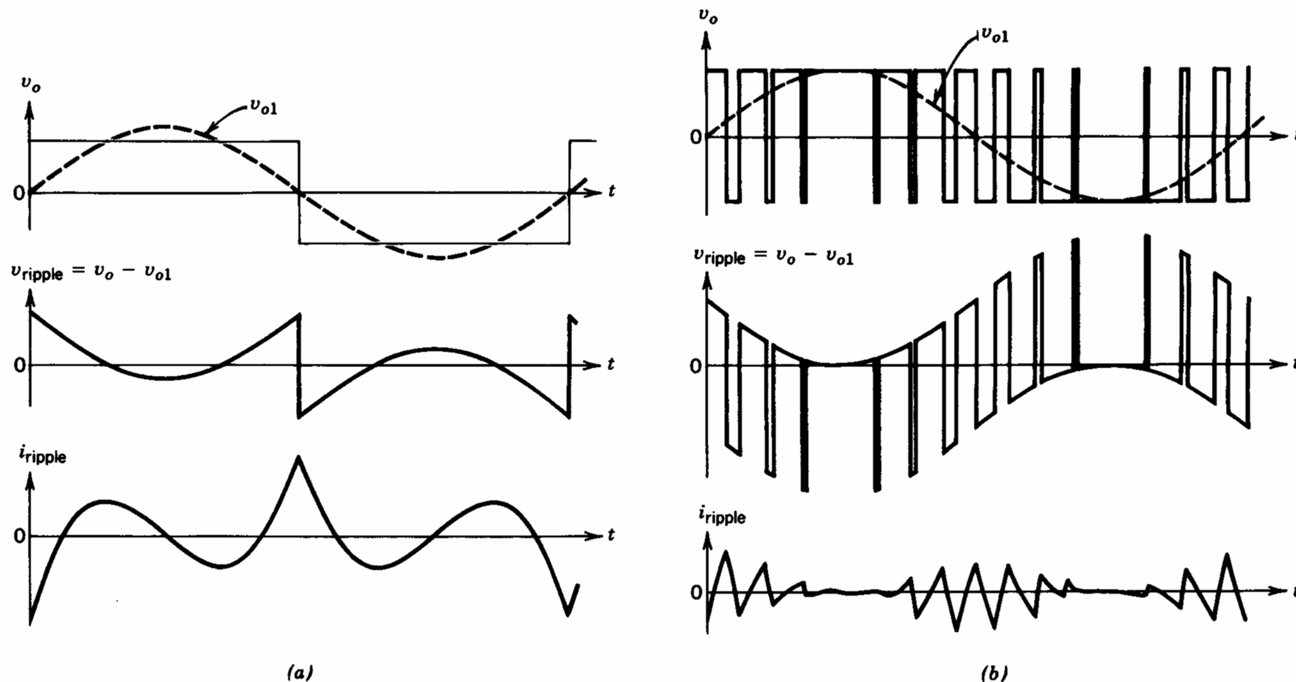

Figure 8-19 Ripple in the inverter output: (*a*) square-wave switching; (*b*) PWM bipolar voltage switching.

- PWM results in much smaller ripple current

Push-Pull Inverter

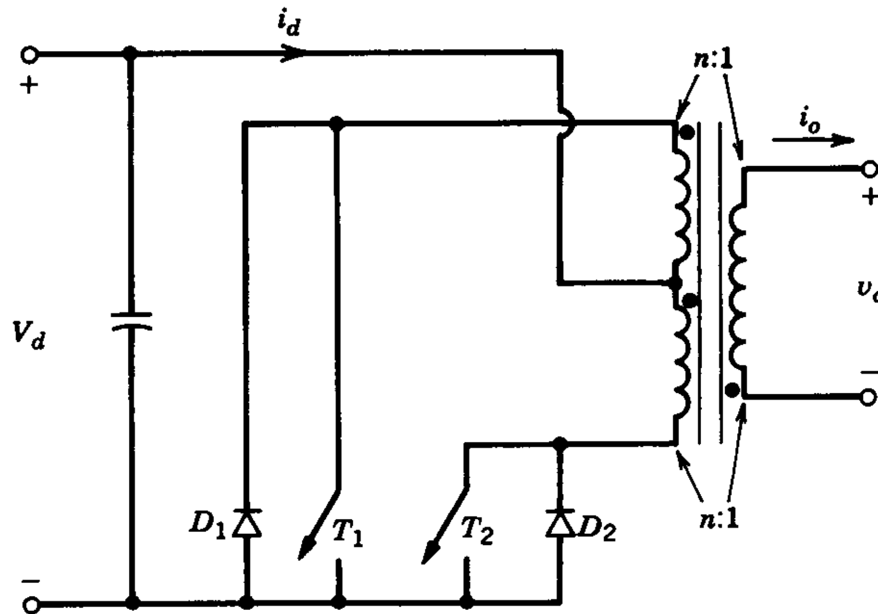

Figure 8-20 Push–pull inverter (single phase).

- Low Voltage to higher output using square-wave operation

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Three-Phase Inverter

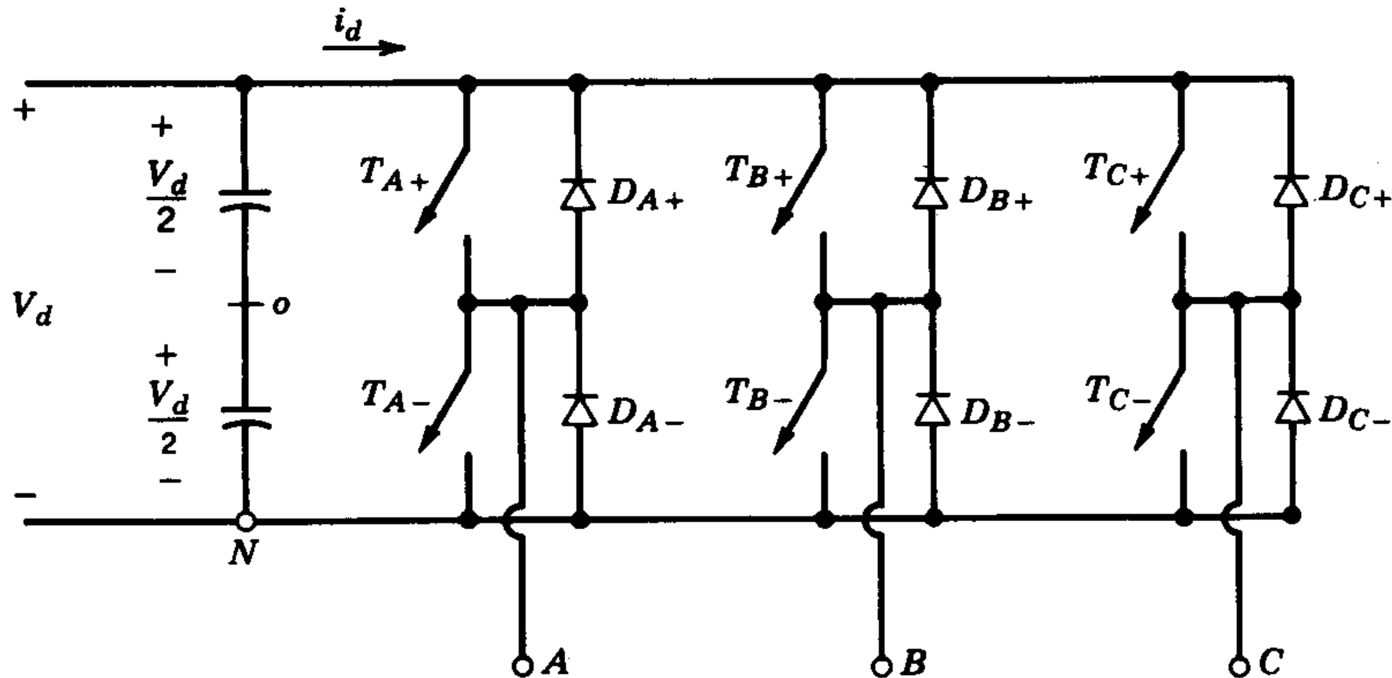

Figure 8-21 Three-phase inverter.

- Three inverter legs; capacitor mid-point is fictitious

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Three-Phase PWM Waveforms

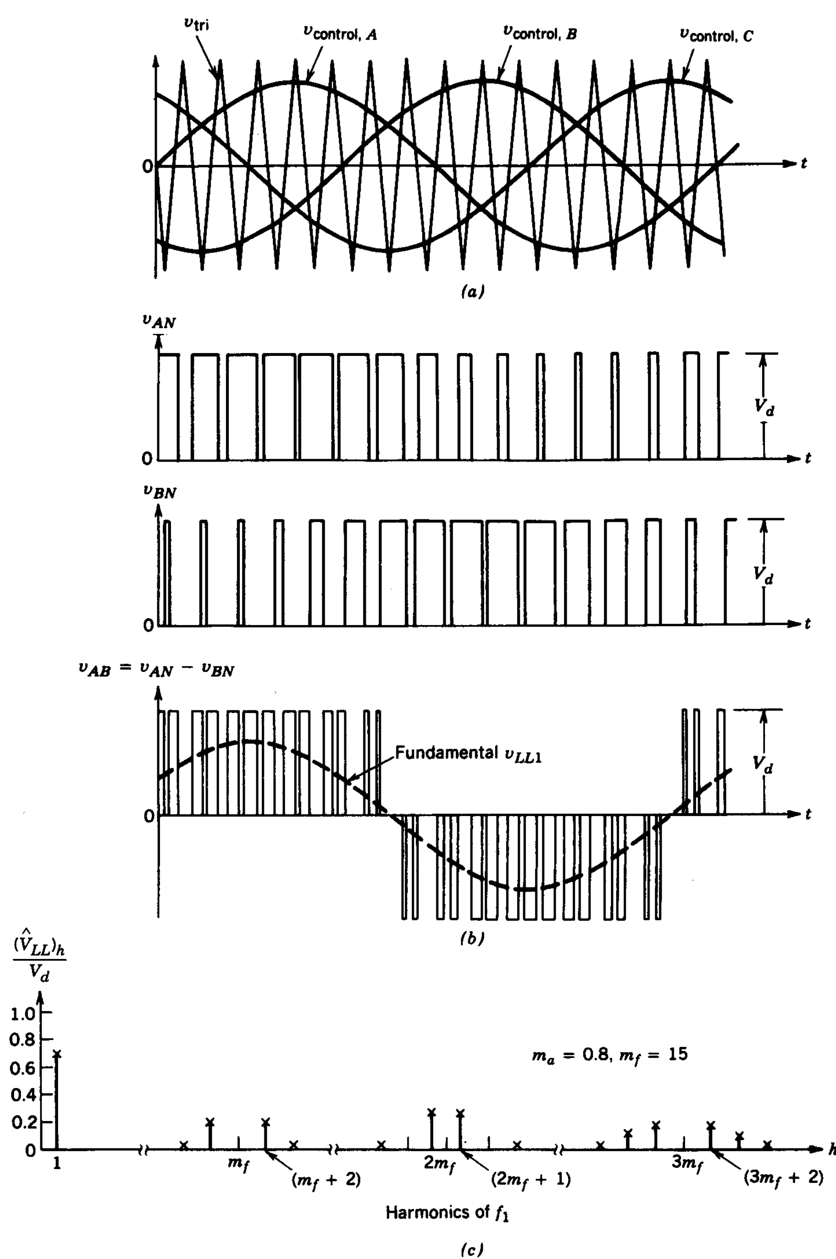

Figure 8-22 Three-phase PWM waveforms and harmonic spectrum.

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Three-Phase Inverter Harmonics

Table 8-2 Generalized Harmonics of v_{LL} for a Large and Odd m_f That Is a Multiple of 3.

h \ m_a	*0.2*	*0.4*	*0.6*	*0.8*	*1.0*
1	*0.122*	*0.245*	*0.367*	*0.490*	*0.612*
$m_f \pm 2$	0.010	0.037	0.080	0.135	0.195
$m_f \pm 4$				0.005	0.011
$2m_f \pm 1$	0.116	0.200	0.227	0.192	0.111
$2m_f \pm 5$				0.008	0.020
$3m_f \pm 2$	0.027	0.085	0.124	0.108	0.038
$3m_f \pm 4$		0.007	0.029	0.064	0.096
$4m_f \pm 1$	0.100	0.096	0.005	0.064	0.042
$4m_f \pm 5$			0.021	0.051	0.073
$4m_f \pm 7$				0.010	0.030

Note: $(V_{LL})_h/V_d$ are tabulated as a function of m_a where $(V_{LL})_h$ are the rms values of the harmonic voltages.

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Three-Phase Inverter Output

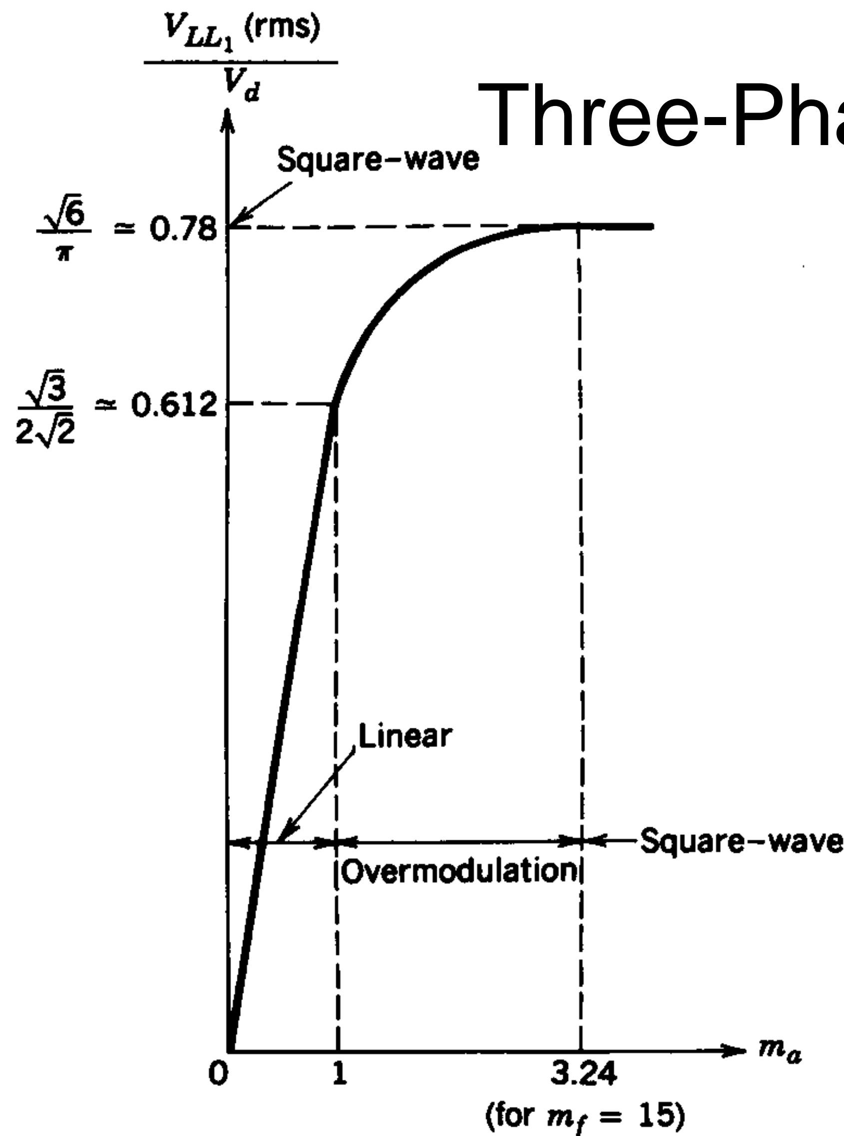

Figure 8-23 Three-phase inverter; V_{LL_1}(rms)/V_d as a function of m_a.

- Linear and over-modulation ranges

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Three-Phase Inverter: Square-Wave Mode

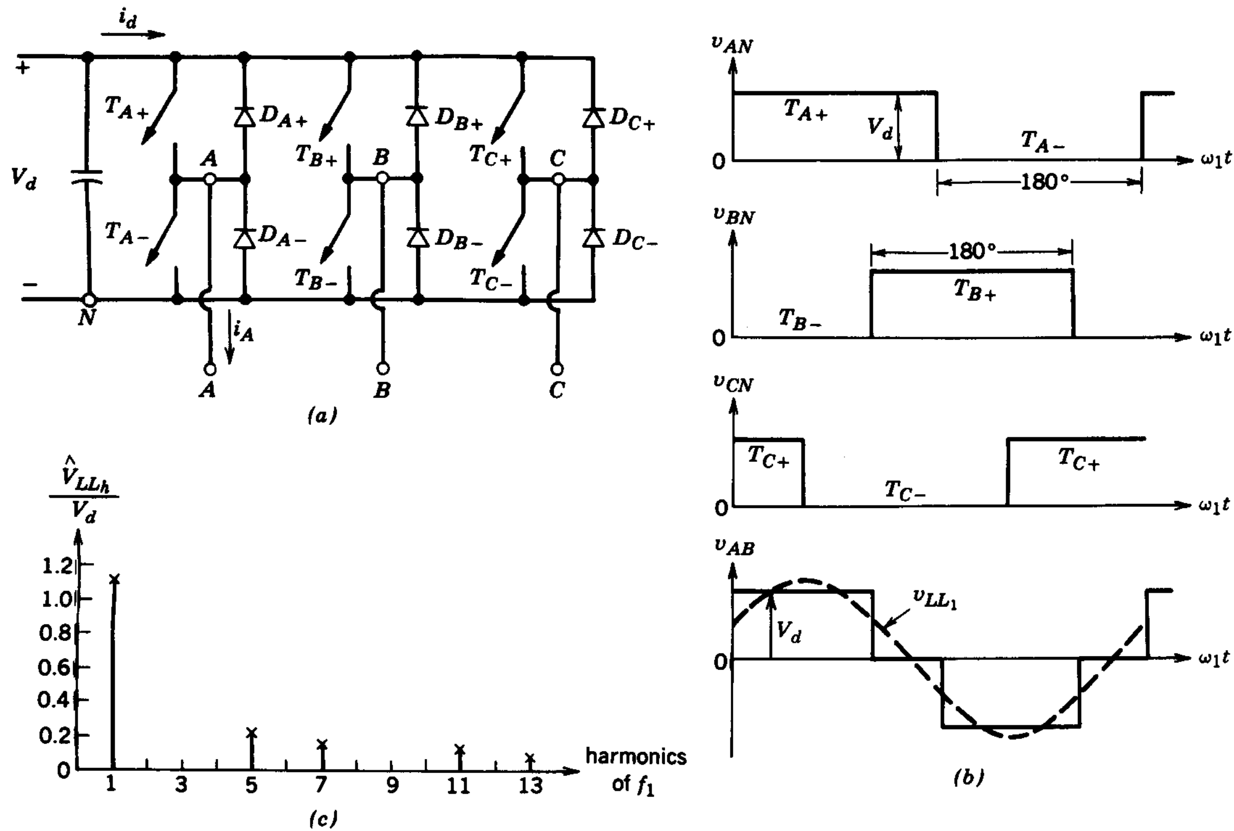

Figure 8-24 Square-wave inverter (three phase).

- Harmonics are of the fundamental frequency

Three-Phase Inverter: Fundamental Frequency

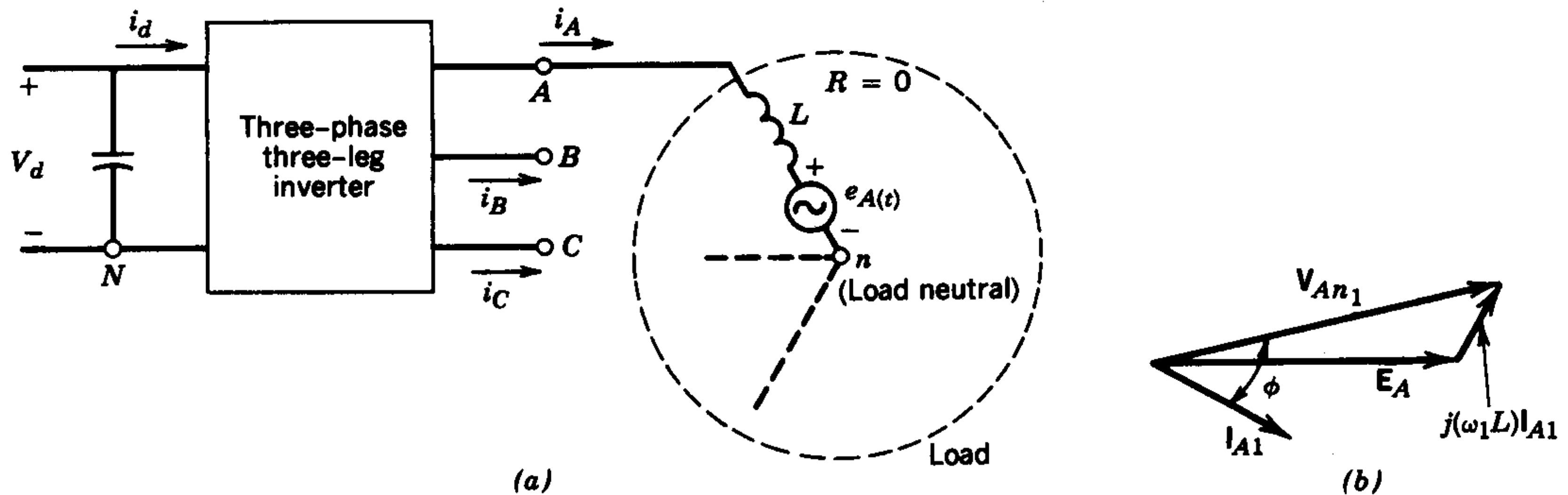

Figure 8-25 Three-phase inverter: (*a*) circuit diagram; (*b*) phasor diagram (fundamental frequency).

- Analysis at the fundamental frequency can be done using phasors

Square-Wave and PWM Operation

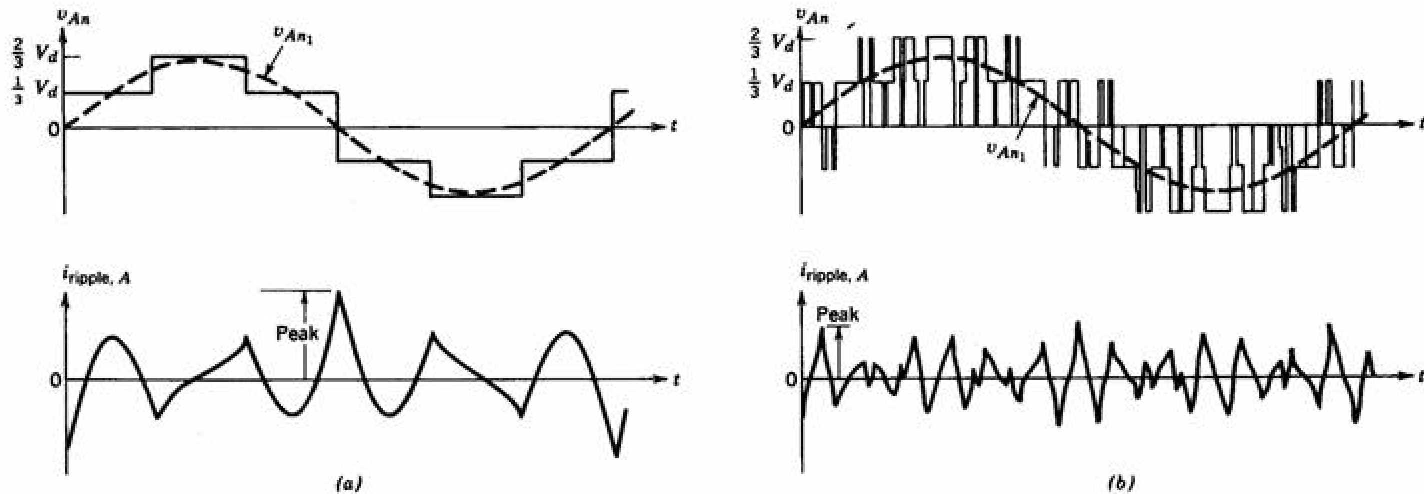

Figure 8-26 Phase-to-load-neutral variables of a three-phase inverter: (*a*) square wave; (*b*) PWM.

- PWM results in much smaller ripple current

DC-Side Current in a Three-Phase Inverter

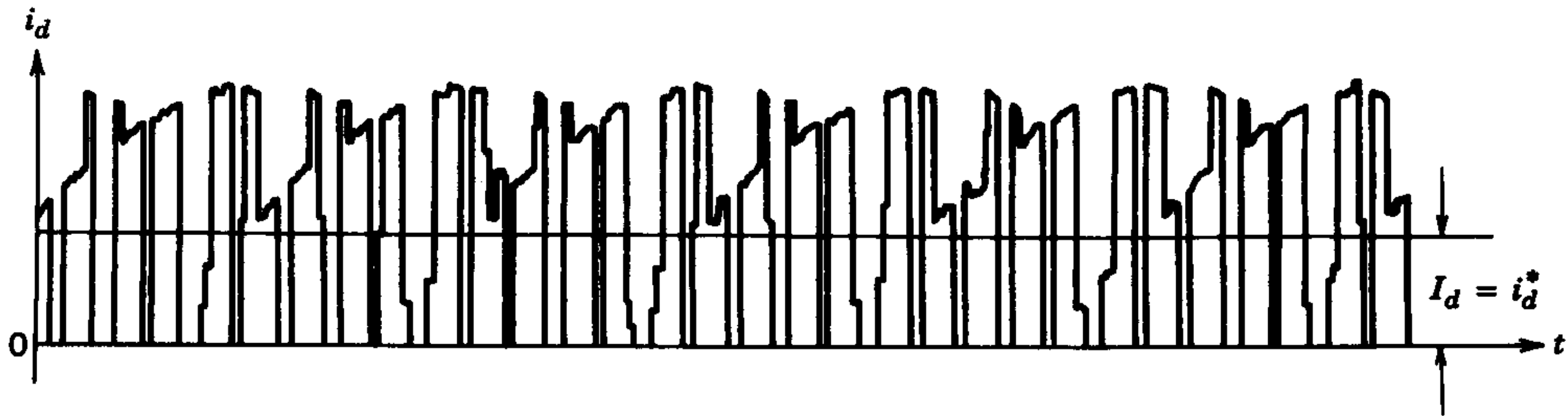

Figure 8-27 Input dc current in a three-phase inverter.

- The current consists of a dc component and the switching-frequency related harmonics

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Square-Wave Operation

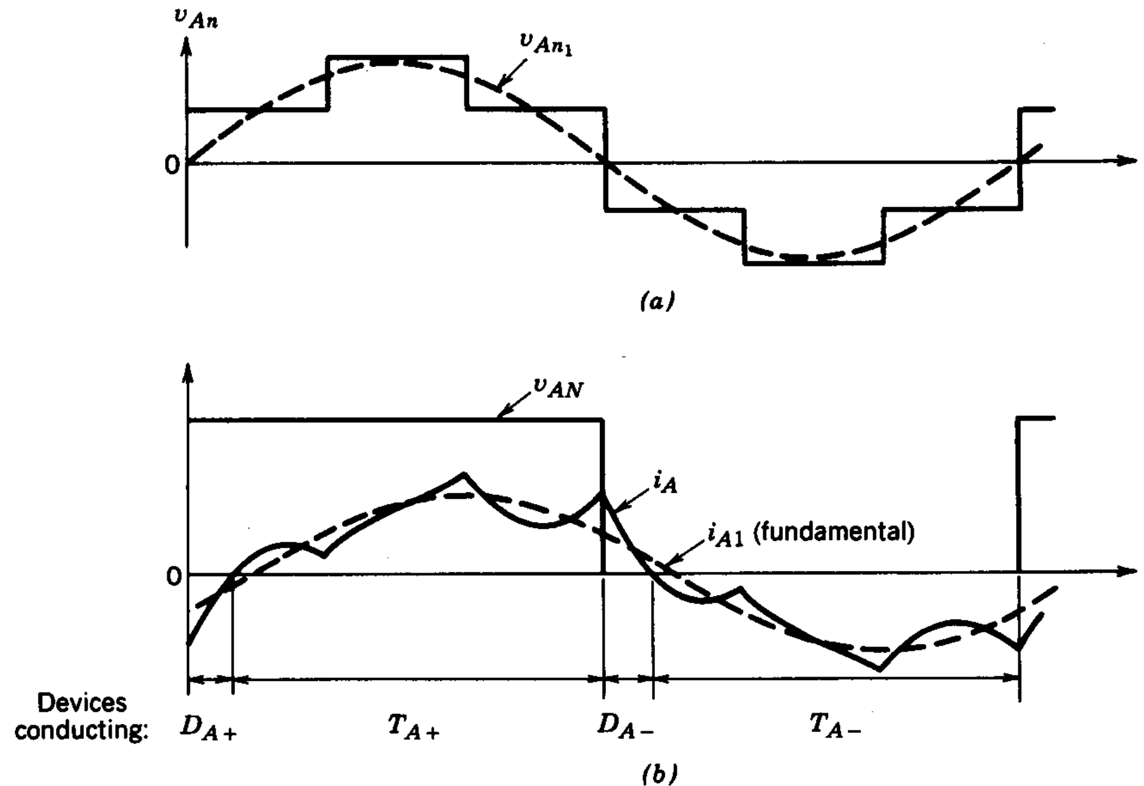

Figure 8-28 Square-wave inverter: phase A waveforms.

- devices conducting are indicated

PWM Operation

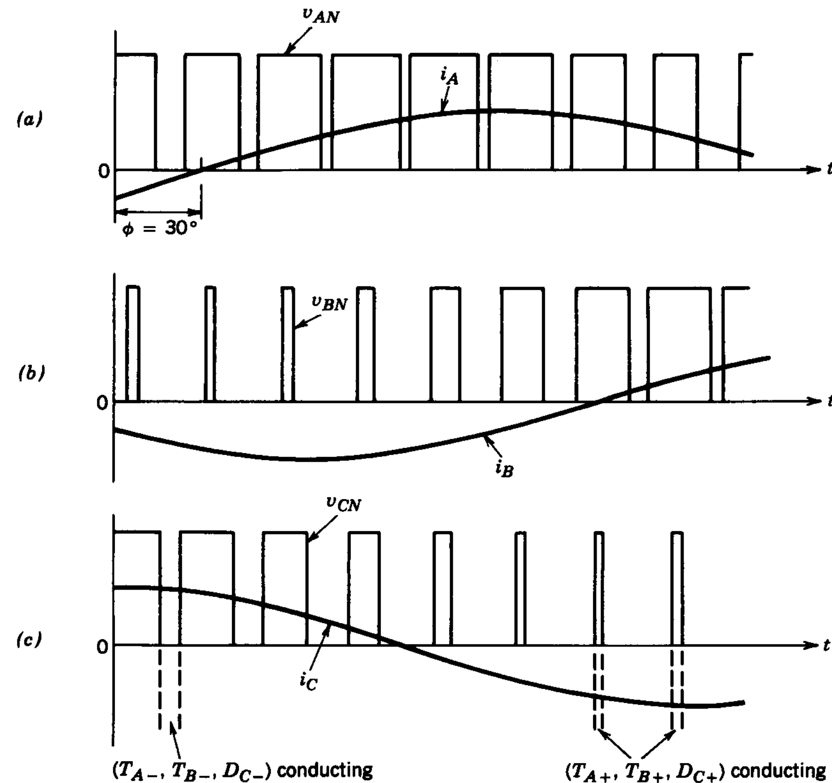

Figure 8-29 PWM inverter waveforms: load power factor angle = 30° (lag).

- devices conducting are indicated

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Short-Circuit States in PWM Operation

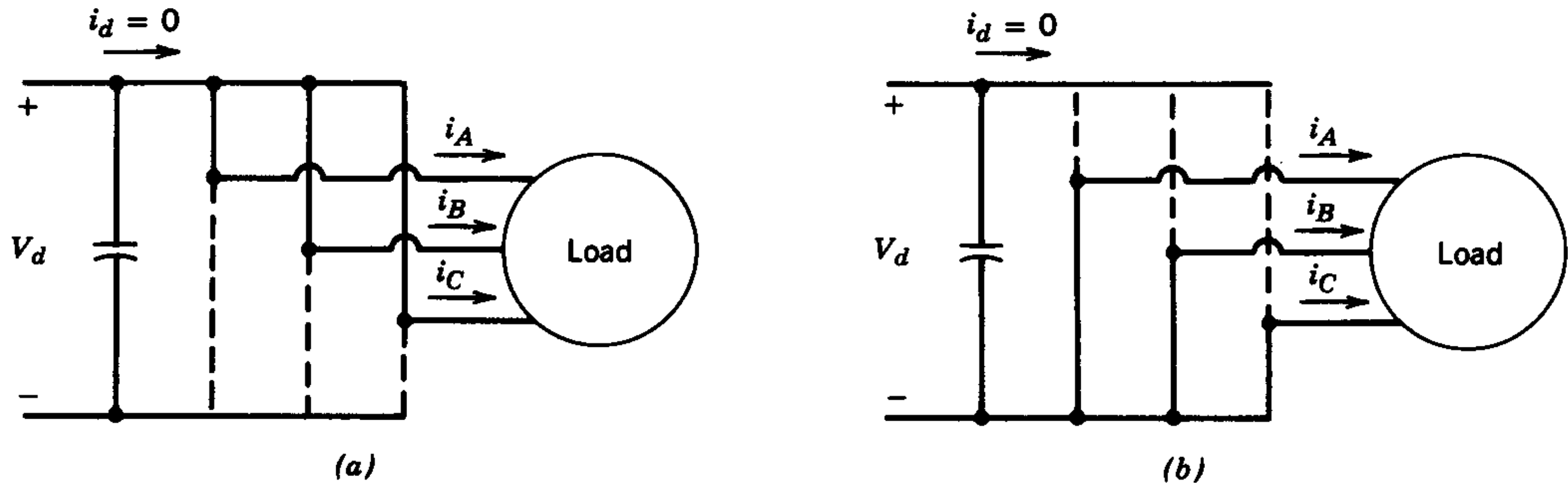
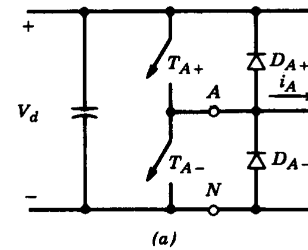


Figure 8-30 Short-circuit states in a three-phase PWM inverter.

- top group or the bottom group results in short circuiting three terminals

Effect of Blanking Time



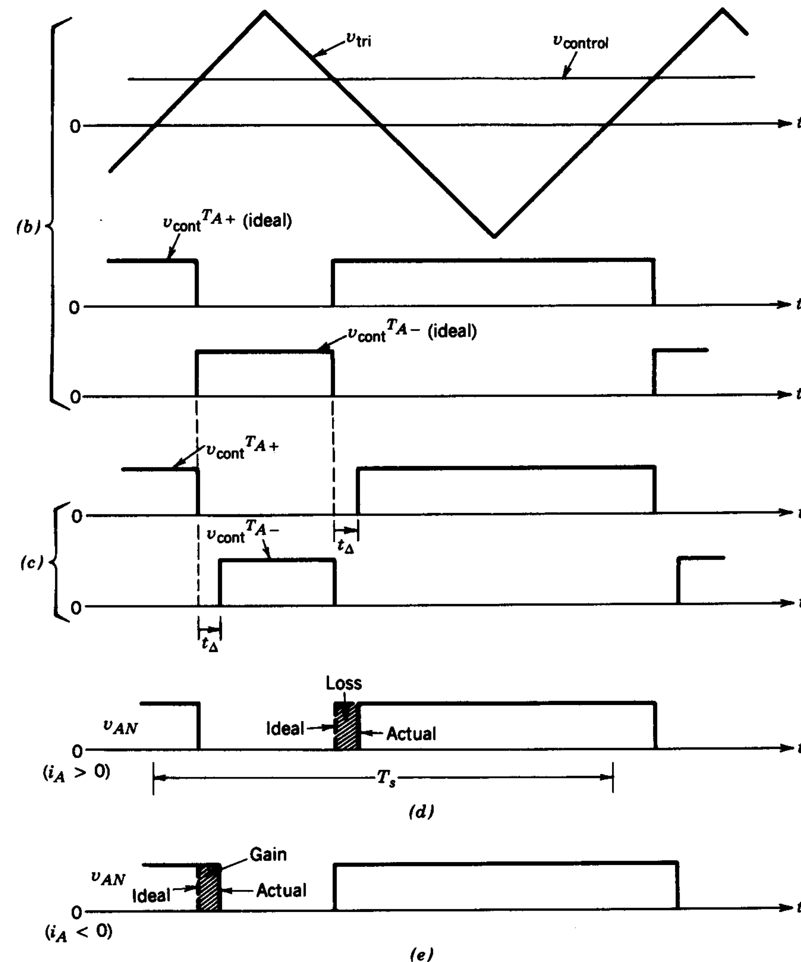


Figure 8-31 Effect of blanking time t_Δ.

- Results in nonlinearity

Effect of Blanking Time

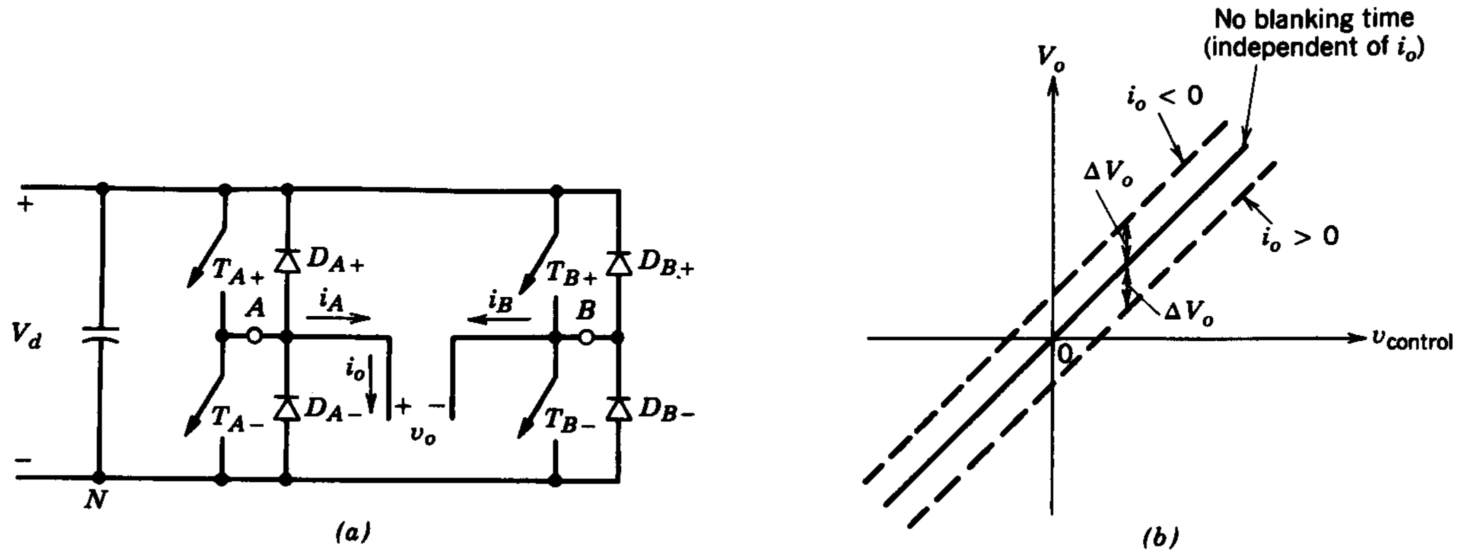


Figure 8-32 Effect of t_Δ on V_o, where ΔV_o is defined as a voltage drop if positive.

- Voltage jump when the current reverses direction

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Effect of Blanking Time

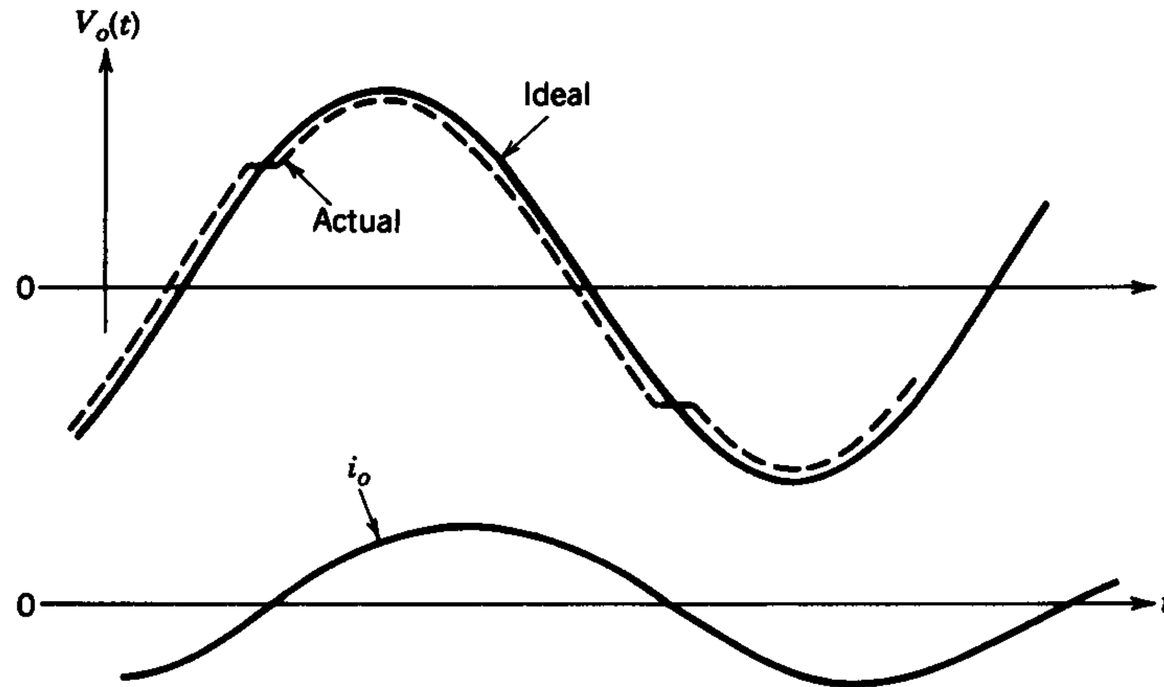

Figure 8-33 Effect of t_Δ on the sinusoidal output.

- Effect on the output voltage

Programmed Harmonic Elimination

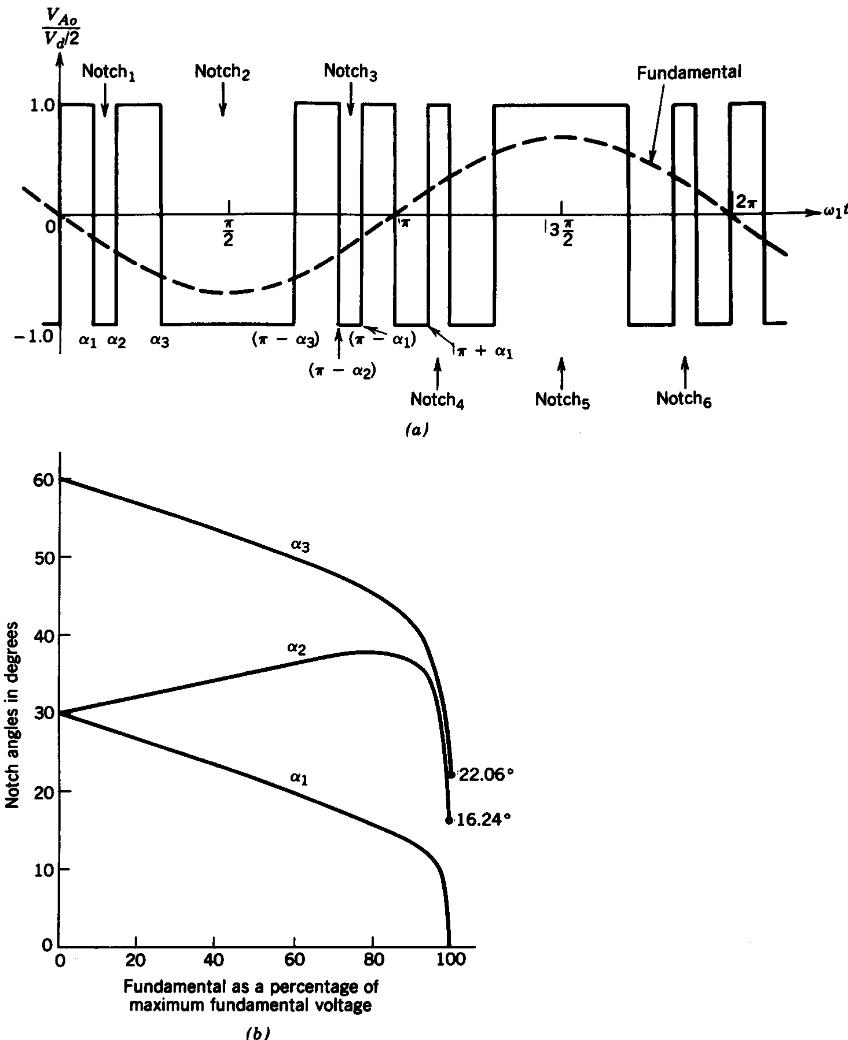

Figure 8-34 Programmed harmonic elimination of fifth and seventh harmonics.

- Angles based on the desired output

Tolerance-Band Current Control

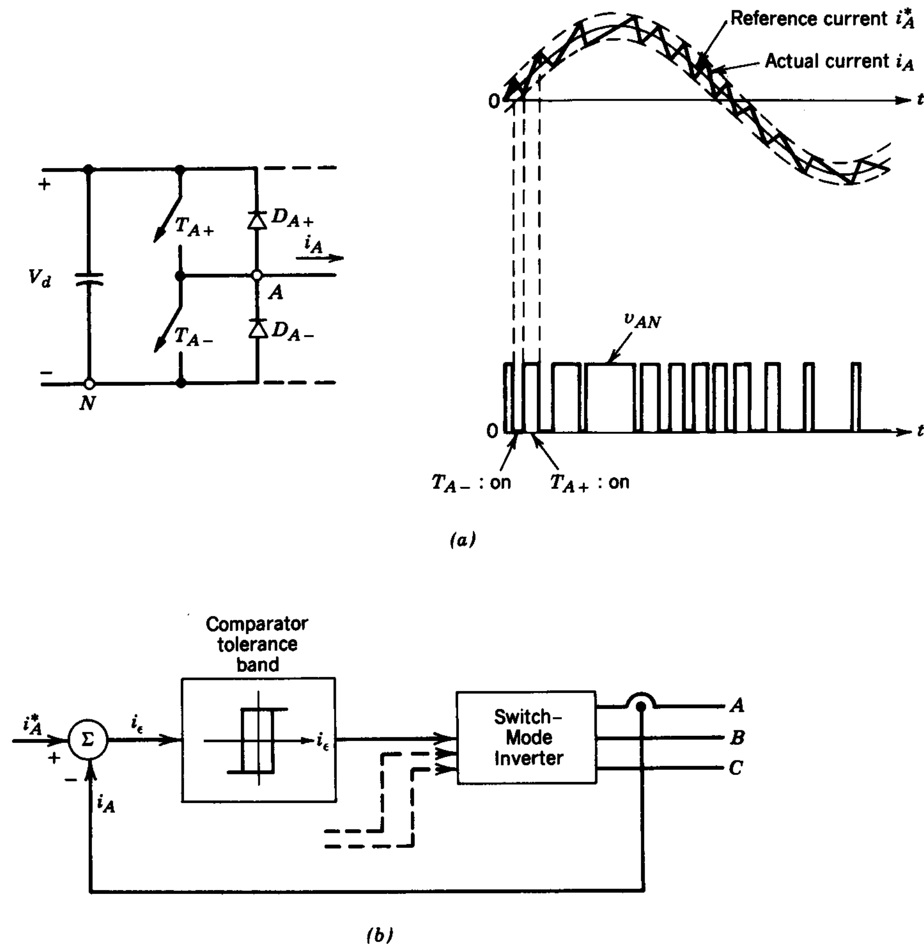

Figure 8-35 Tolerance band current control.

- Results in a variable frequency operation

Fixed-Frequency Operation

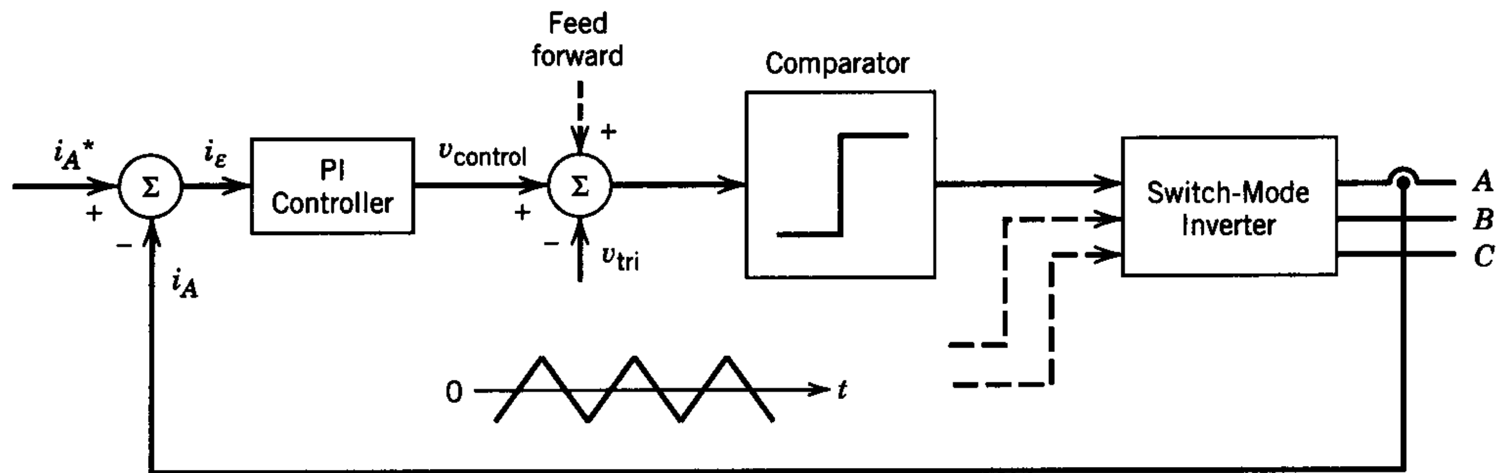

Figure 8-36 Fixed-frequency current control.

- Better control is possible using *dq* analysis

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Transition from Inverter to Rectifier Mode

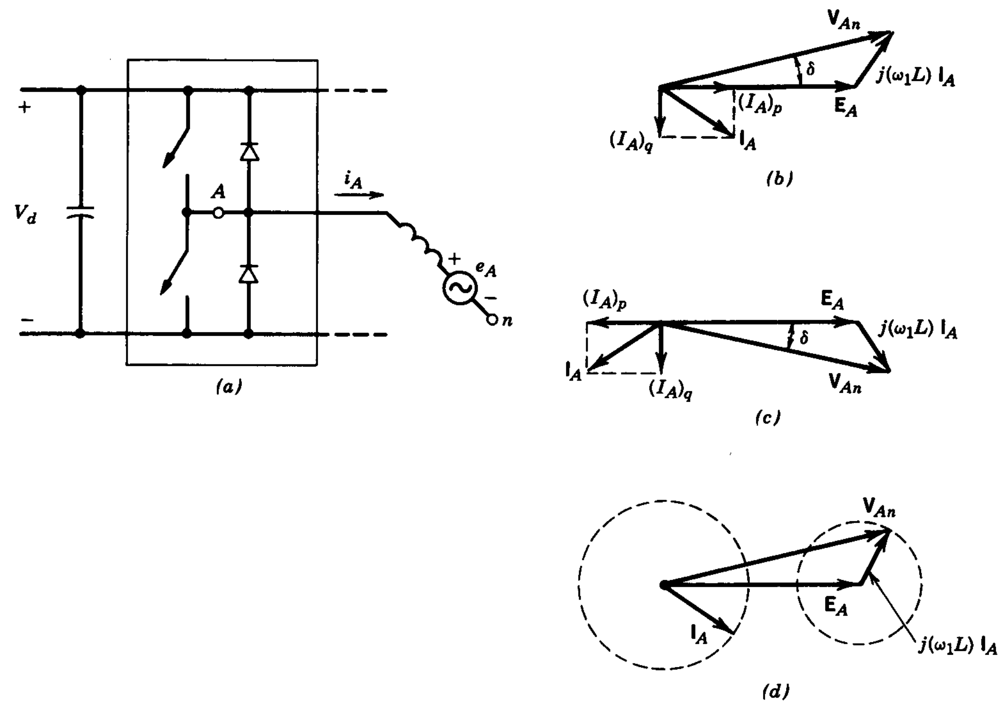

Figure 8-37 Operation modes: (*a*) circuit; (*b*) inverter mode; (*c*) rectifier mode; (*d*) constant I_A.

- Can analyze based on the fundamental-frequency components

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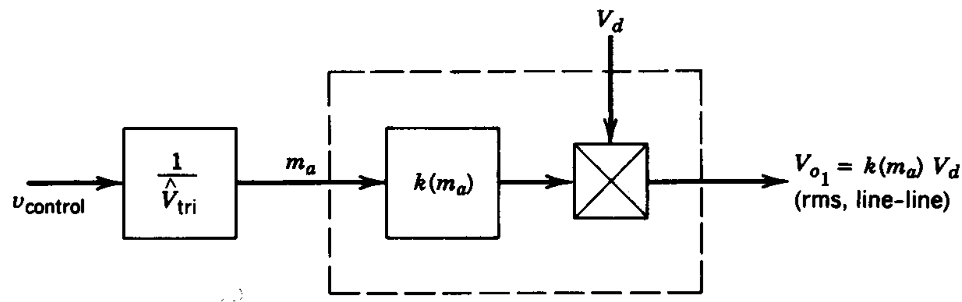
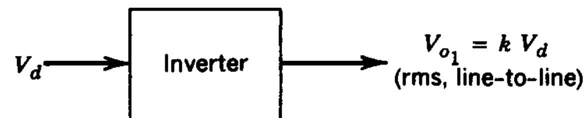
Summary of DC-AC Inverters



(a)



$k = 0.9$ 1-phase
$= 0.78$ 3-phase

(b)

Figure 8-38 Summary of inverter output voltages: (*a*) PWM operation ($m_a \leq 1$); (*b*) square-wave operation.

- Functional representation in a block-diagram form

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Chapter 9

Zero-Voltage or Zero-Current Switchings

Chapter 9 Resonant Converters: Zero-Voltage and/or Zero-Current Switchings 249

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- converters for soft switching

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One Inverter Leg

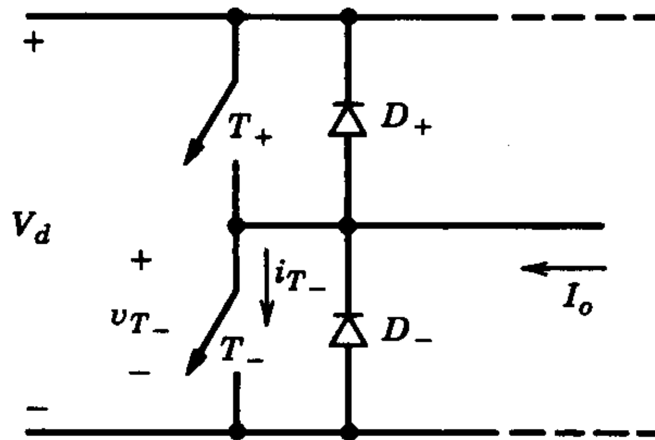

Figure 9-1 One inverter leg.

- The output current can be positive or negative

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Hard Switching Waveforms

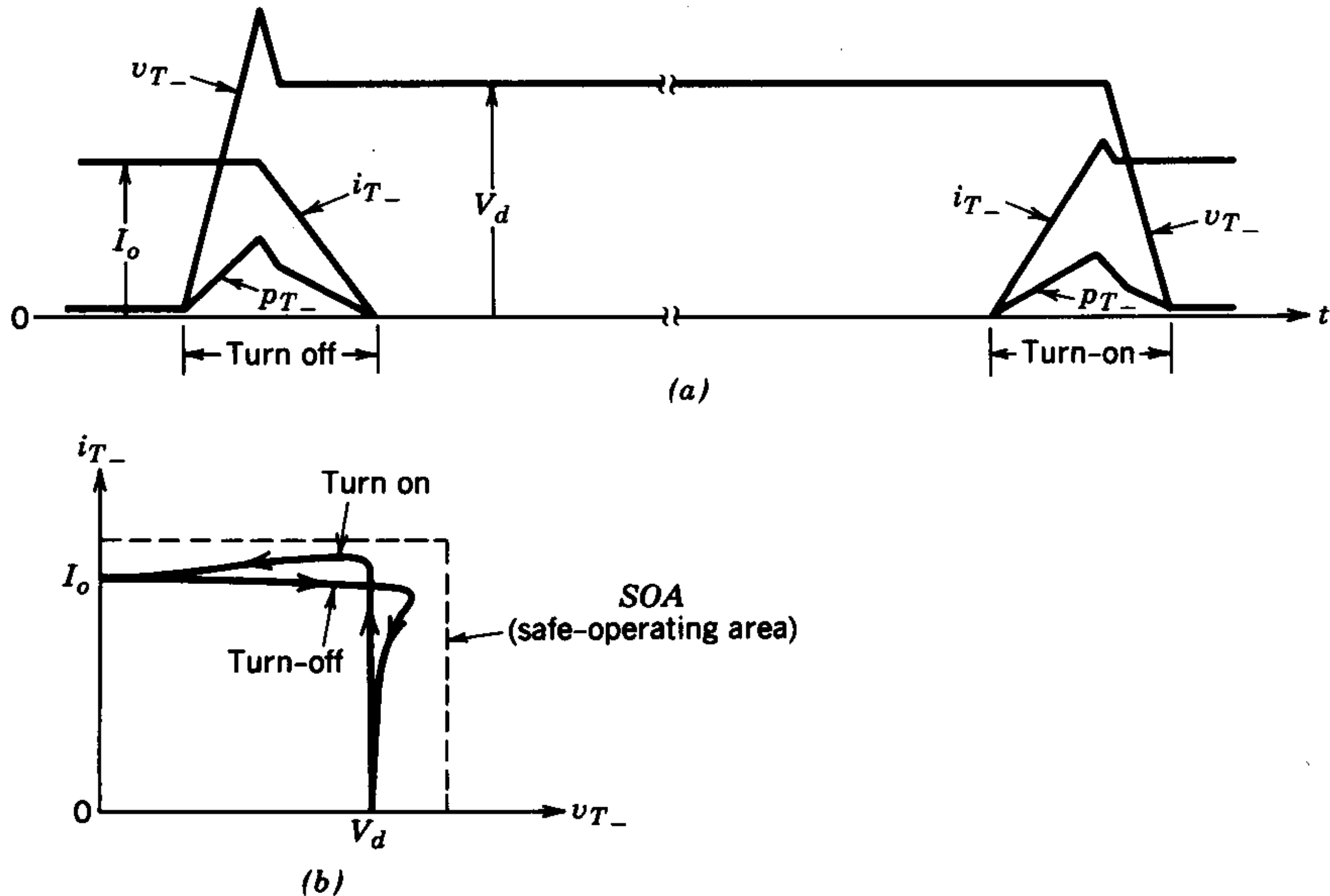

Figure 9-2 Switch-mode inductive current switchings.

- The output current can be positive or negative

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Turn-on and Turn-off Snubbers

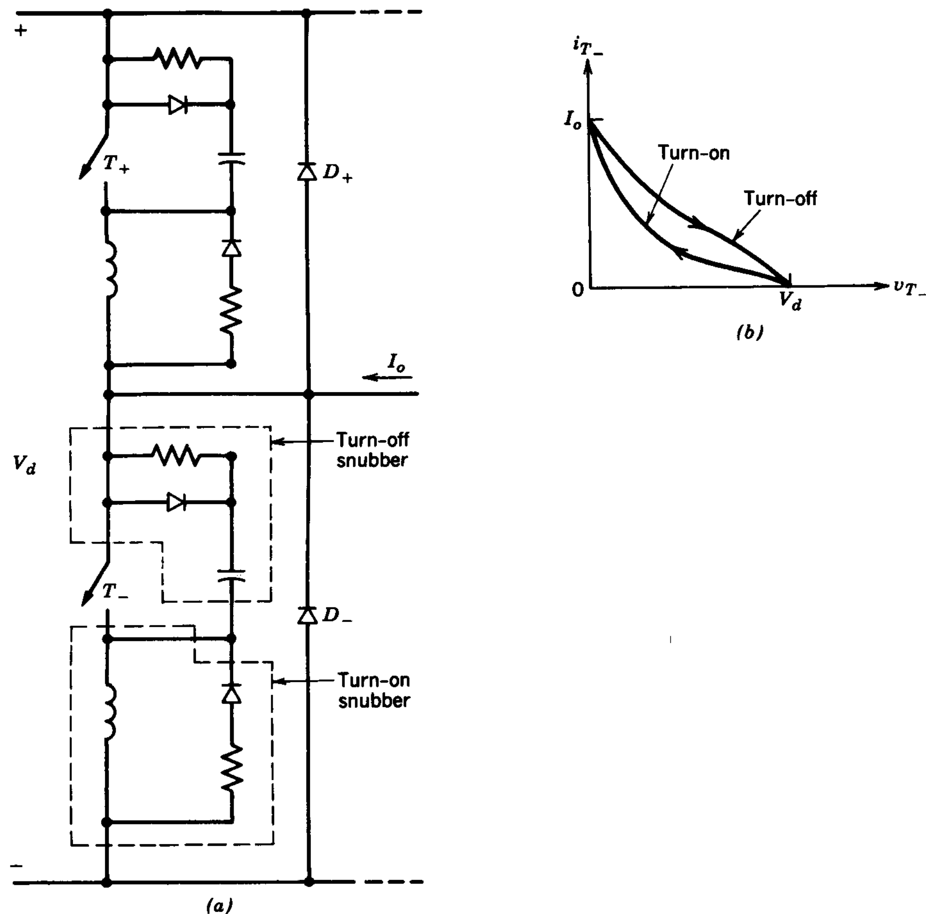

Figure 9-3 Dissipative snubbers: (*a*) snubber circuits; (*b*) switching loci with snubbers.

- Turn-off snubbers are used

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Switching Trajectories

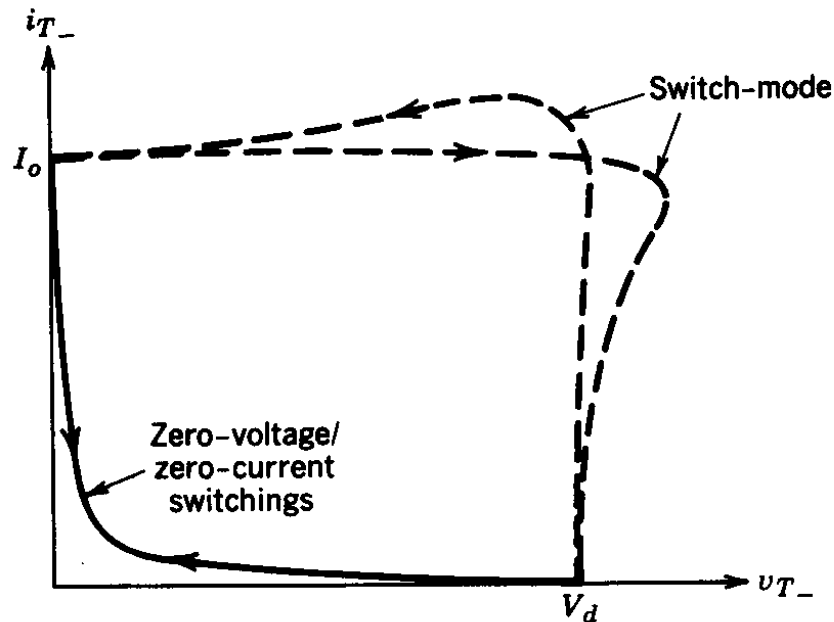

Figure 9-4 Zero-voltage-/zero-current-switching loci.

- Comparison of Hard versus soft switching

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Undamped Series-Resonant Circuit

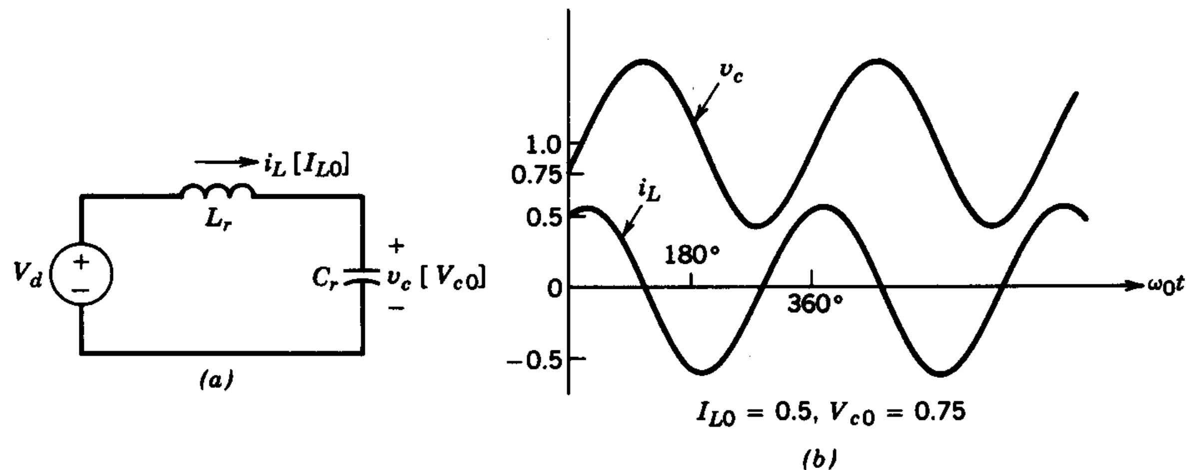

Figure 9-5 Undamped series-resonant circuit; i_L and v_c are normalized: (*a*) circuit; (*b*) waveforms with $I_{L0} = 0.5$, $V_{c0} = 0.75$.

- The waveforms shown include initial conditions

Series-Resonant Circuit with Capacitor-Parallel Load

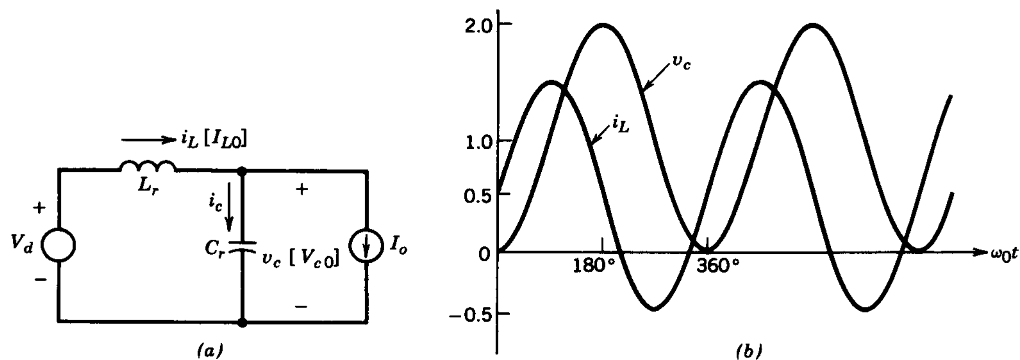

Figure 9-6 Series-resonant circuit with capacitor-parallel load (i_L and v_c are normalized): (*a*) circuit; (*b*) $\mathbf{V}_{c0} = 0$, $I_{L0} = I_o = 0.5$.

- The waveforms shown include initial conditions

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Impedance of a Series-Resonant Circuit

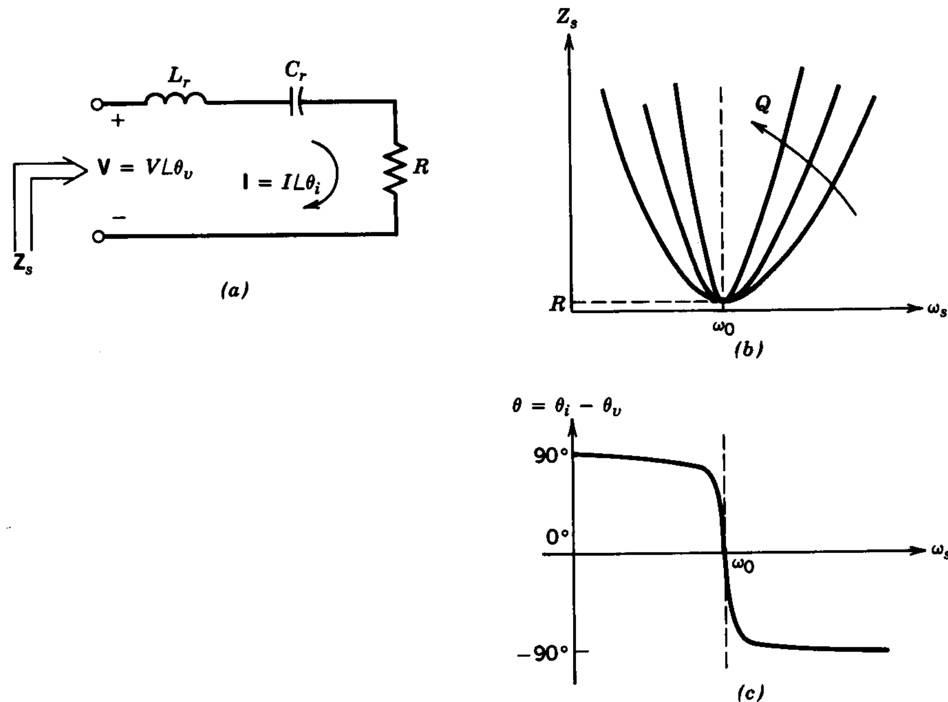

Figure 9-7 Frequency characteristics of a series-resonant circuit.

- The impedance is capacitive below the resonance frequency

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Undamped Parallel-Resonant Circuit

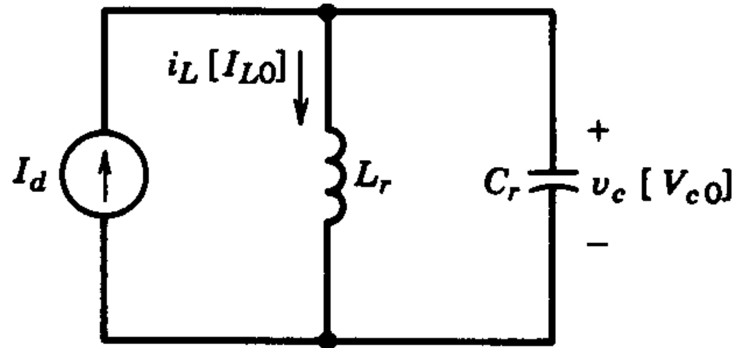

Figure 9-8 Undamped parallel-resonant circuit.

- Excited by a current source

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Impedance of a Parallel-Resonant Circuit

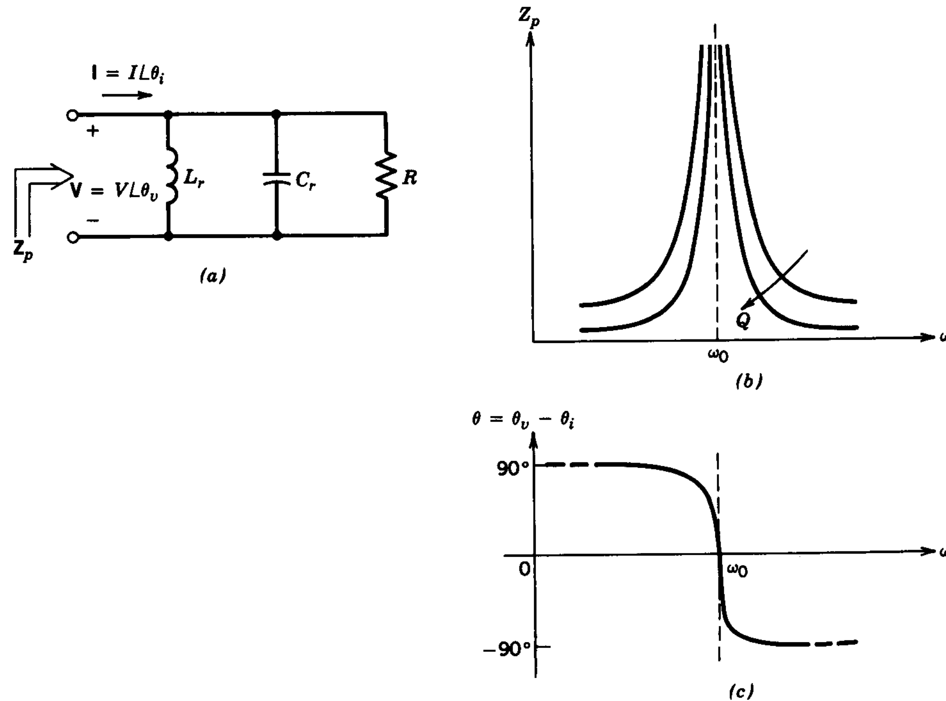

Figure 9-9 Frequency characteristics of a parallel-resonant circuit.

- The impedance is inductive at below the resonant frequency

Series Load Resonant (SLR) Converter

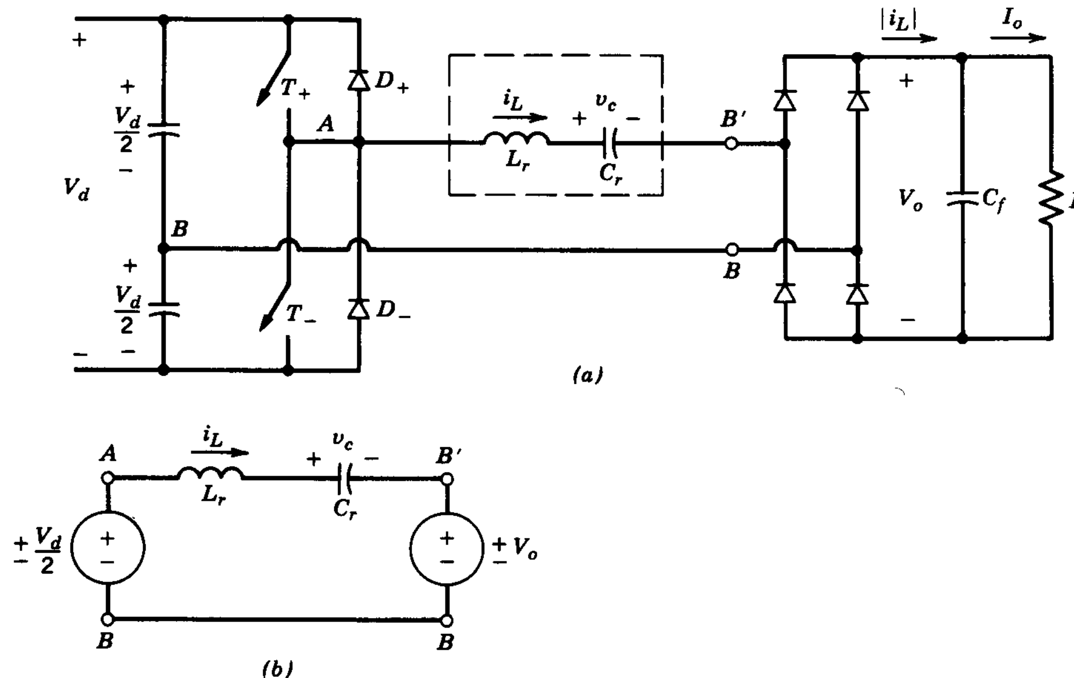

Figure 9-10 SLR dc–dc converter: (*a*) half-bridge; (*b*) equivalent circuit.

- The transformer is ignored in this equivalent circuit

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SLR Converter Waveforms

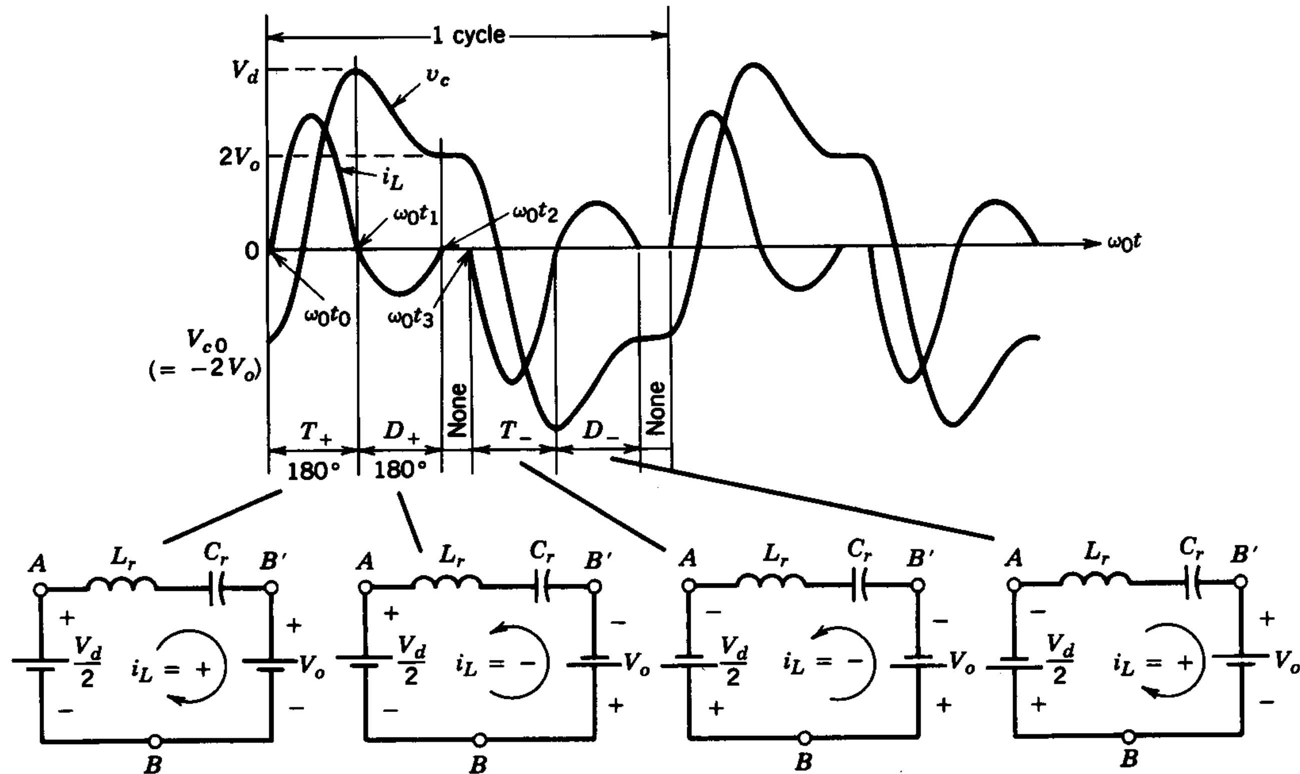

Figure 9-11 SLR dc–dc converter; discontinuous-conduction mode with $\omega_s < \frac{1}{2}\omega_0$.

- The operating frequency is below one-half the resonance frequency

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SLR Converter Waveforms

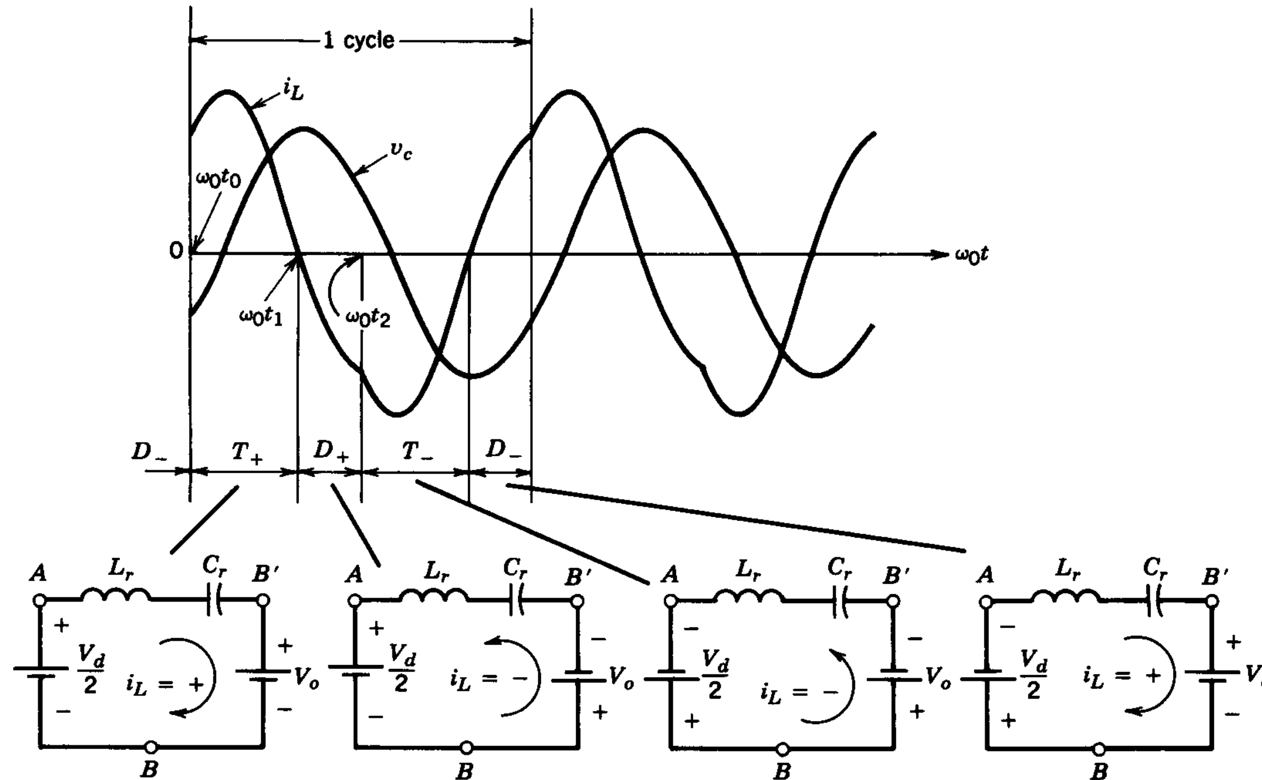

Figure 9-12 SLR dc–dc converter; continuous-conduction mode with $\frac{1}{2}\omega_0 < \omega_s < \omega_0$.

- The operating frequency is in between one-half the resonance frequency and the resonance frequency

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SLR Converter Waveforms

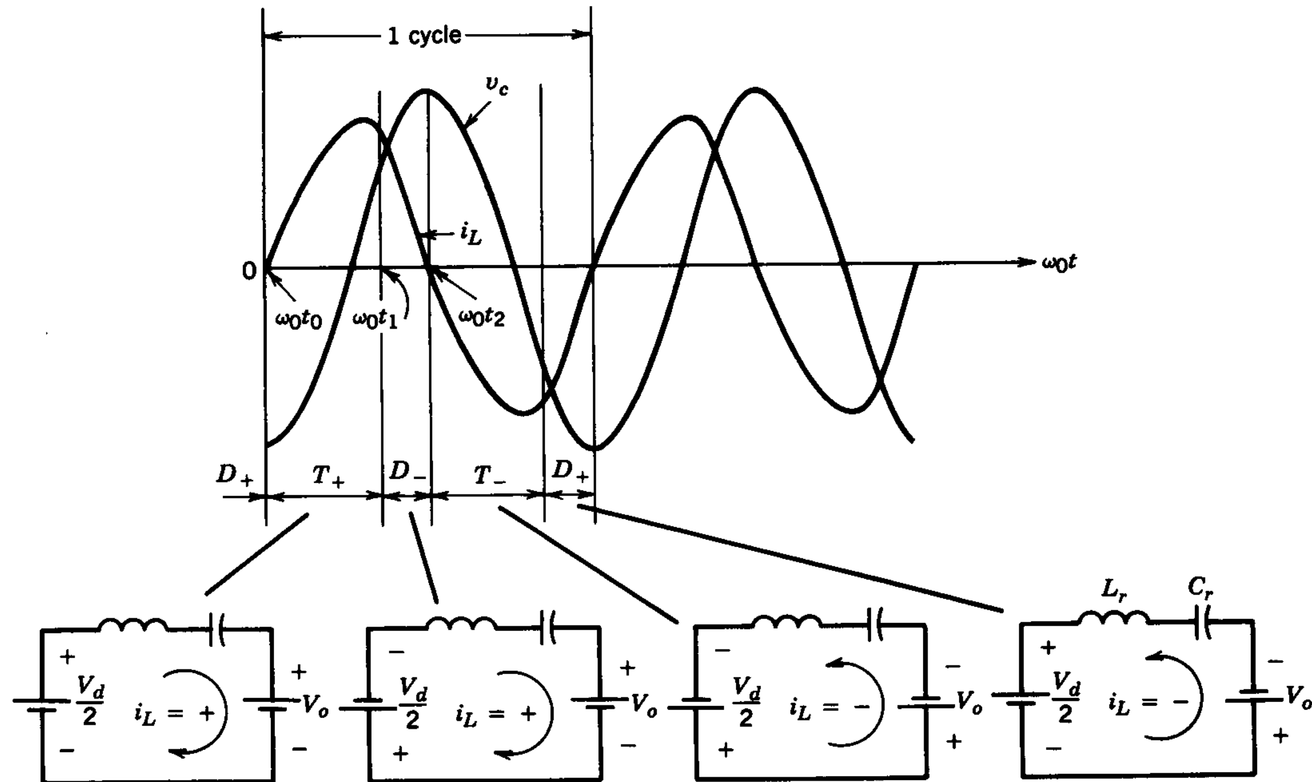

Figure 9-13 SLR dc–dc converter; continuous-conduction mode with $\omega_s > \omega_0$.

- The operating frequency is above the resonance frequency

Lossless Snubbers in SLR Converters

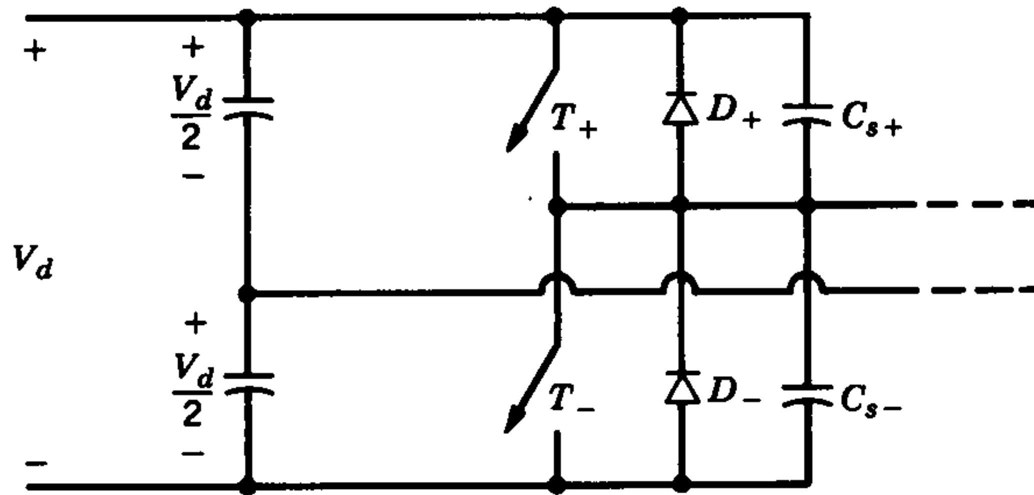

Figure 9-14 Lossless snubbers in an SLR converter at $\omega_s > \omega_0$.

- The operating frequency is above the resonance frequency

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SLR Converter Characteristics

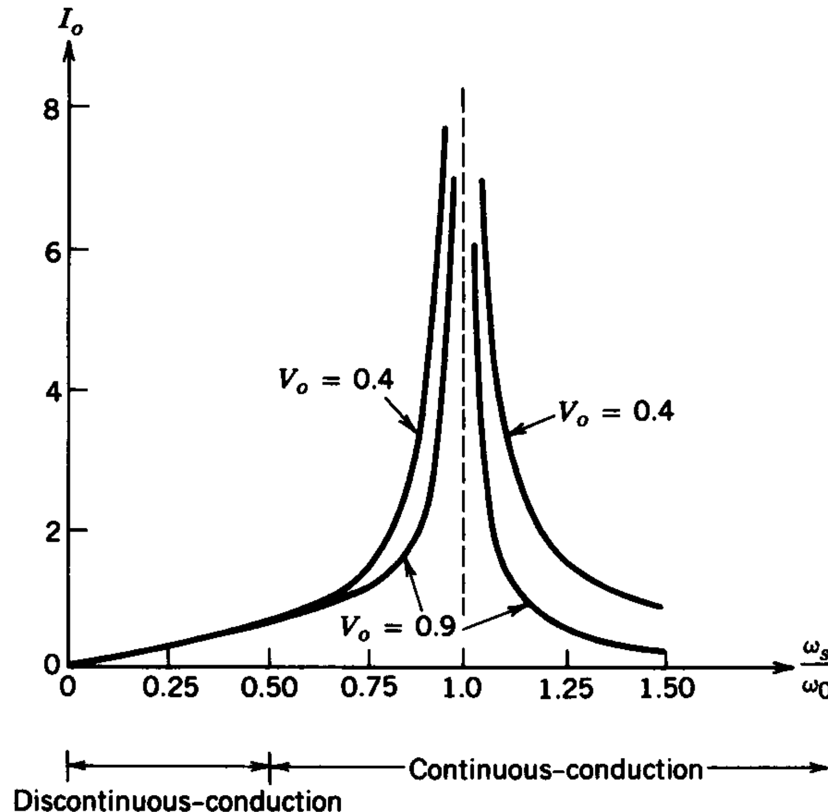

Figure 9-15 Steady-state characteristics of an SLR dc–dc converter; all parameters are normalized.

- Output Current as a function of operating frequency for various values of the output voltage

SLR Converter Control

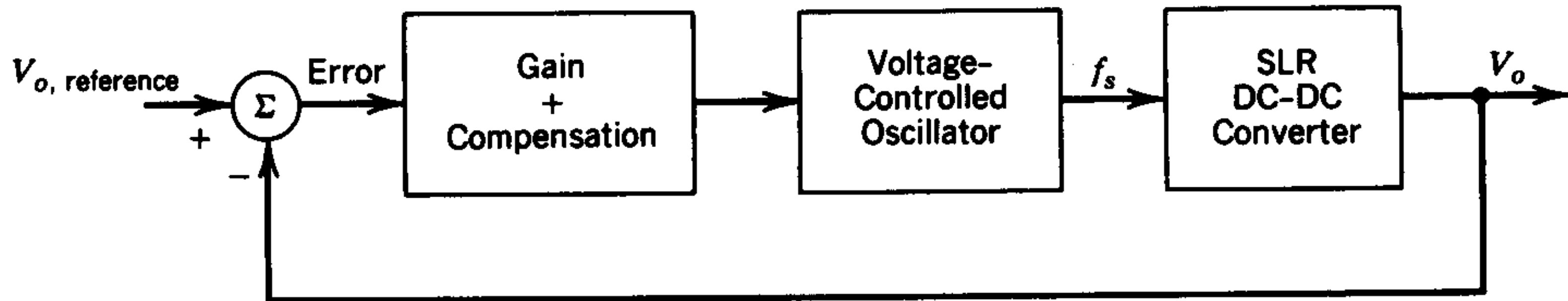

Figure 9-16 Control of SLR dc–dc converter.

- The operating frequency is varied to regulate the output voltage

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Parallel Load Resonant (PLR) Converter

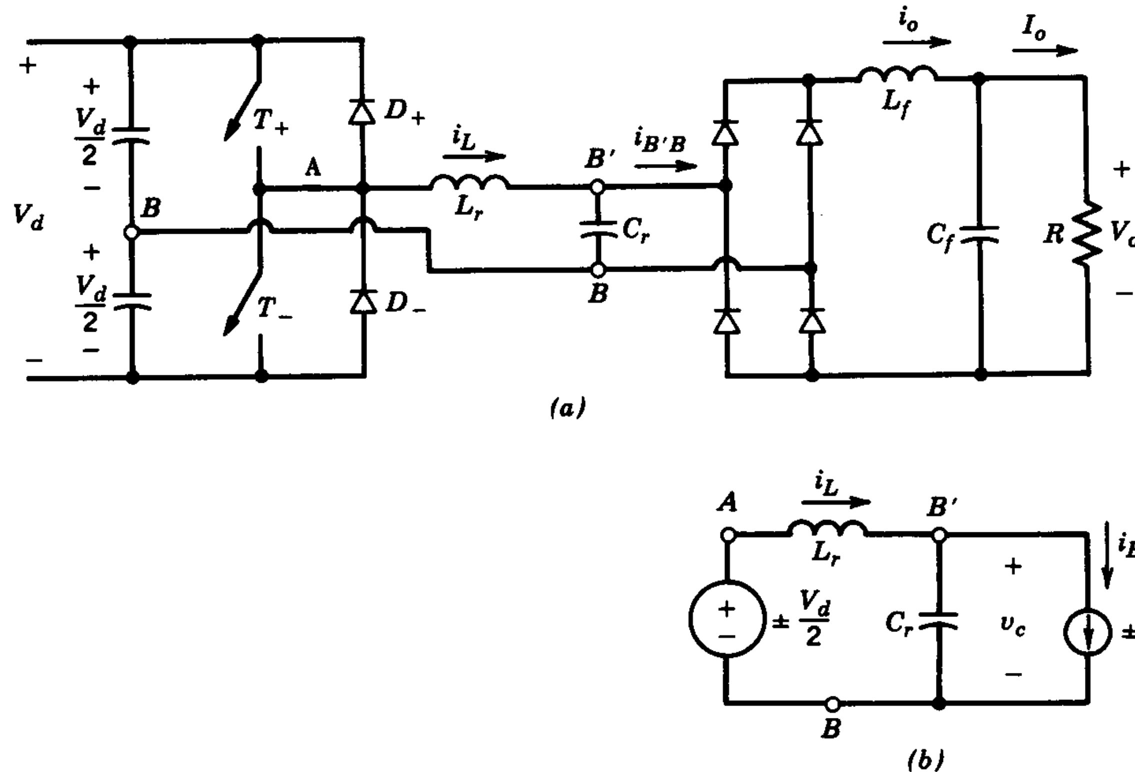

Figure 9-17 PLR dc–dc converter: (*a*) half-bridge; (*b*) equivalent circuit.

- The transformer is ignored in this equivalent circuit

PLR Converter Waveforms

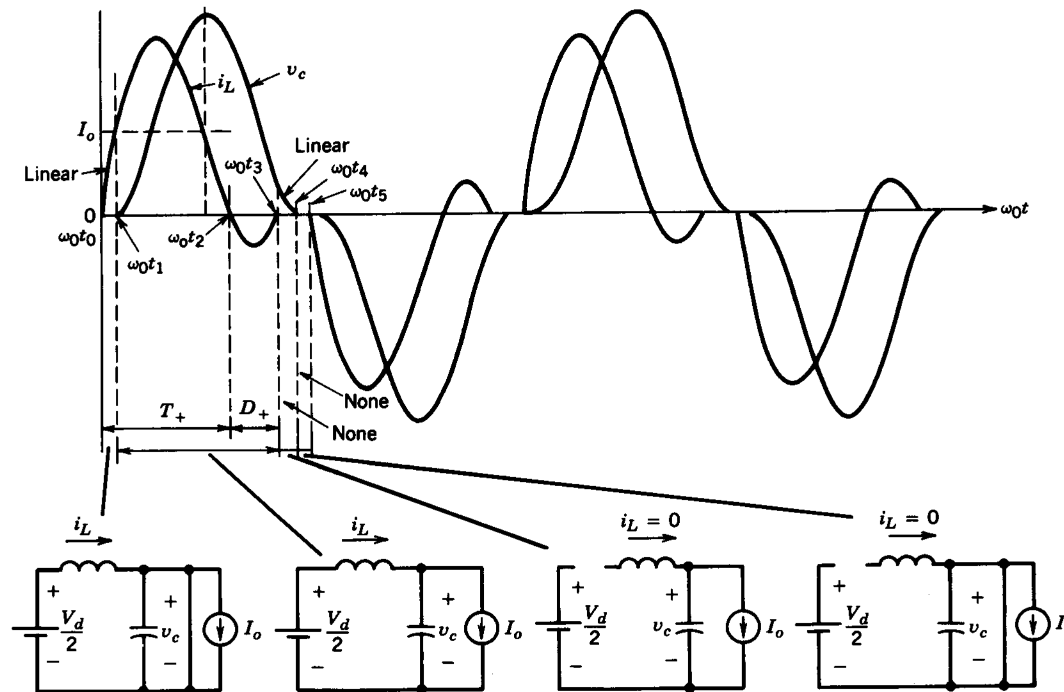

Figure 9-18 PLR dc–dc converter in a discontinuous mode.

- The current is in a discontinuous conduction mode

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PLR Converter Waveforms

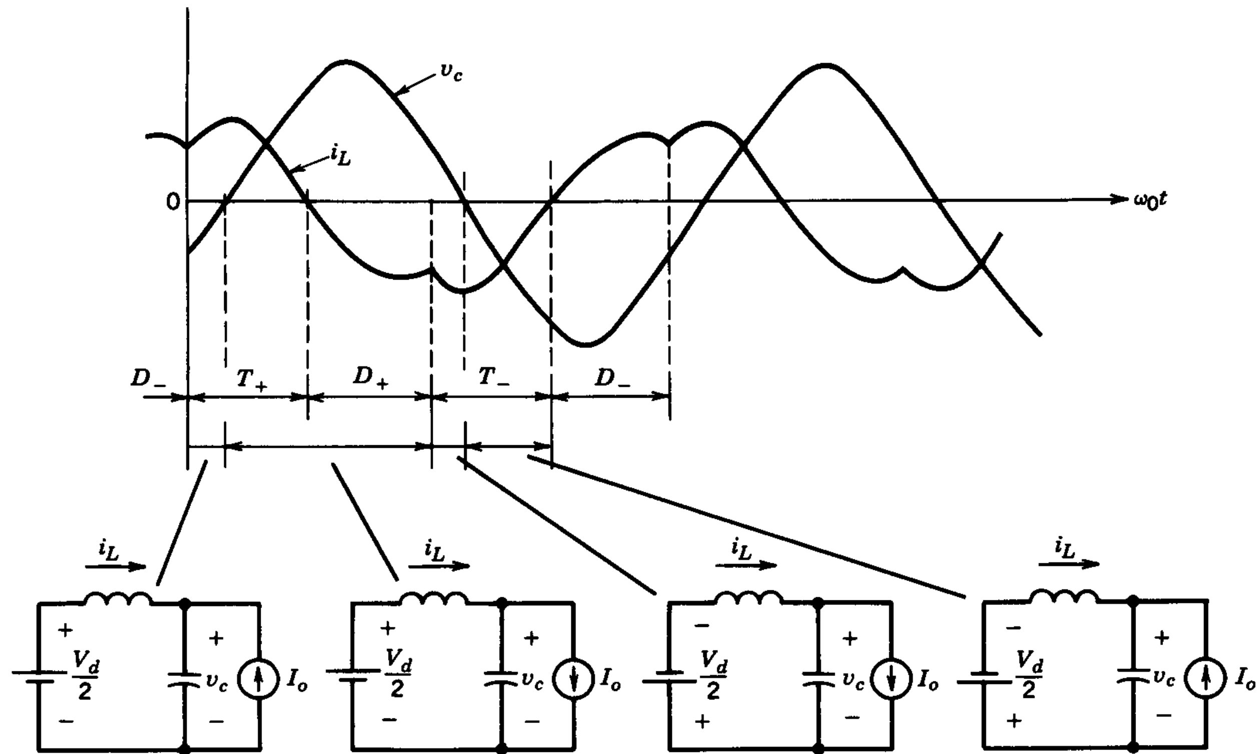

Figure 9-19 PLR dc−dc converter in a continuous mode with $\omega_s < \omega_0$.

• The operating frequency is below the resonance frequency

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PLR Converter Waveforms

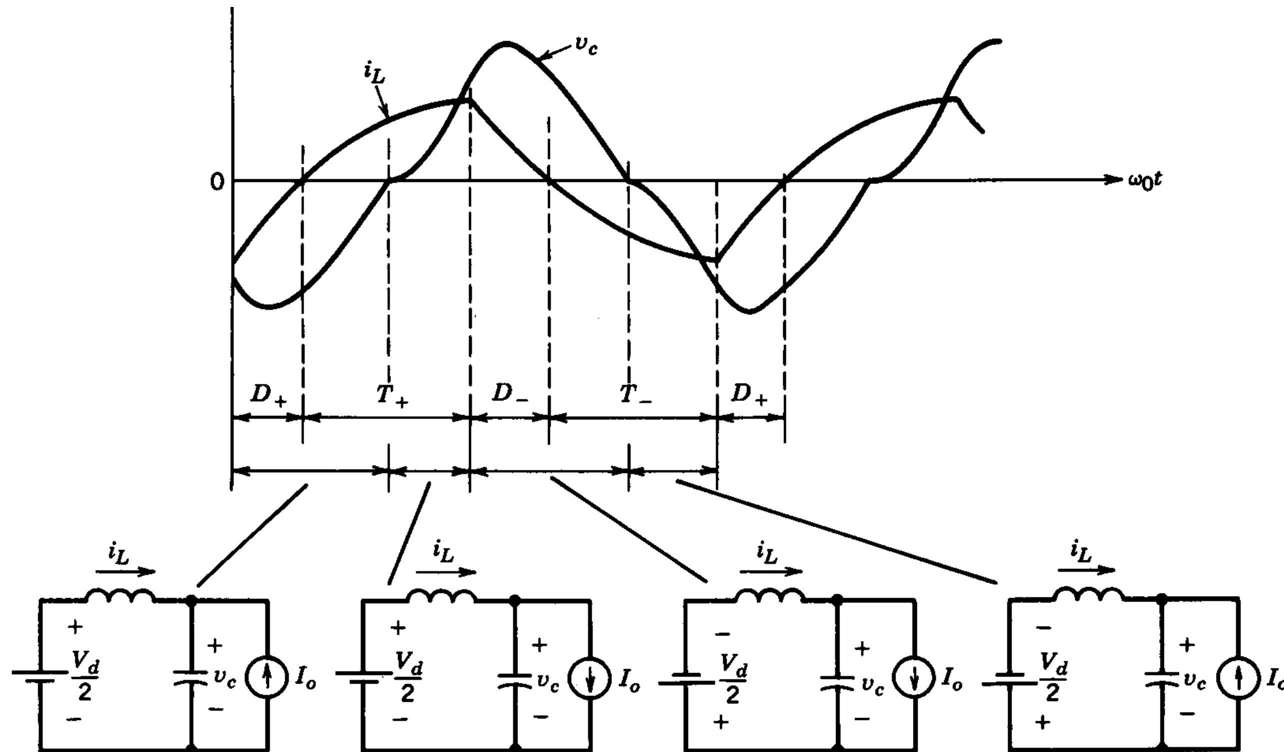

Figure 9-20 PLR dc–dc converter in a continuous mode with $\omega_s > \omega_0$.

- The operating frequency is above the resonance frequency

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PLR Converter Characteristics

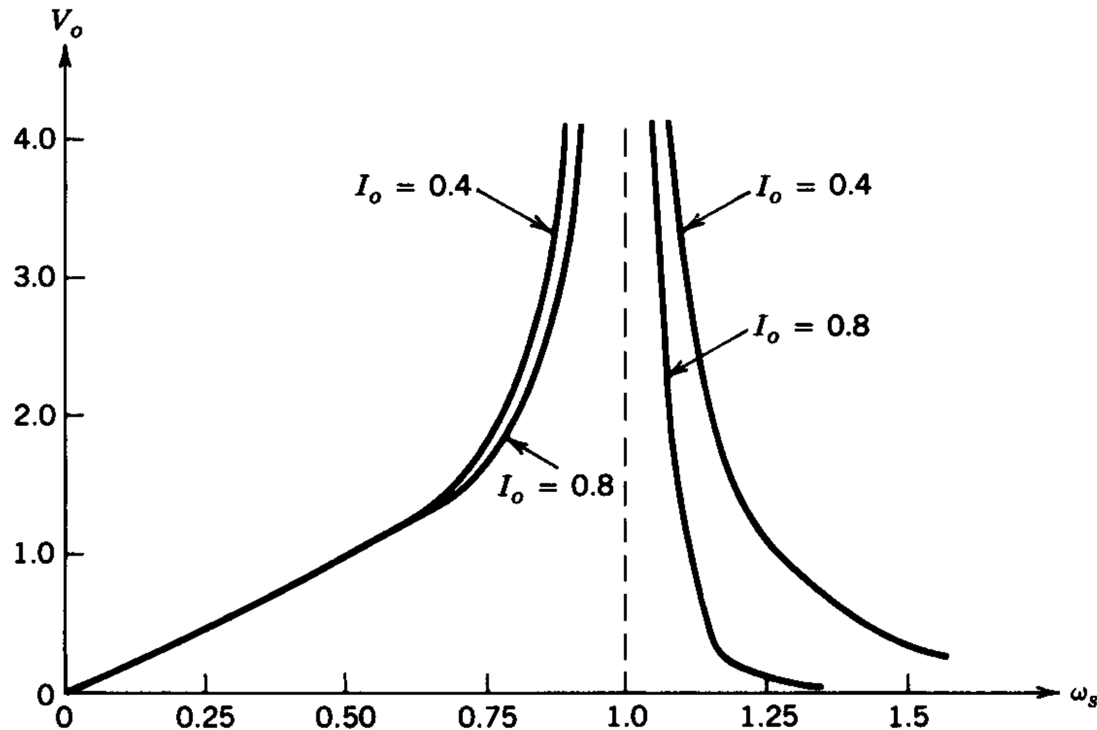

Figure 9-21 Steady-state characteristics of a PLR dc–dc converter. All quantities are normalized.

- Output voltage as a function of operating frequency for various values of the output current

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Hybrid-Resonant DC-DC Converter

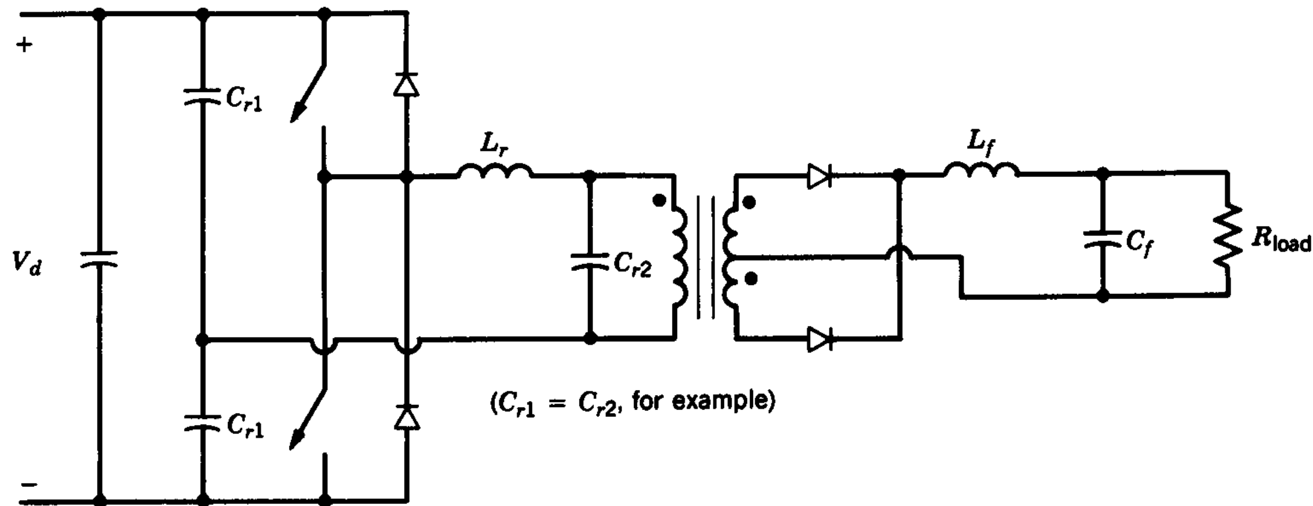

Figure 9-22 Hybrid-resonant dc–dc converter.

- Combination of series and parallel resonance

Parallel-Resonant Current-Source Converter

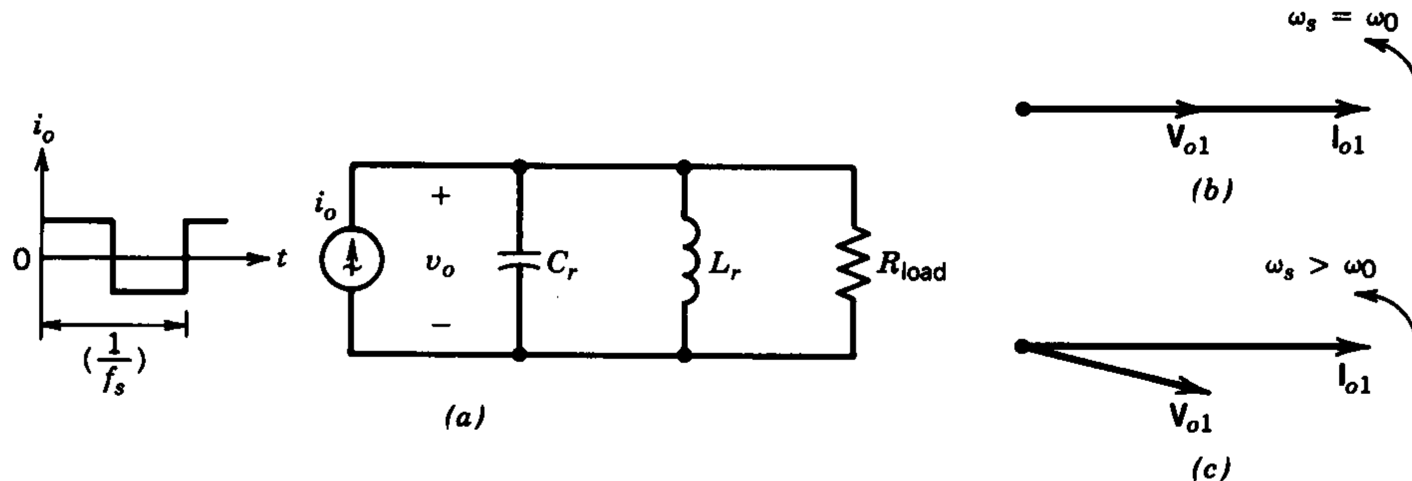

Figure 9-23 Basic circuit for current-source, parallel-resonant converter for induction heating: (*a*) basic circuit; (*b*) phasor diagram at $\omega_s = \omega_0$; (*c*) phasor diagram at $\omega_s > \omega_0$.

- Basic circuit to illustrate the operating principle at the fundamental frequency

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Parallel-Resonant Current-Source Converter

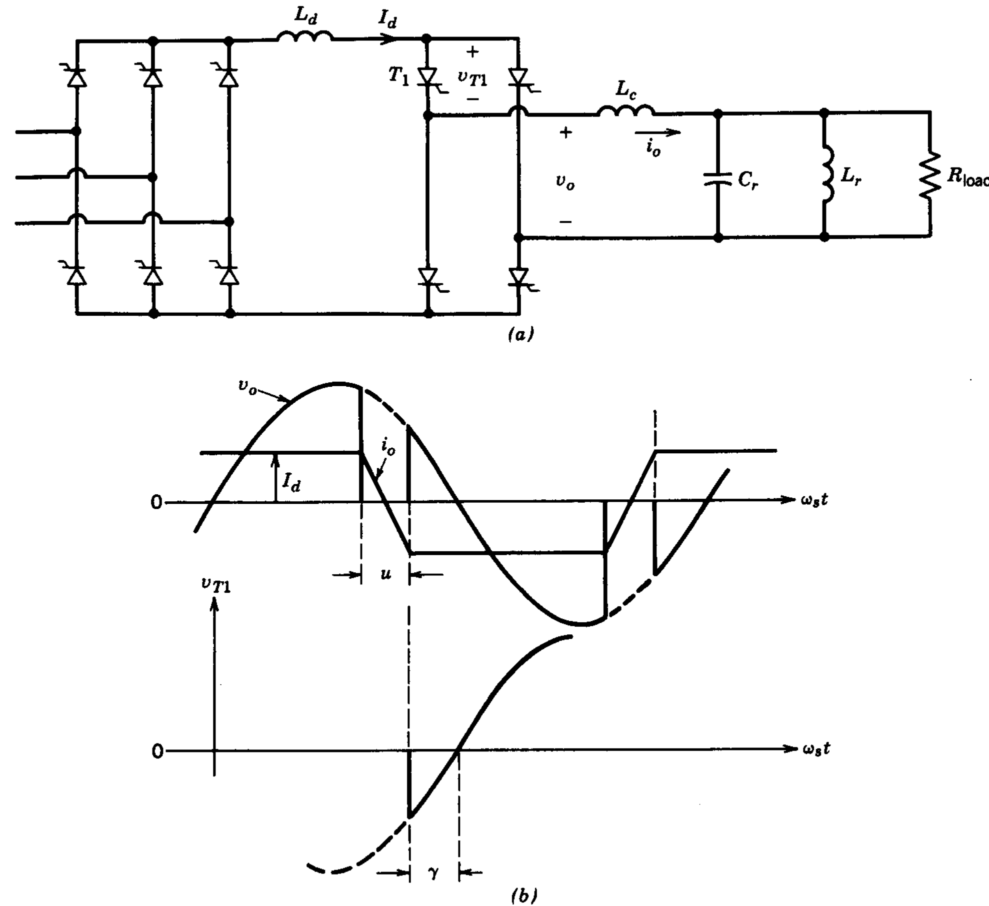

Figure 9-24 Current-source, parallel-resonant inverter for induction heating: (*a*) circuit; (*b*) waveforms.

- Using thyristors; for induction heating

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Class-E Converters

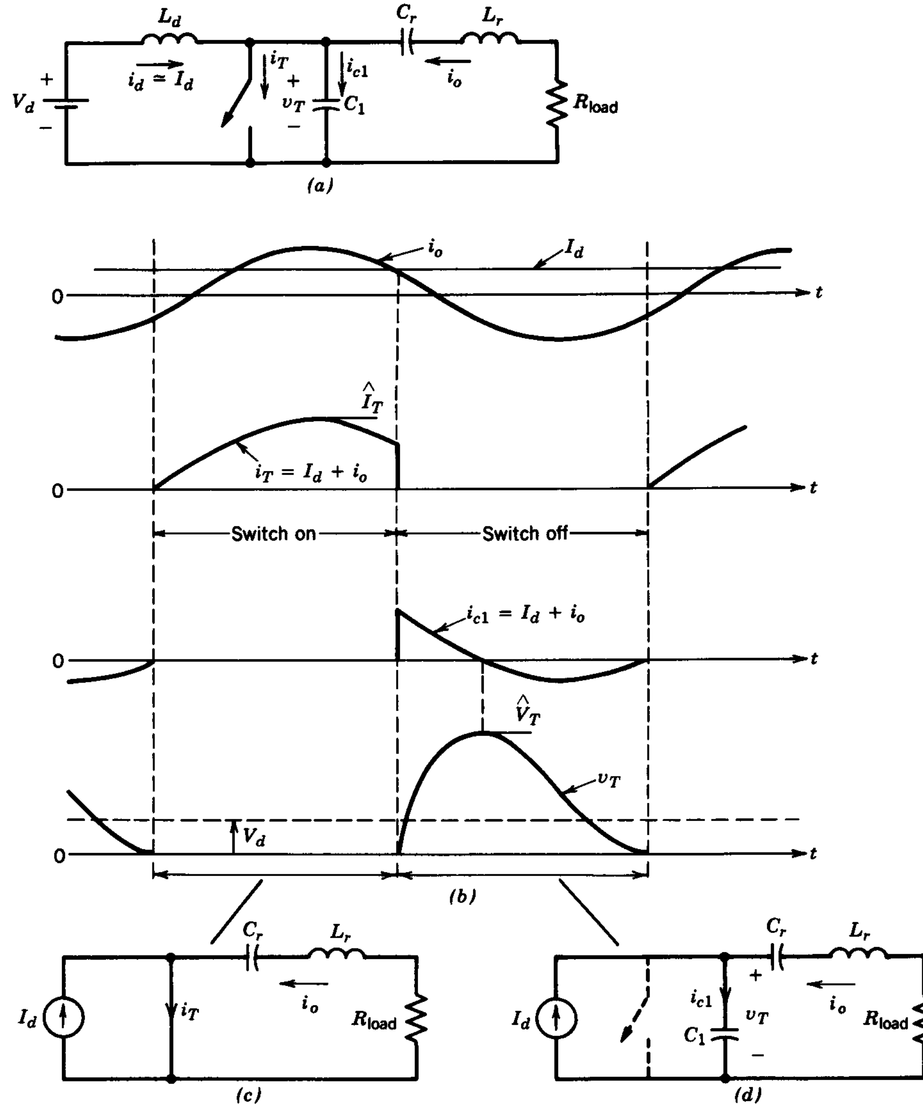

Figure 9-25 Class E converter (optimum mode, $D = 0.5$).

Optimum mode

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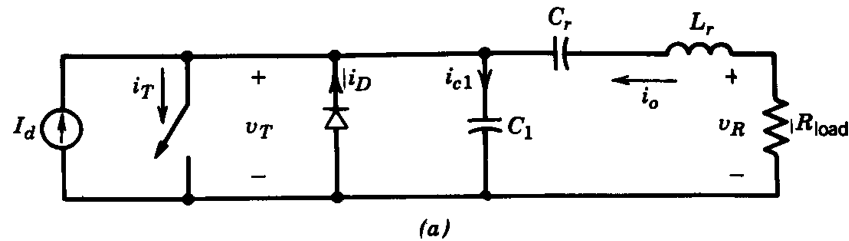
Class-E Converters



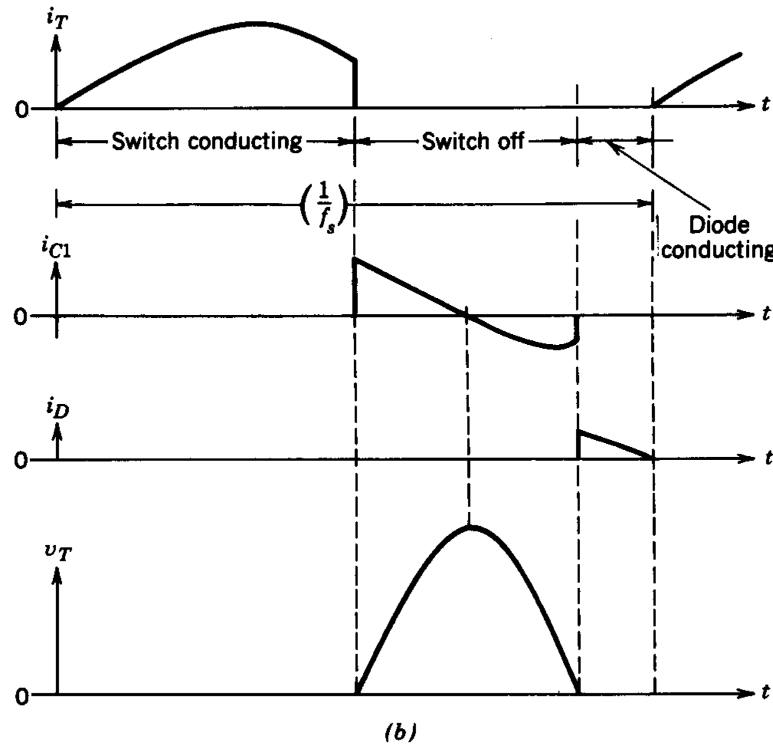


Figure 9-26 Class E converter (nonoptimum mode).

Non-Optimum mode

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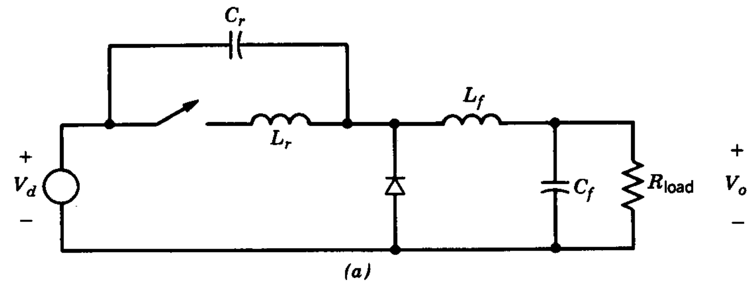
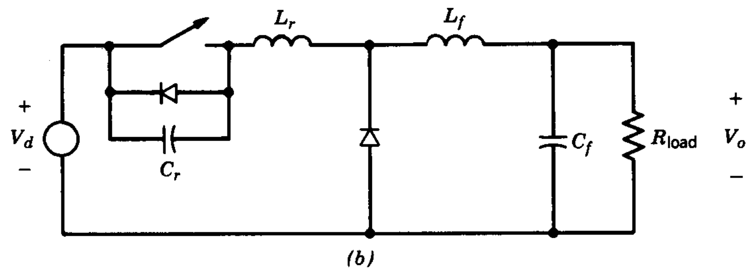
Resonant Switch Converters





Classifications

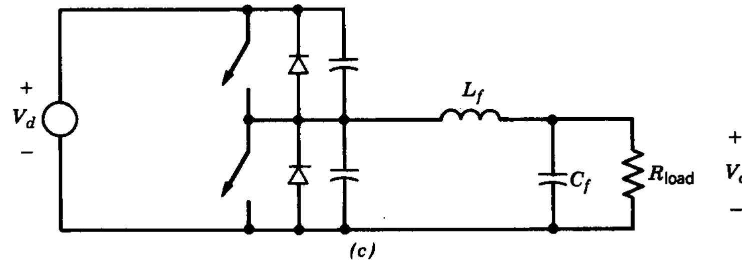


Figure 9-27 Resonant-switch converters: (a) ZCS dc–dc converter (step-down); (*b*) ZVS dc–dc converter (step-down); (*c*) ZVS-CV dc–dc converter (step-down).

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ZCS Resonant-Switch Converter

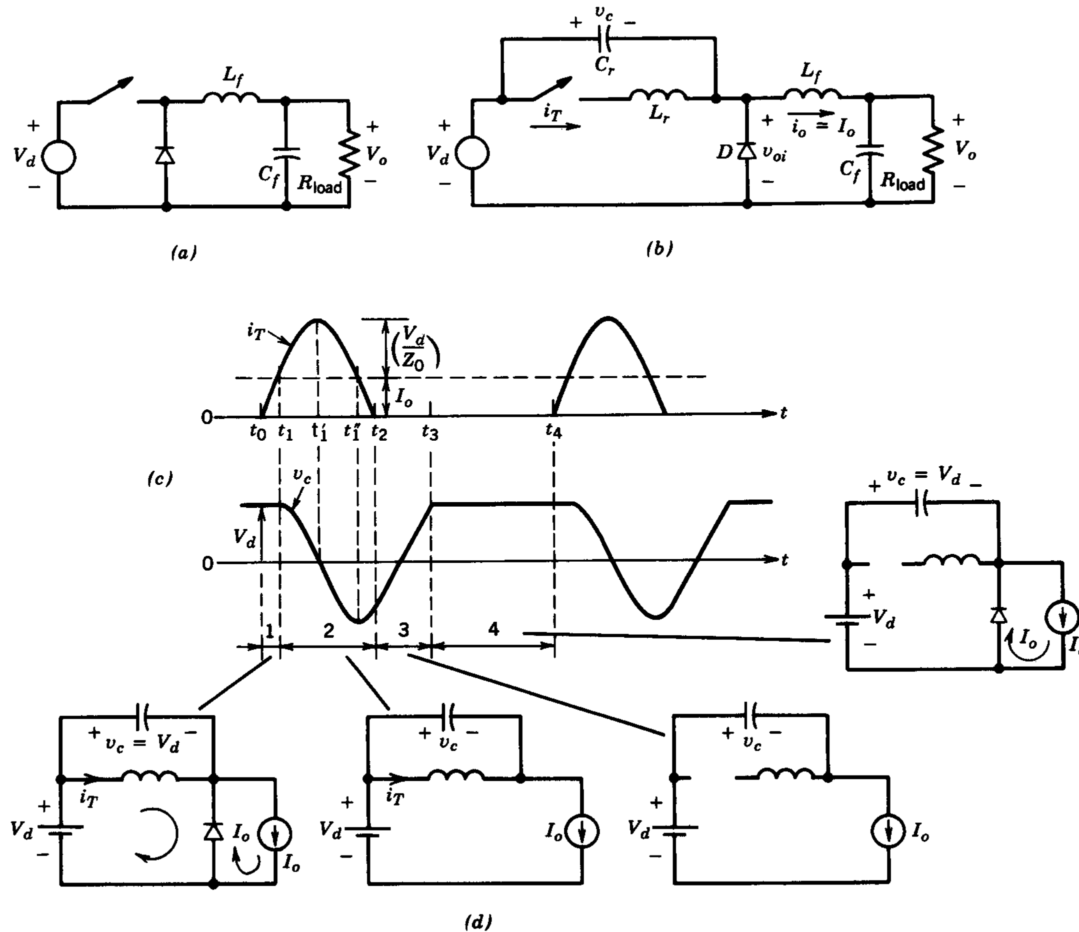

Figure 9-28 ZCS resonant-switch dc–dc converter.

- One possible implementation

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ZCS Resonant-Switch Converter

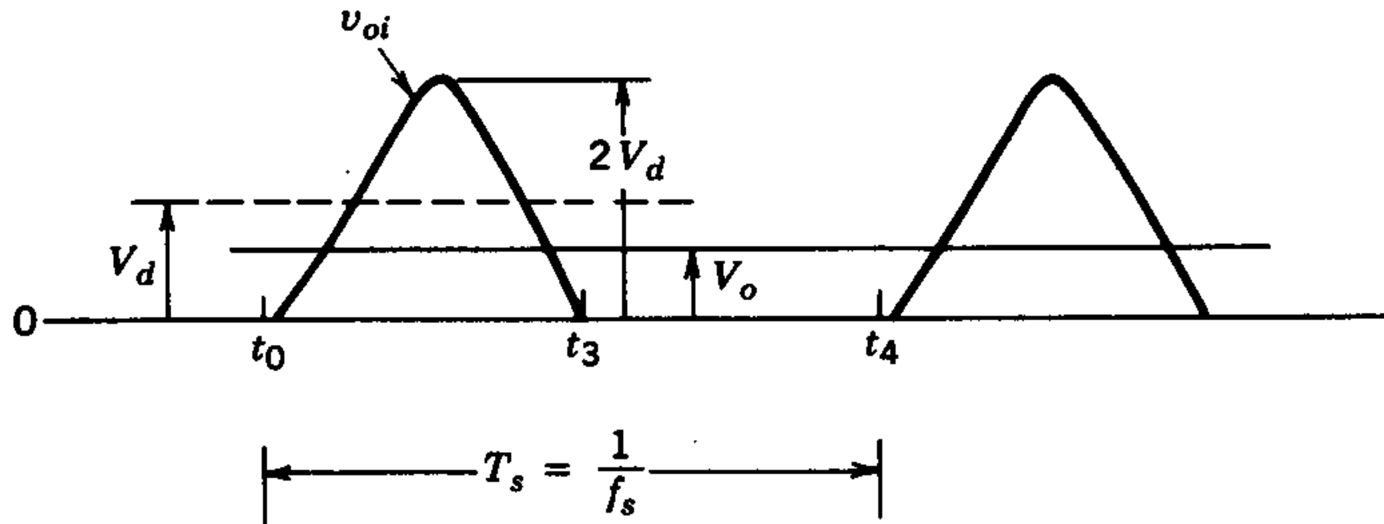

Figure 9-29 v_{oi} waveform in a ZCS resonant-switch dc–dc converter.

- Waveforms; voltage is regulated by varying the switching frequency

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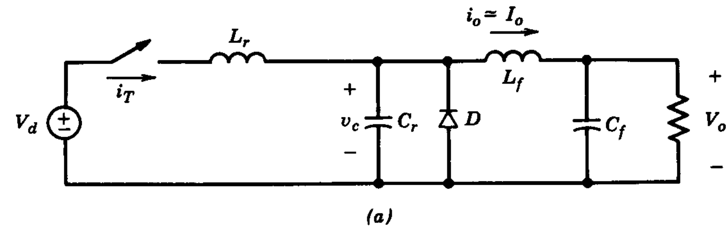
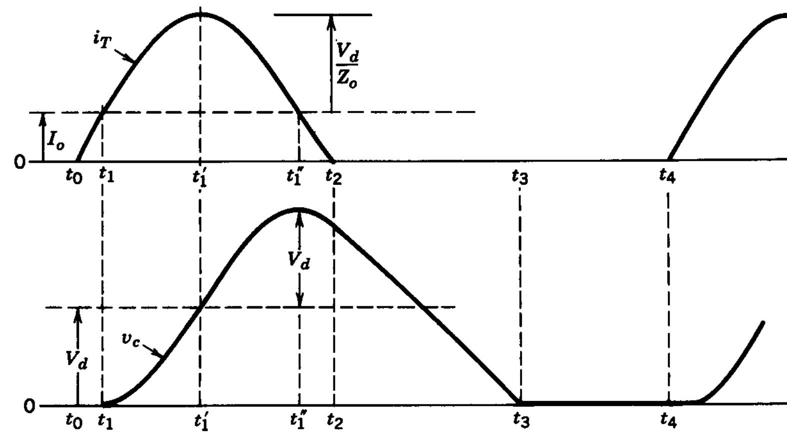
ZCS Resonant-Switch Converter



- A practical circuit



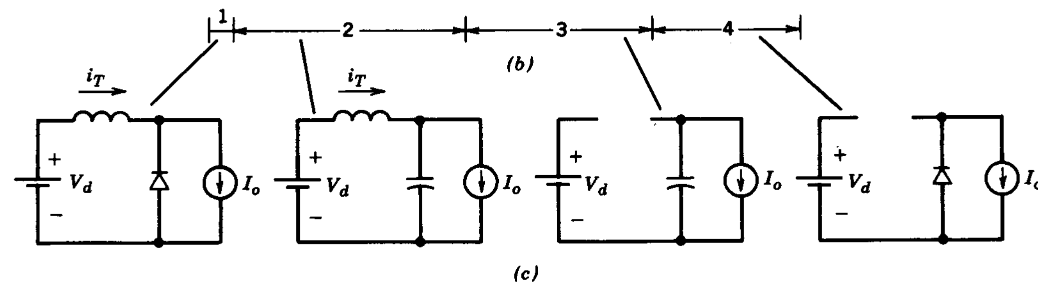


Figure 9-30 ZCS resonant-switch dc–dc converter; alternate configuration.

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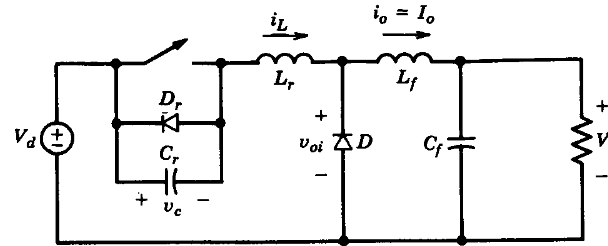
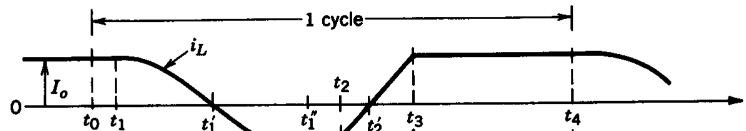
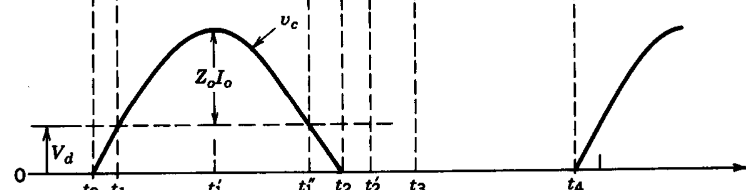
ZVS Resonant-Switch Converter





(b)



- Serious limitations

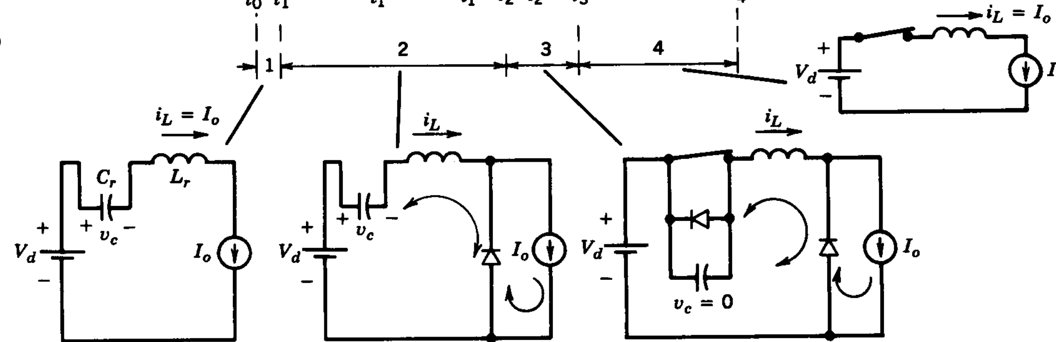


Figure 9-31 ZVS resonant-switch dc–dc converter.

ZVS Resonant-Switch Converter

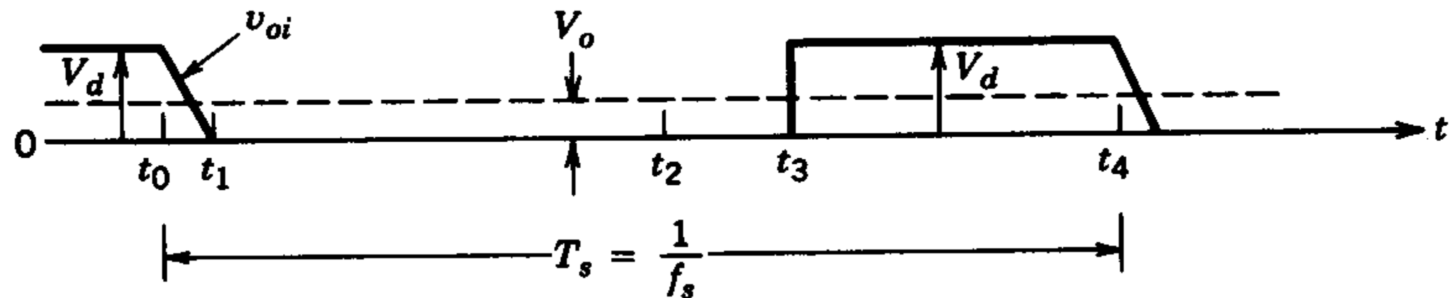


Figure 9-32 The v_{oi} waveform in a ZVS resonant-switch dc–dc converter.

- Waveforms

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MOSFET Internal Capacitances

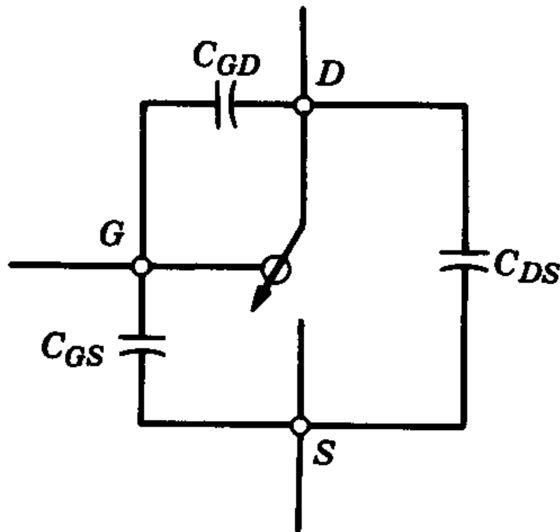

Figure 9-33 Switch internal capacitances.

- These capacitances affect the MOSFET switching

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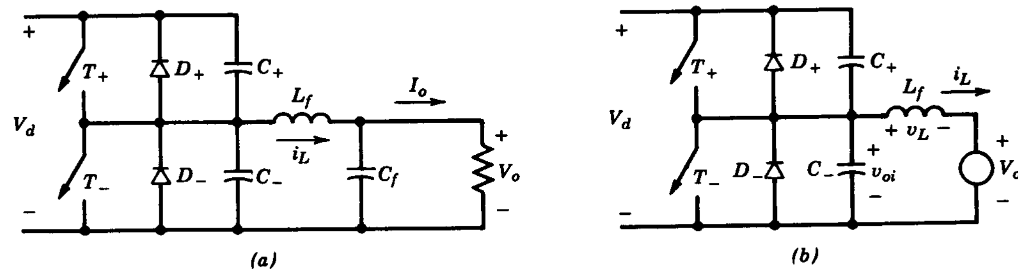
ZVS-CV DC-DC Converter



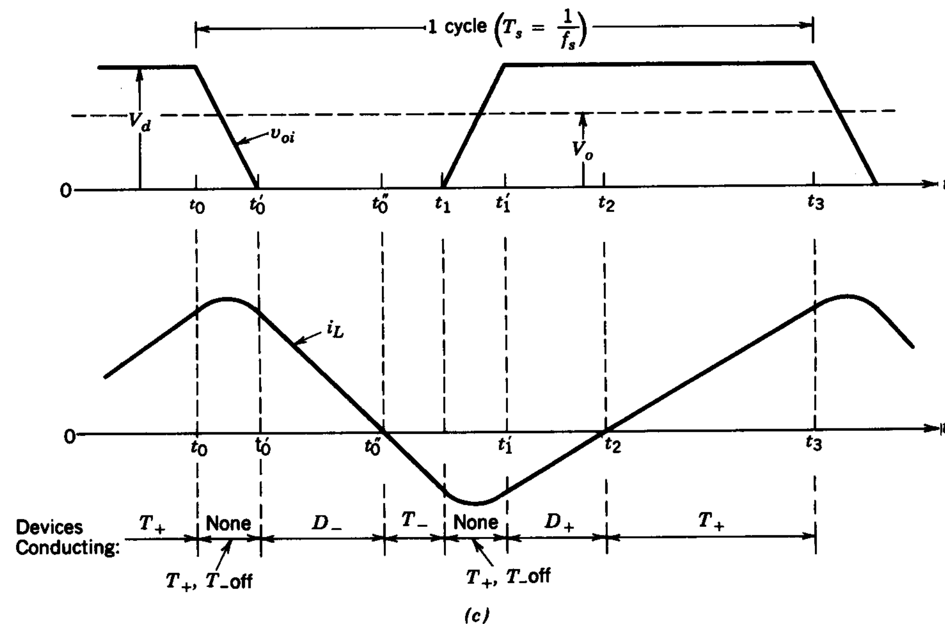


Figure 9-34 ZVS-CV dc–dc converter.

- The inductor current must reverse direction during each switching cycle

ZVS-CV DC-DC Converter

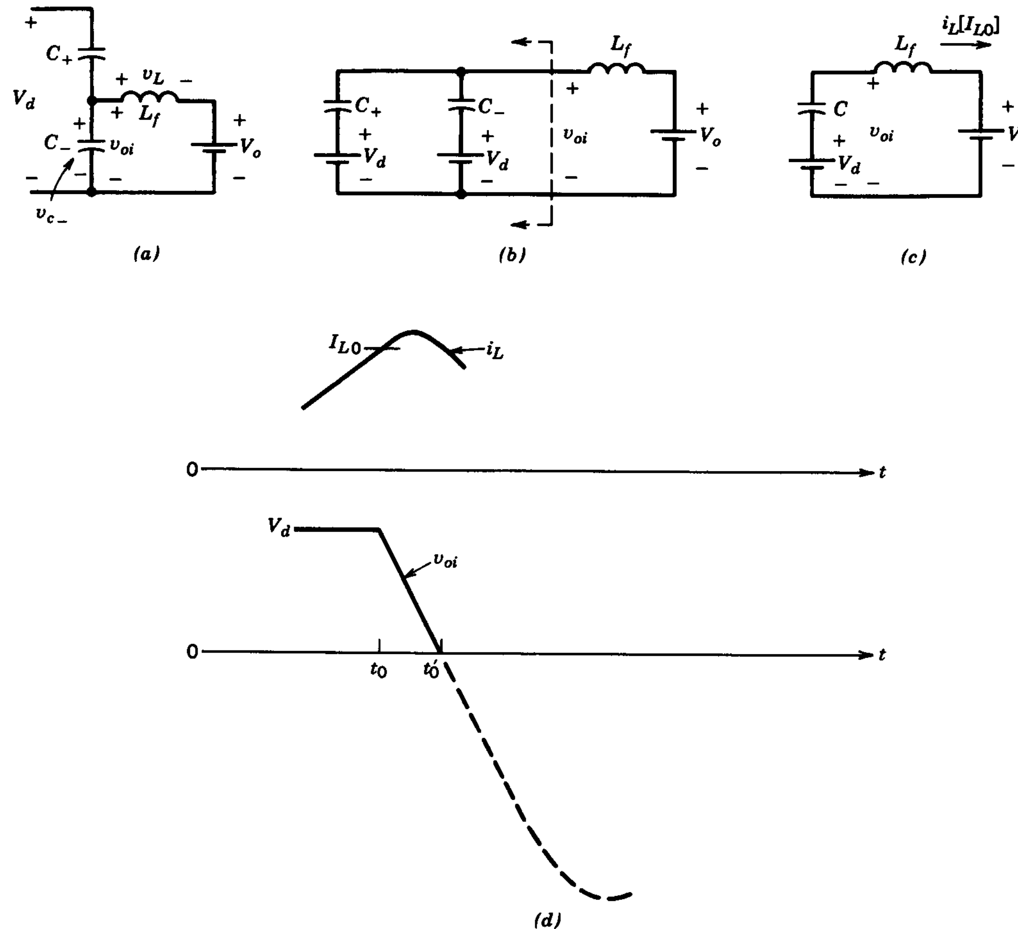
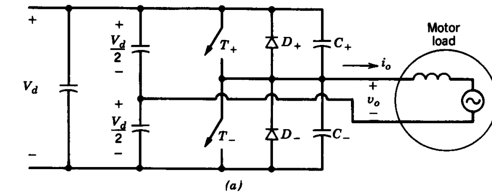
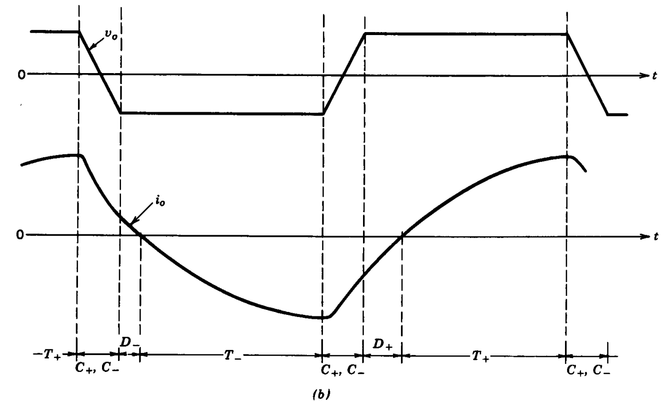


Figure 9-35 ZVS-CV dc–dc converter; T_+, T_- off.

- One transition is shown

ZVS-CV Principle Applied to DC-AC Inverters





- Very large ripple in the output current

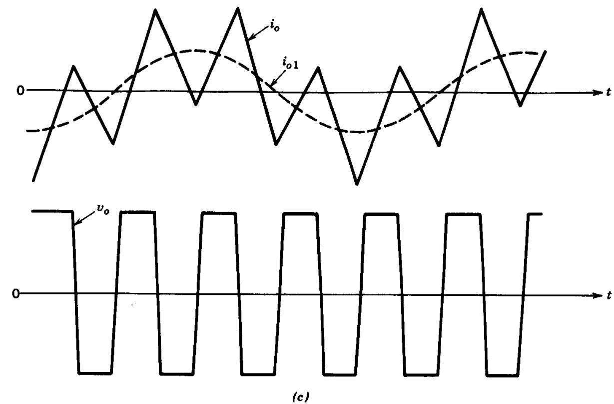


Figure 9-36 ZVS-CV dc-to-ac inverter: (*a*) half-bridge; (*b*) square-wave mode; (*c*) current-regulated mode.

Three-Phase ZVS-CV DC-AC Inverter

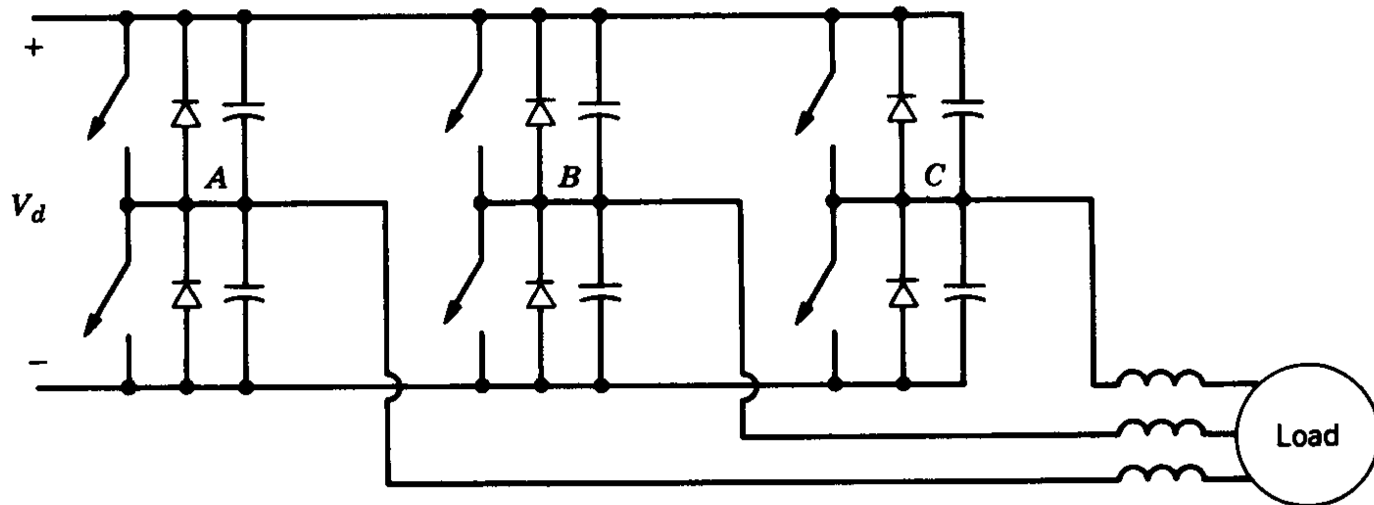


Figure 9-37 Three-phase, ZVS-CV dc-to-ac inverter.

- Very large ripple in the output current

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Output Regulation by Voltage Control

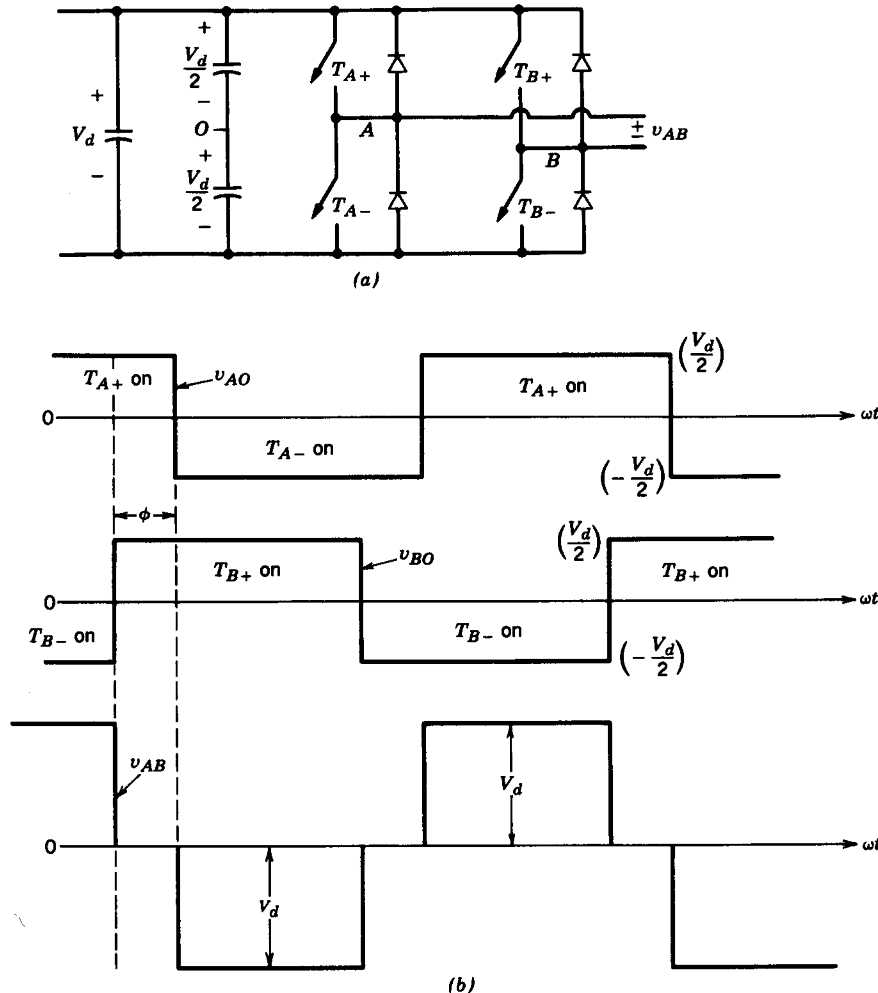

Figure 9-38 Voltage control by voltage cancellation: conventional switch-mode converter.

- Each pole operates at nearly 50% duty-ratio

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ZVS-CV with Voltage Cancellation

- Commonly used

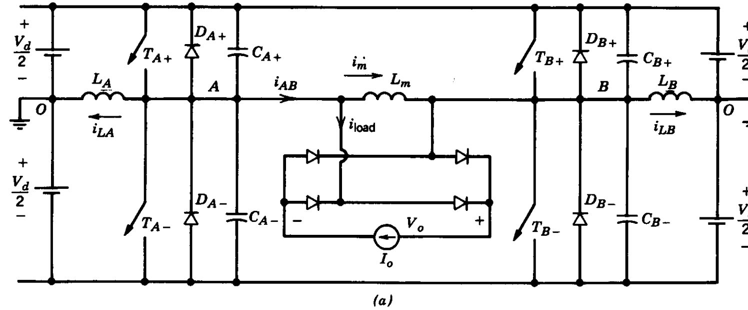
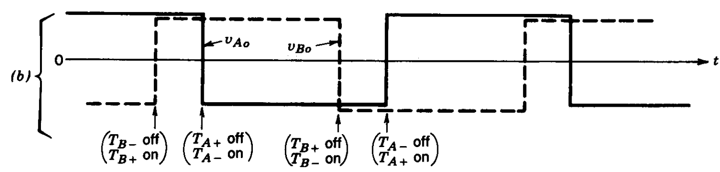
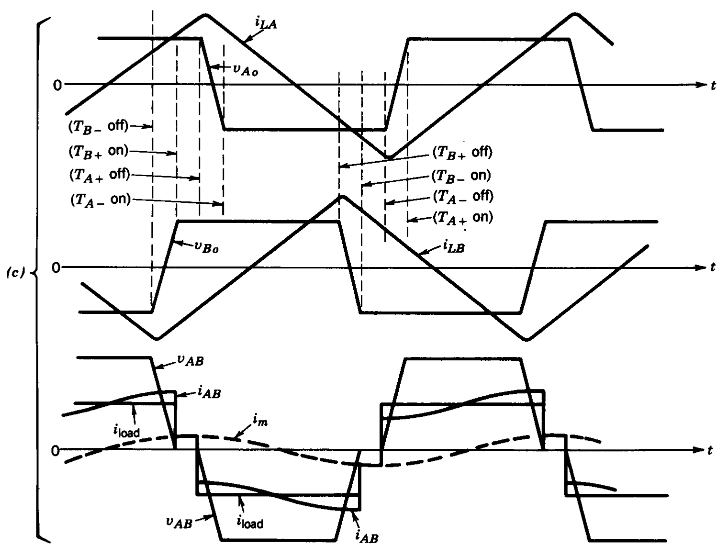

Figure 9-39 ZVS-CV full-bridge dc–dc converter: (*a*) circuit; (*b*) idealized switch-mode waveforms; (*c*) ZVS-CV waveforms.

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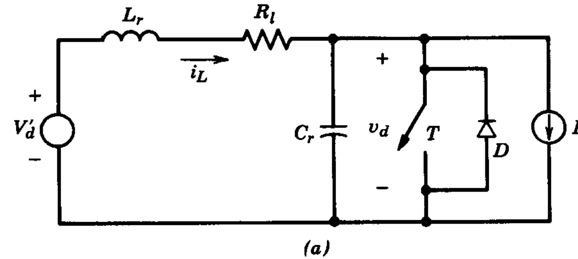
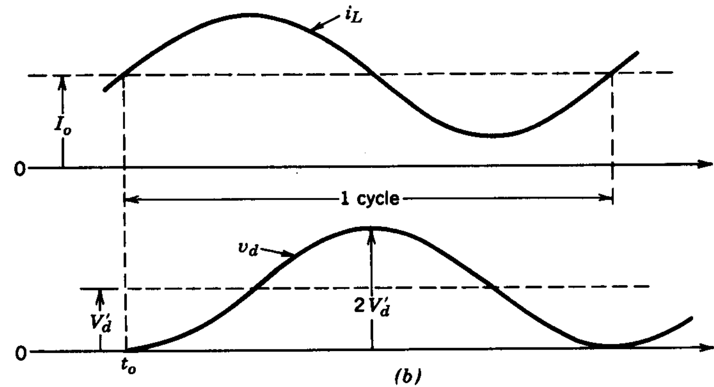
Resonant DC-Link Inverter





• The dc-link voltage is made to oscillate

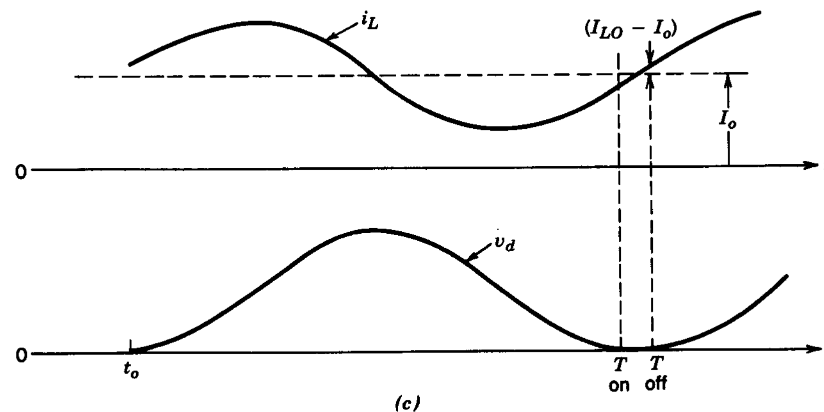


Figure 9-40 Resonant-dc-link inverter, basic concept: (*a*) basic circuit; (*b*) lossless $R_l = 0$; (*c*) losses are present.

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Three-Phase Resonant DC-Link Inverter

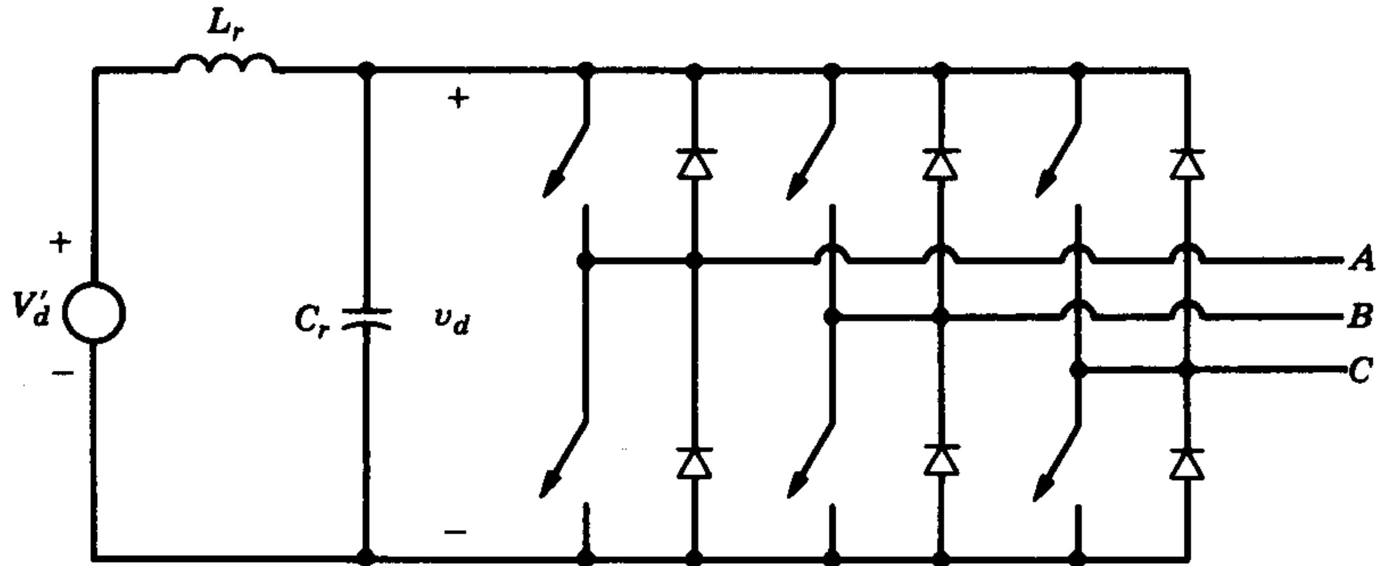

Figure 9-41 Three-phase resonant-dc-link inverter.

- Modifications have been proposed

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High-Frequency-Link Inverter

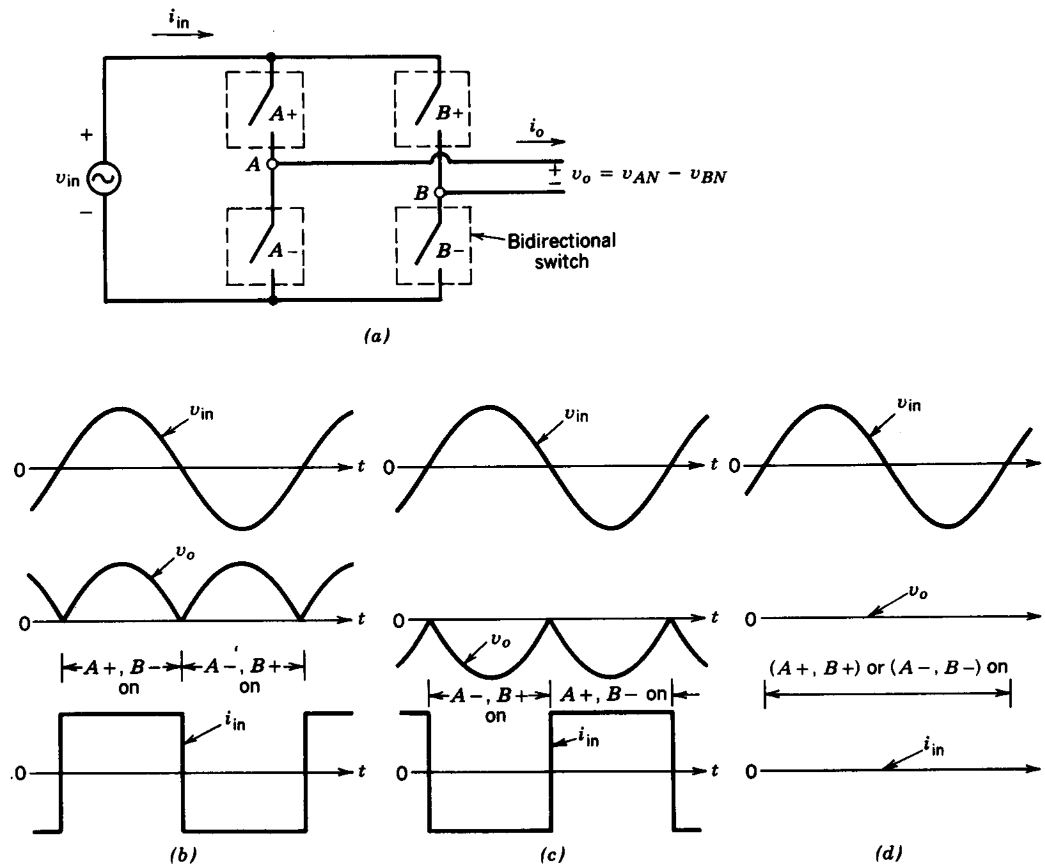

Figure 9-42 High-frequency-link integral-half-cycle inverter.

- Basic principle for selecting integral half-cycles of the high-frequency ac input

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High-Frequency-Link Inverter

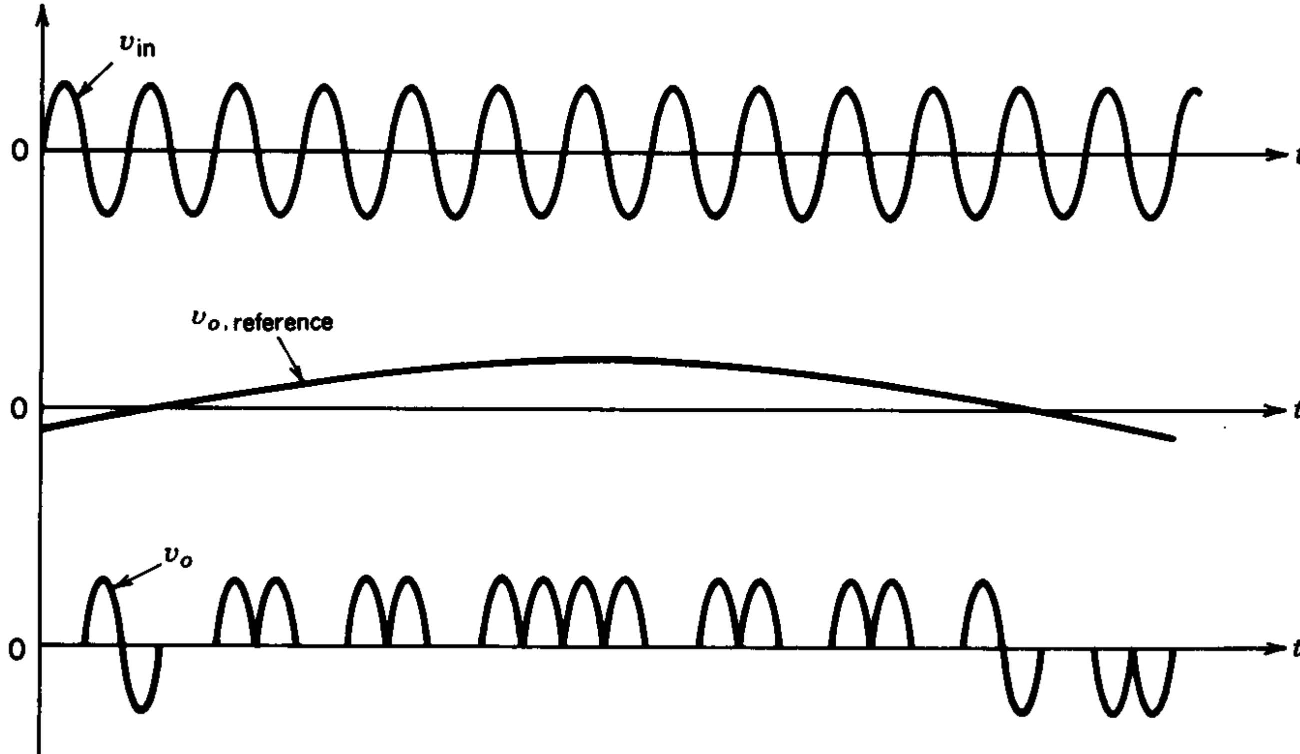

Figure 9-43 Synthesis of low-frequency ac output.

- Low-frequency ac output is synthesized by selecting integral half-cycles of the high-frequency ac input

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High-Frequency-Link Inverter

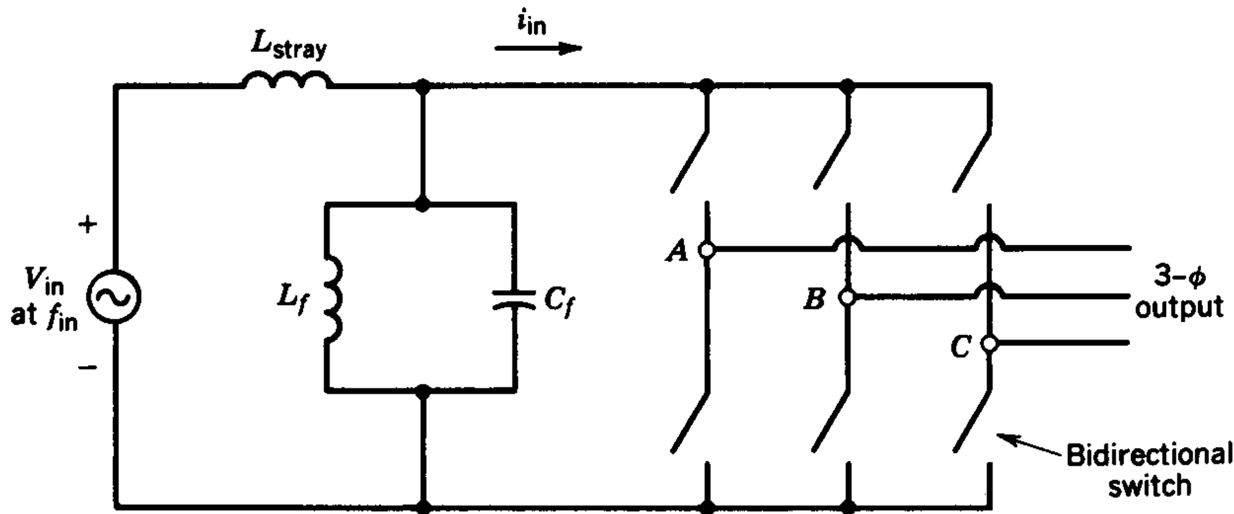

Figure 9-44 High-frequency ac to low-frequency three-phase ac converter.

- Shows how to implement such an inverter

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Chapter 10

Switching DC Power Supplies

Chapter 10 Switching dc Power Supplies **301**

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- One of the most important applications of power electronics

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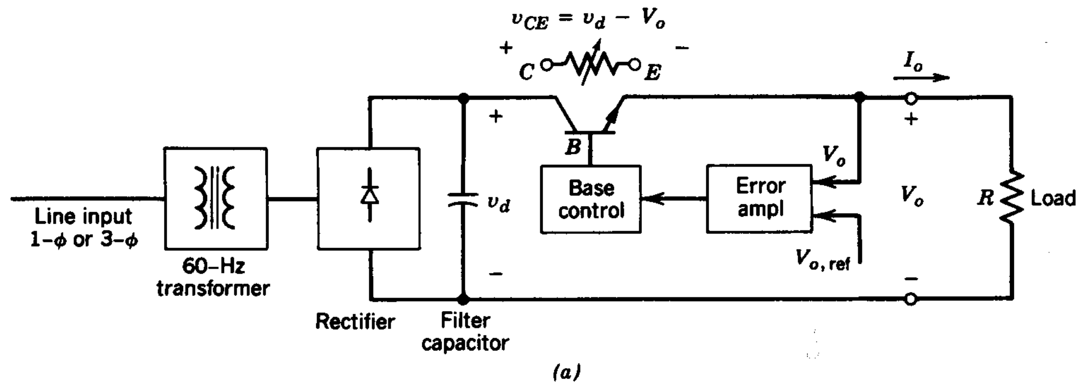
Linear Power Supplies



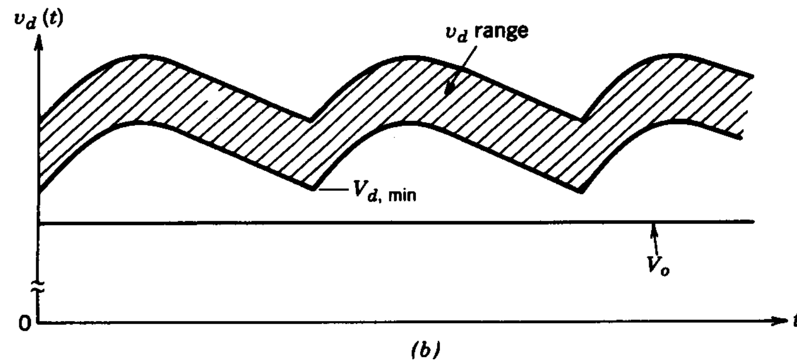


Figure 10-1 Linear power supply: (*a*) schematic; (*b*) selection of transformer turns ratio so that $V_{d,\min} > V_o$ by a small margin.

- Very poor efficiency and large weight and size

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Switching DC Power Supply: Block Diagram

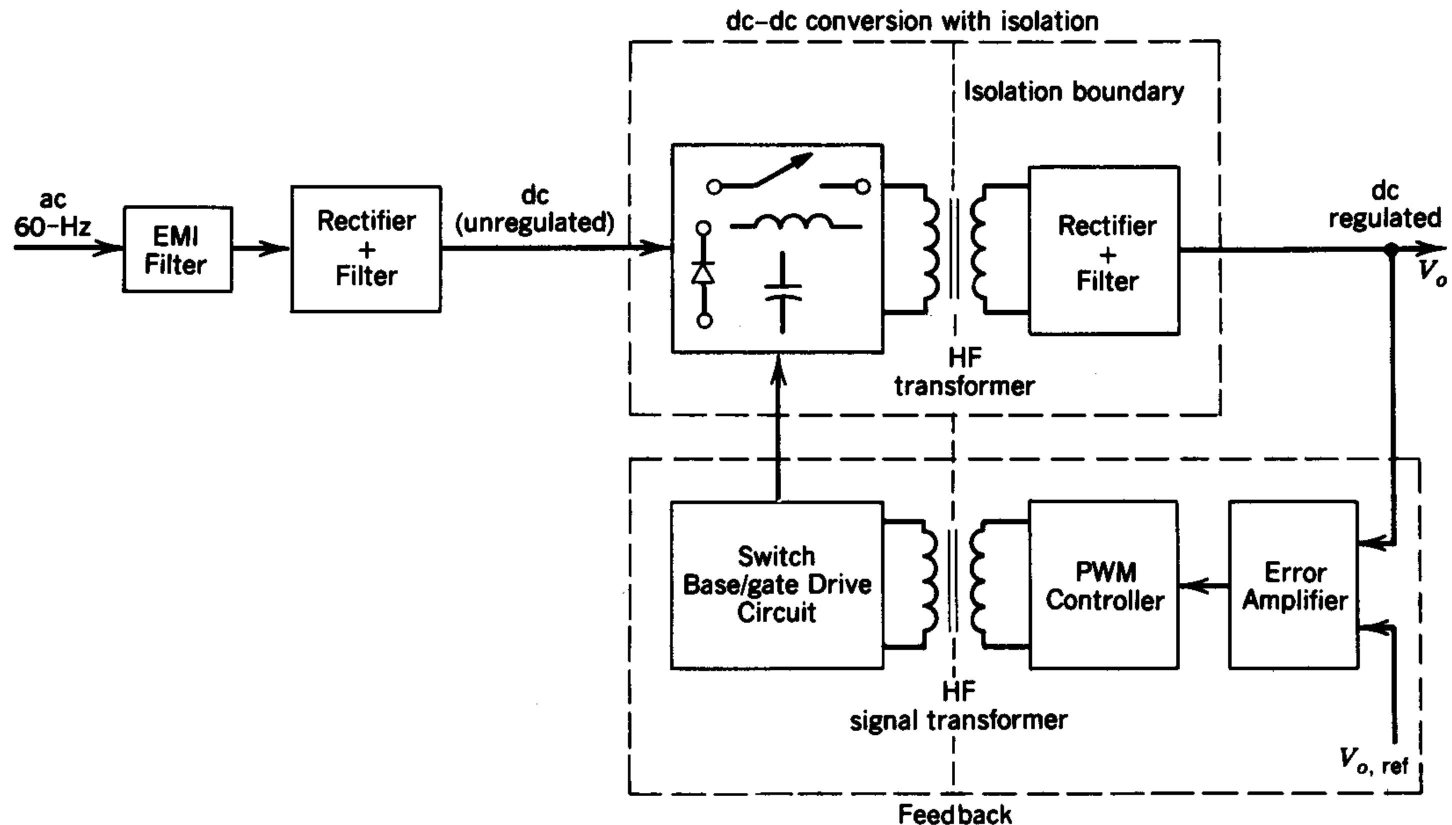

Figure 10-2 Schematic of a switch-mode dc power supply.

- High efficiency and small weight and size

Switching DC Power Supply: Multiple Outputs

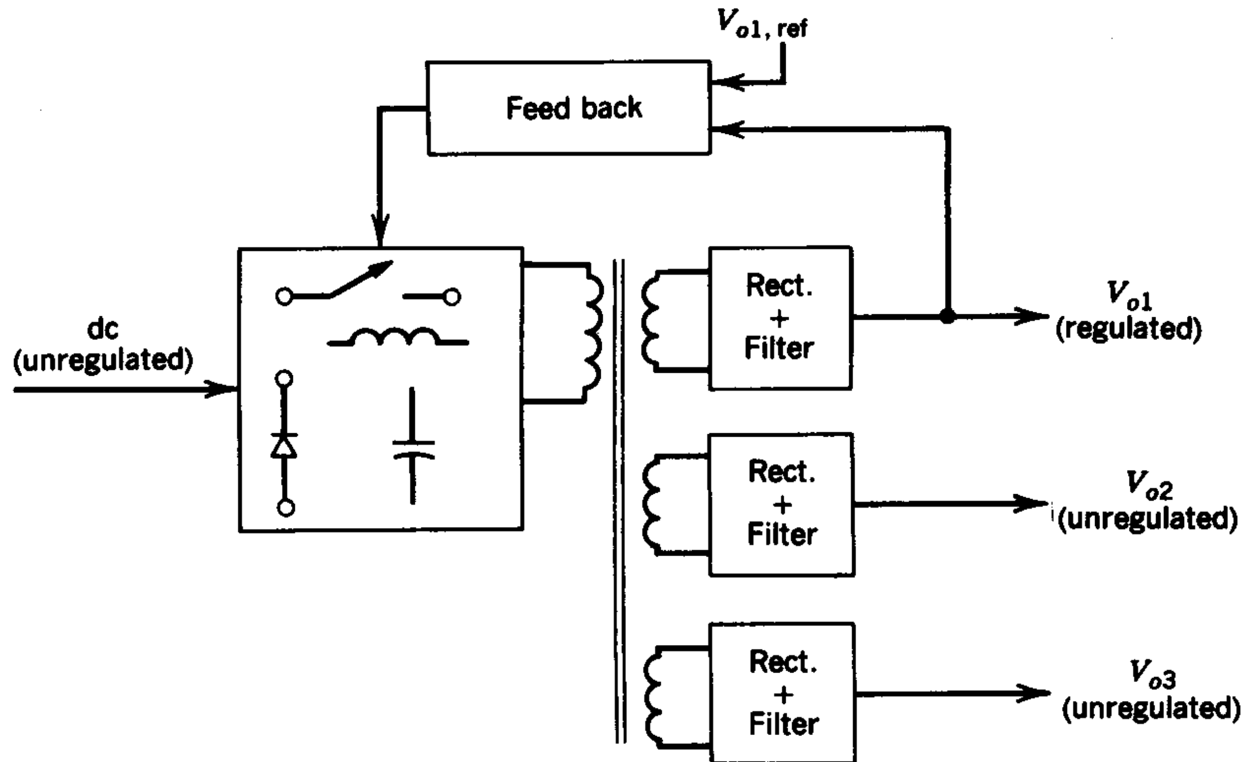

Figure 10-3 Multiple outputs.

- In most applications, several dc voltages are required, possibly electrically isolated from each other

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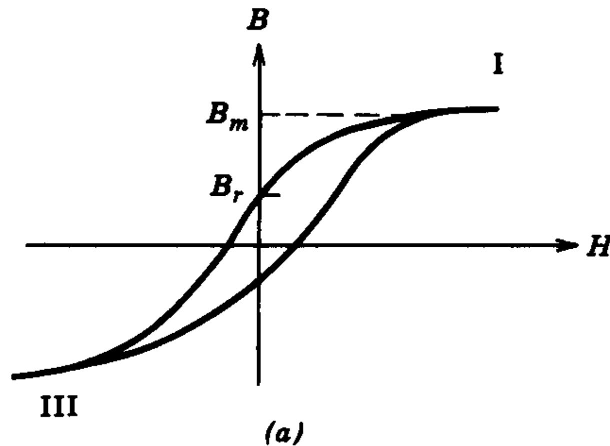
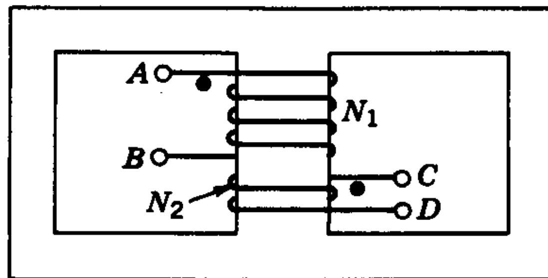
Transformer Analysis





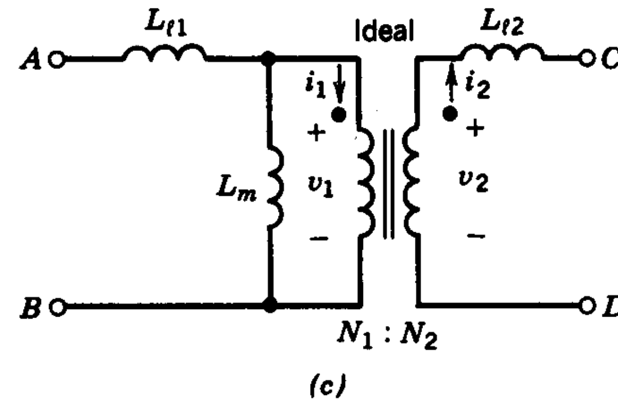


Figure 10-4 Transformer representation: (*a*) typical *B–H* loop of transformer core; (*b*) two-winding transformer; (*c*) equivalent circuit.

- Needed to discuss high-frequency isolated supplies

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PWM to Regulate Output

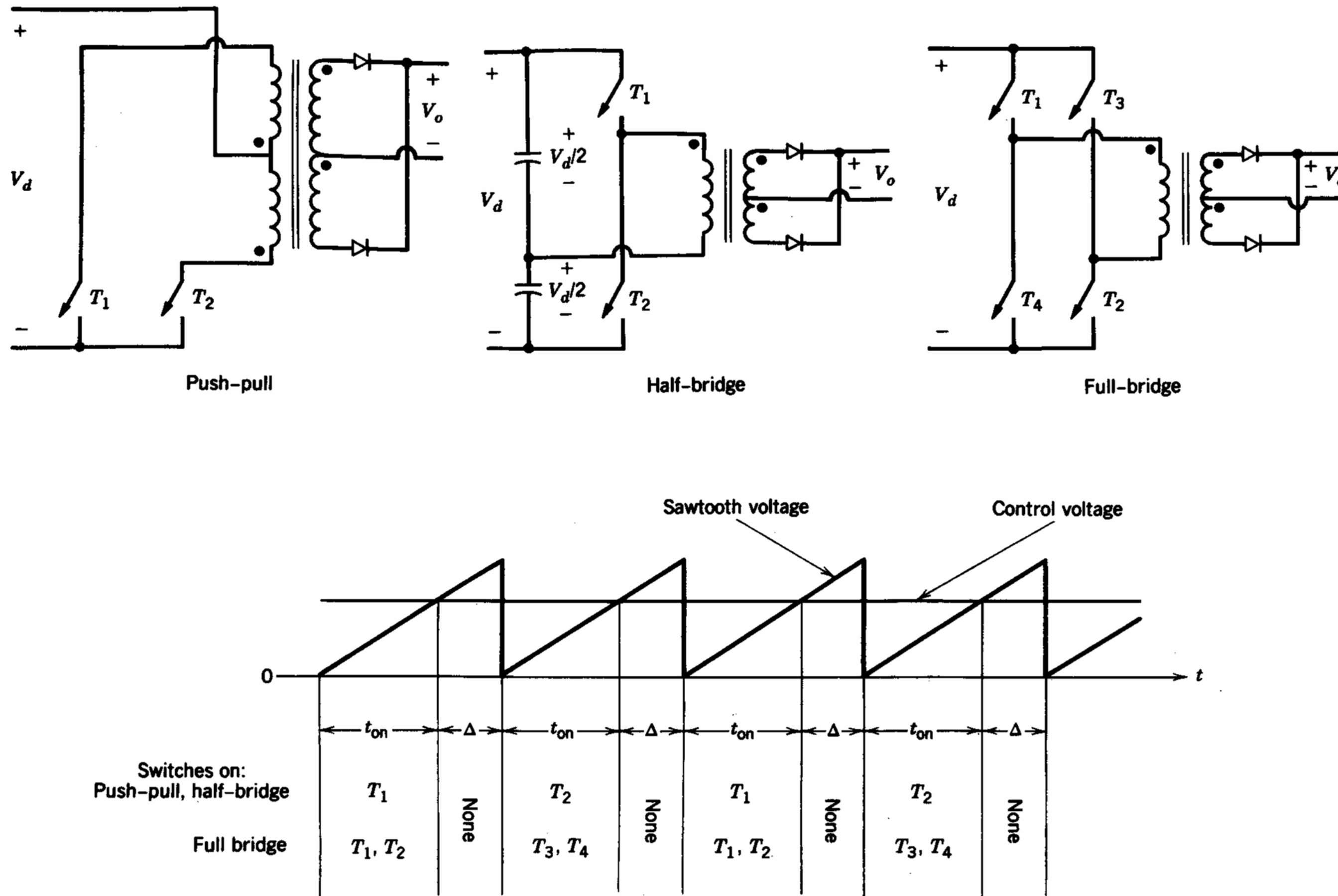

Figure 10-5 PWM Scheme used in dc–dc converters, where the converter output is rectified to produce a dc output.

- Basic principle is the same as discussed in Chapter 8

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Flyback Converter

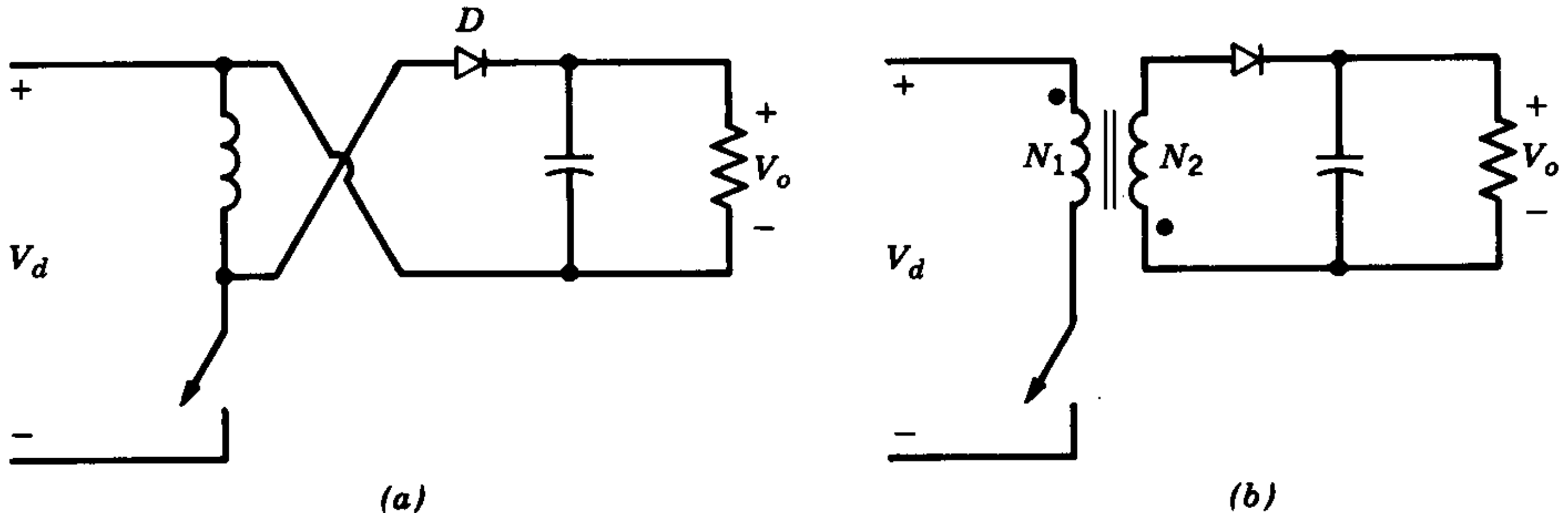

Figure 10-6 Flyback converter.

- Derived from buck-boost; very power at small power (> 50 *W*) power levels

Flyback Converter

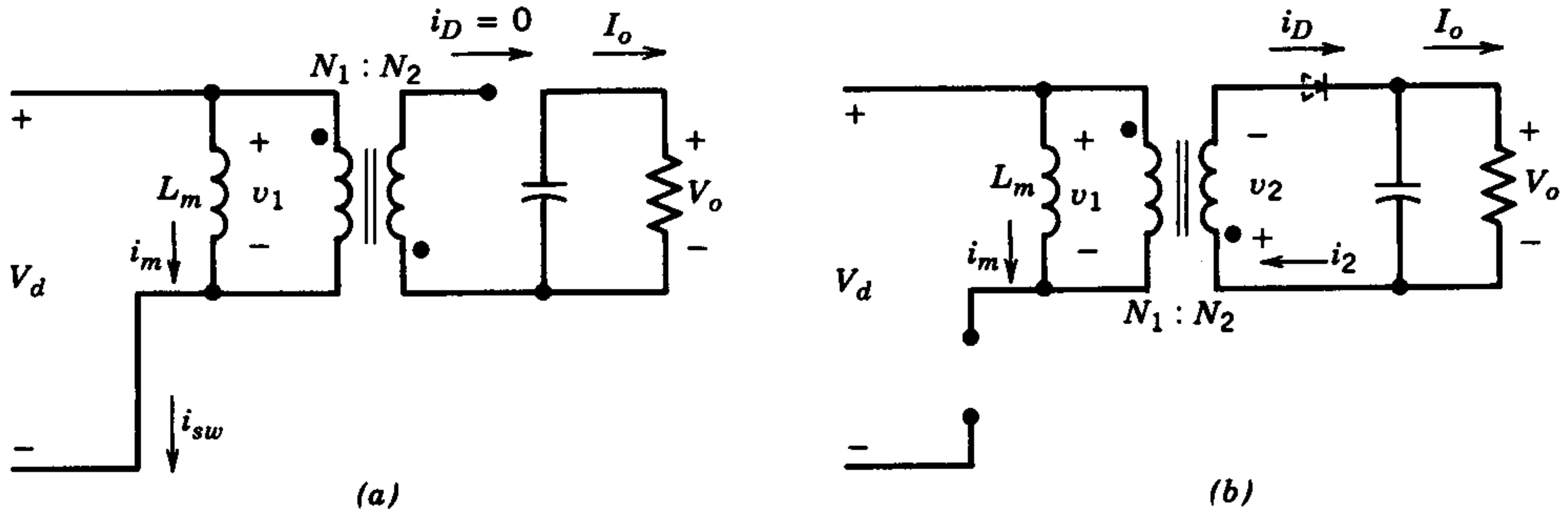

Figure 10-7 Flyback converter circuit states: (*a*) switch on; (*b*) switch off.

- Switch on and off states (assuming incomplete core demagnetization)

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Flyback Converter

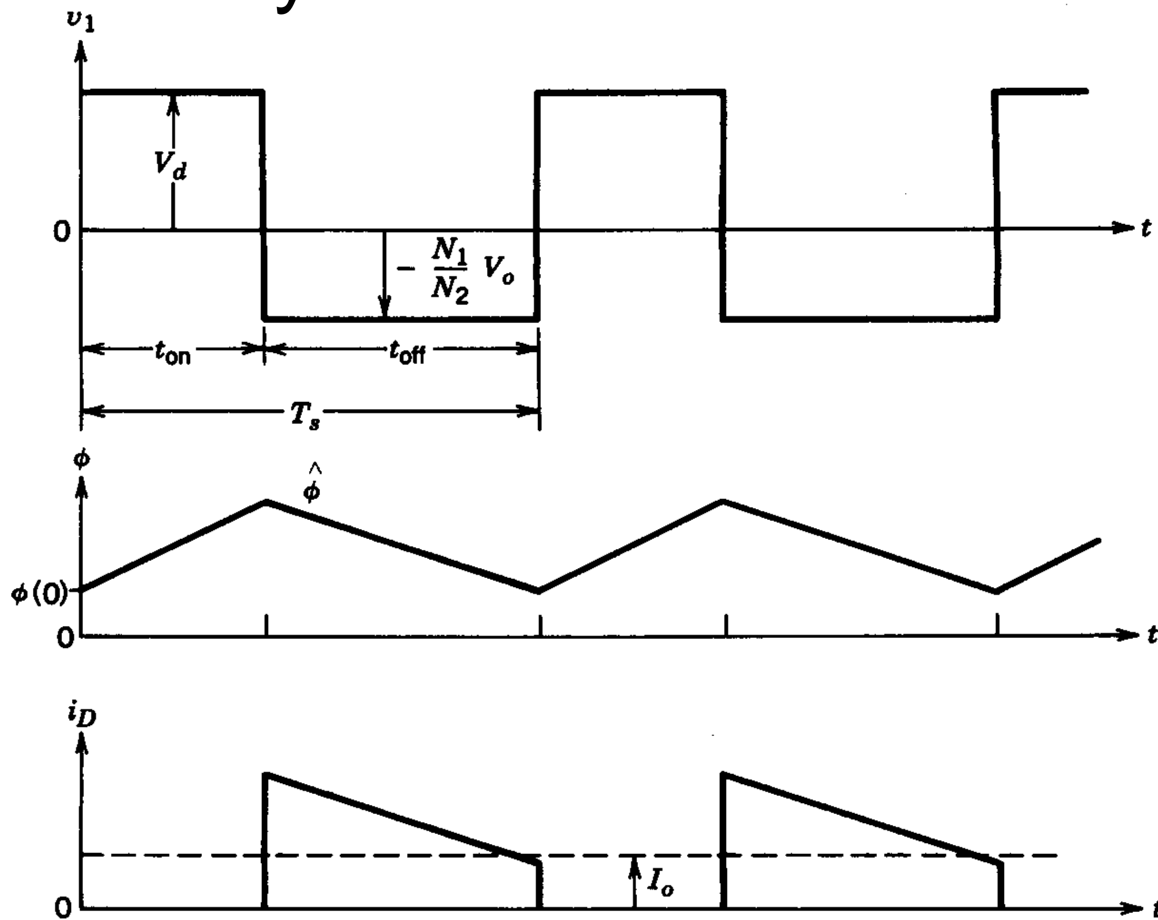

Figure 10-8 Flyback converter waveforms.

- Switching waveforms (assuming incomplete core demagnetization)

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Other Flyback Converter Topologies

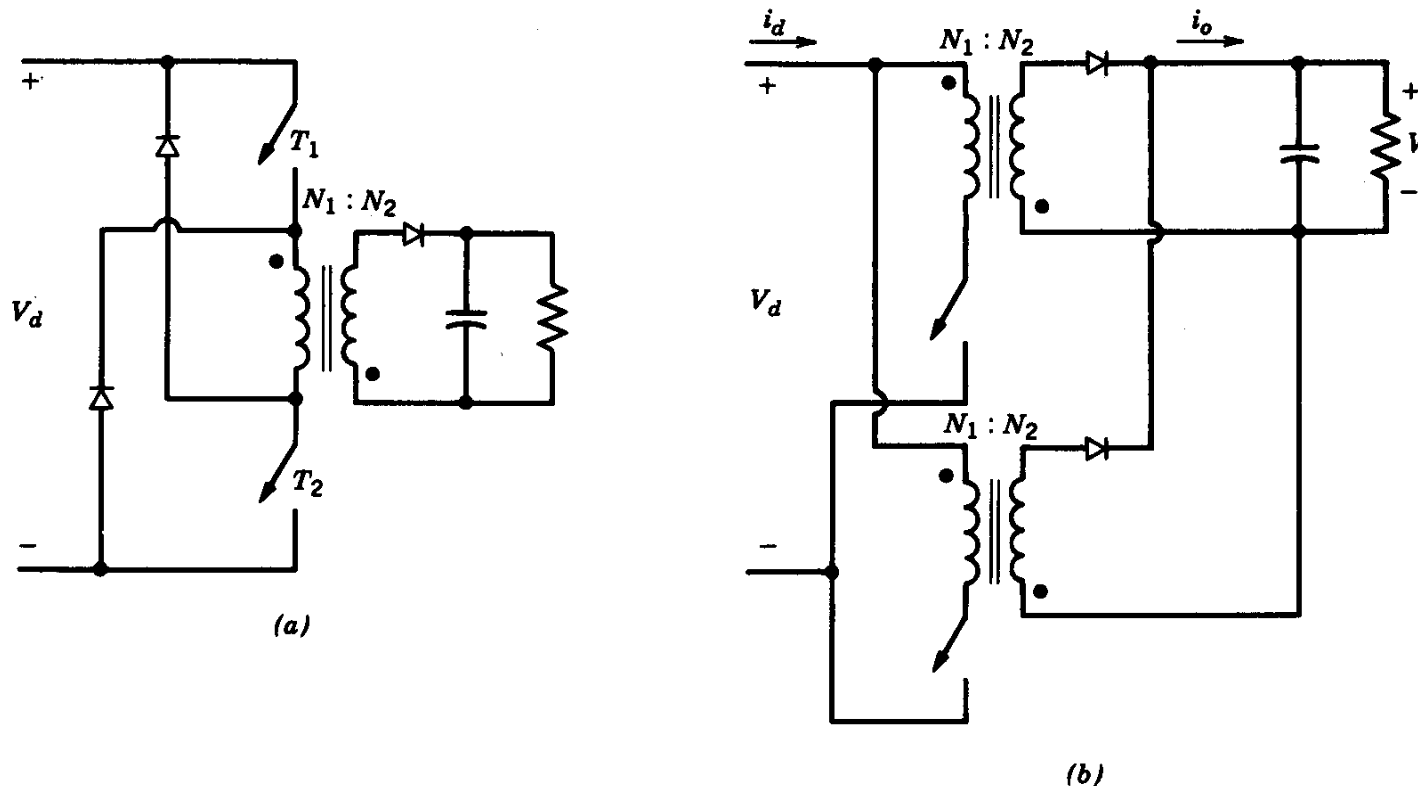

Figure 10-9 Other flyback topologies: (*a*) two-transistor flyback converter; (*b*) parallelled flyback converters.

- Not commonly used

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Forward Converter

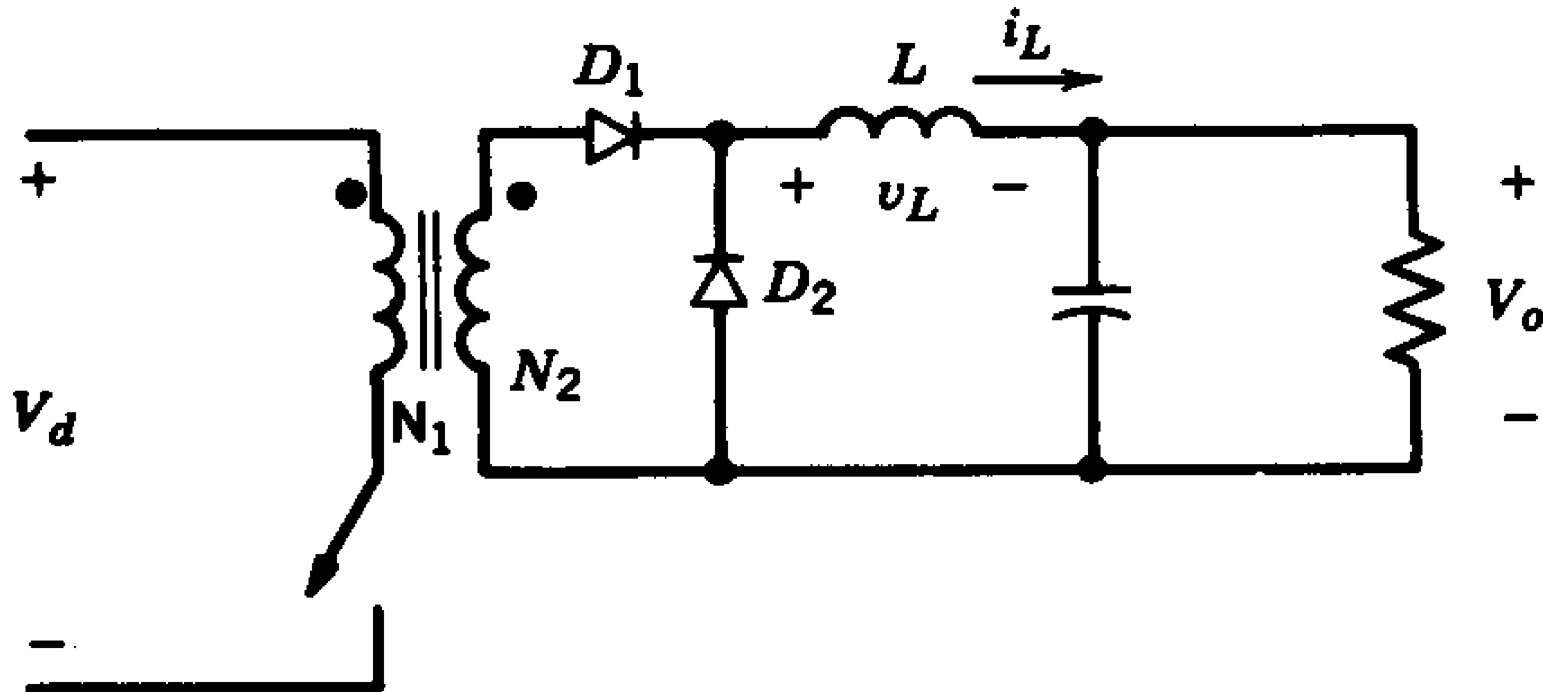

Figure 10-10 Idealized forward converter.

- Derived from Buck; idealized to assume that the transformer is ideal (not possible in practice)

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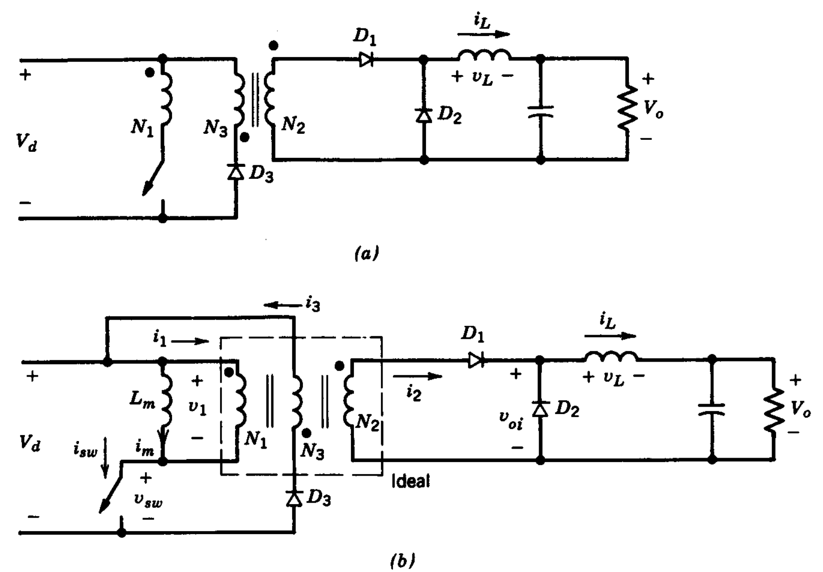
Forward Converter: in Practice



- Switching waveforms (assuming incomplete core demagnetization)

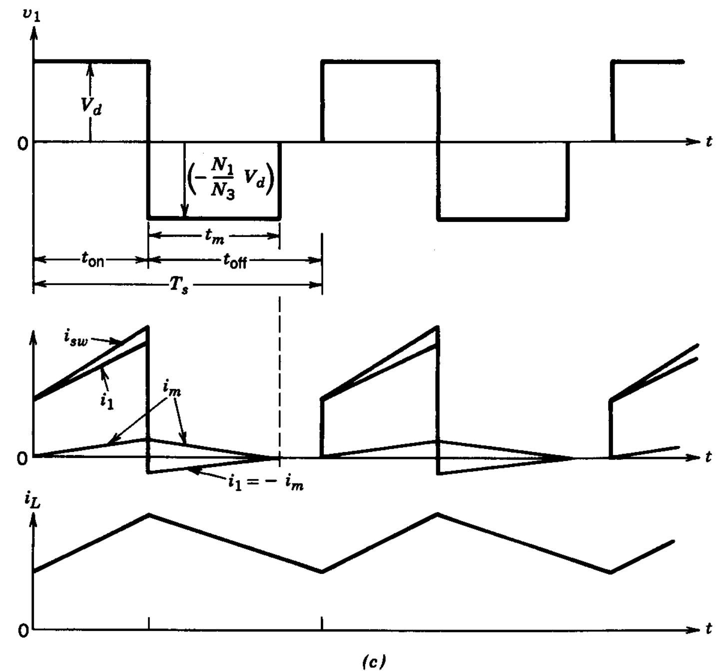


Figure 10-11 Practical forward converter.

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Forward Converter: Other Possible Topologies

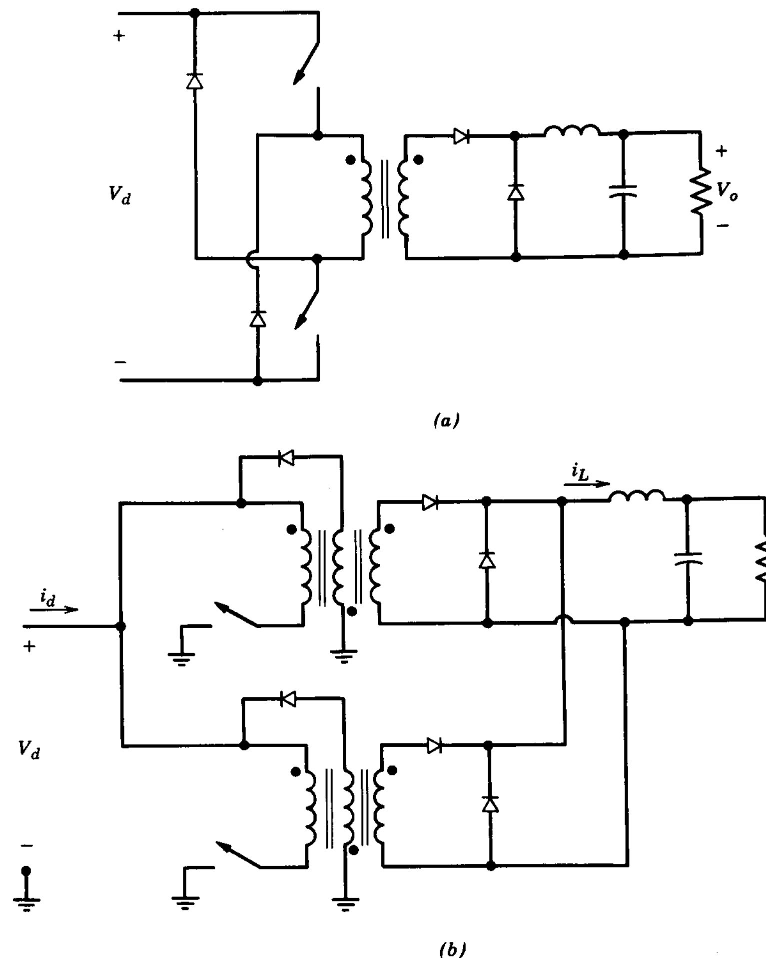

Figure 10-12 Other topologies of forward converter: (*a*) two-switch forward converter; (*b*) parallelled forward converters.

- Two-switch Forward converter is very commonly used

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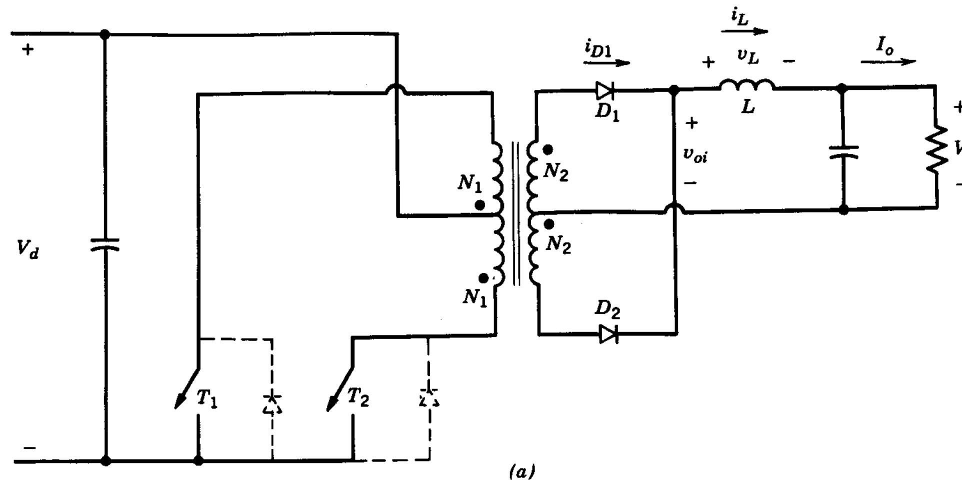
Push-Pull Inverter



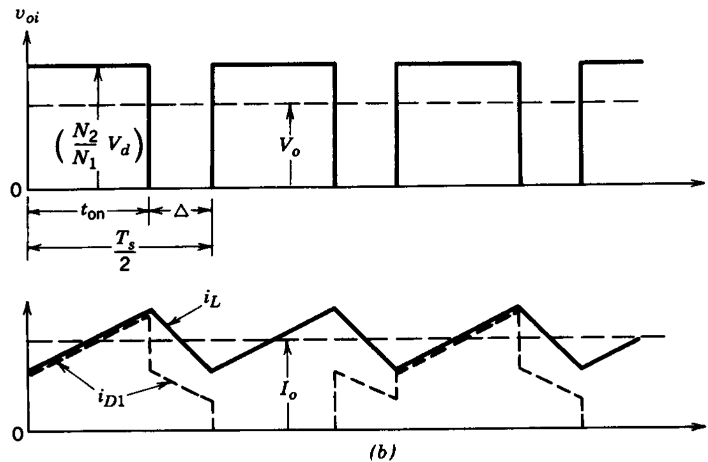


Figure 10-13 Push–pull converter.

- Leakage inductances become a problem

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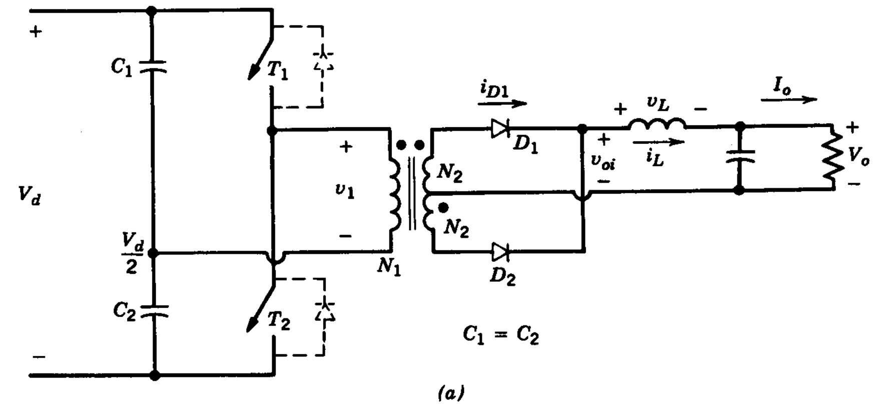
Half-Bridge Converter



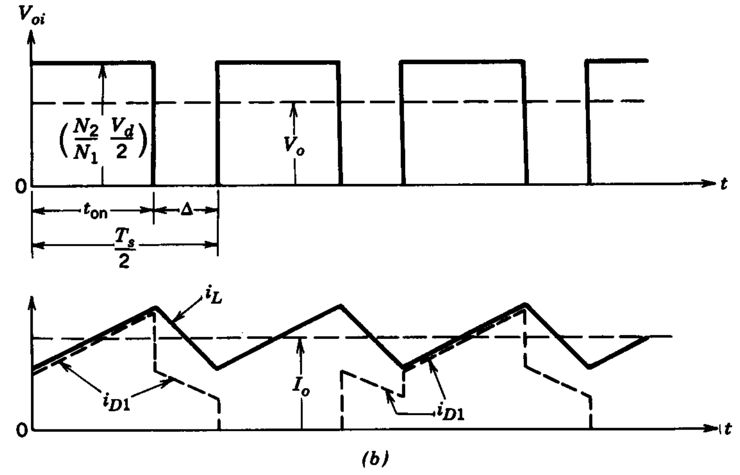


Figure 10-14 Half-bridge dc–dc converter.

- Derived from Buck

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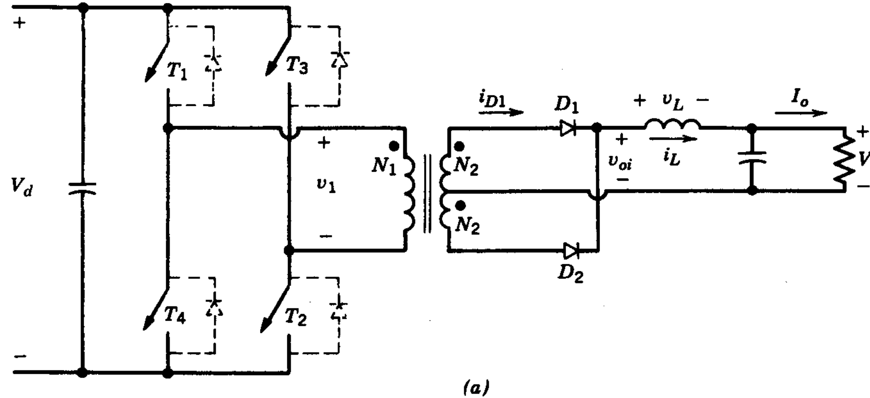
Full-Bridge Converter



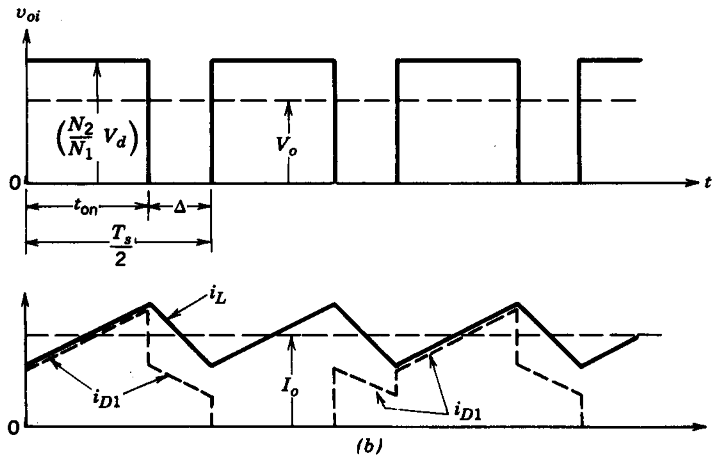


Figure 10-15 Full-bridge converter.

- Used at higher power levels (> 0.5 *kW*)

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Current-Source Converter

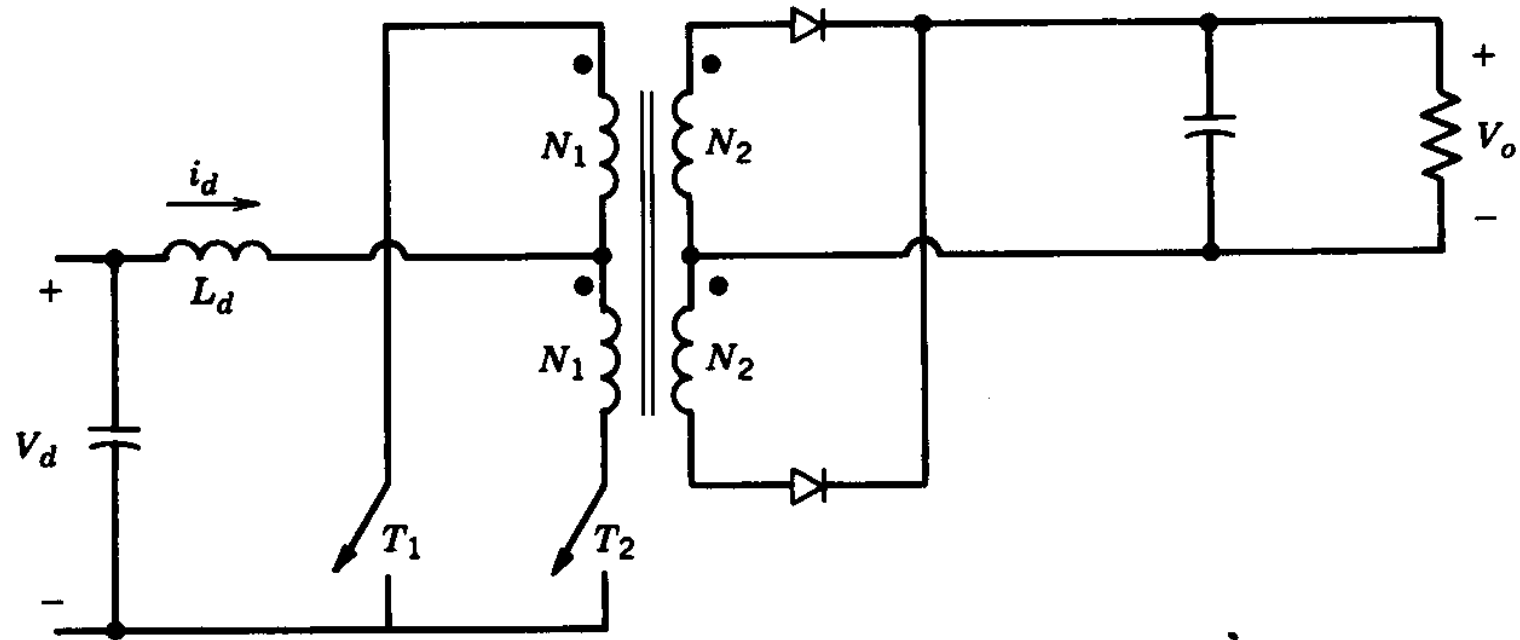

Figure 10-16 Current source converter ($D > 0.5$).

- More rugged (no shoot-through) but both switches must not be open simultaneously

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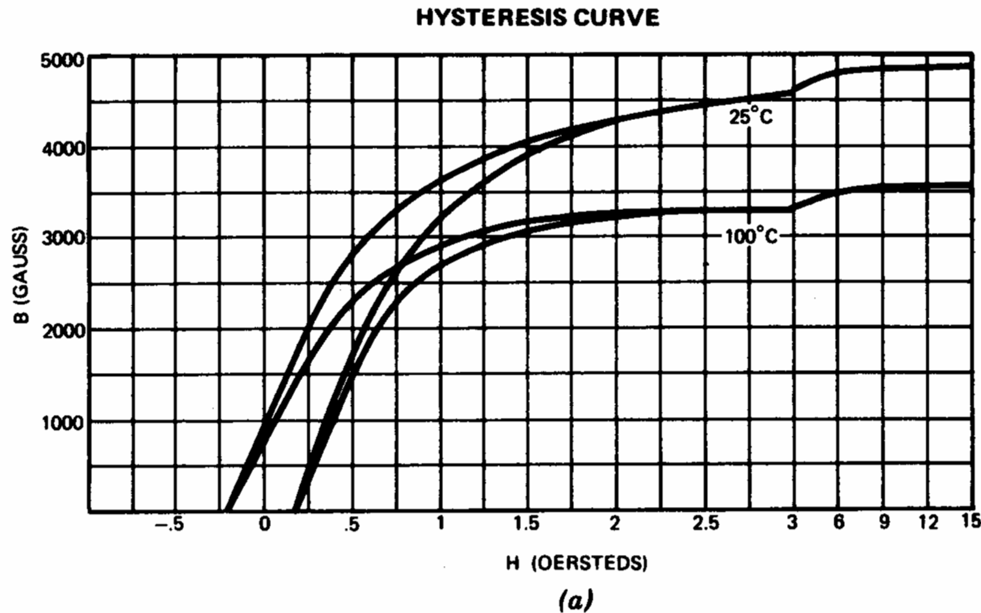
Ferrite Core Material



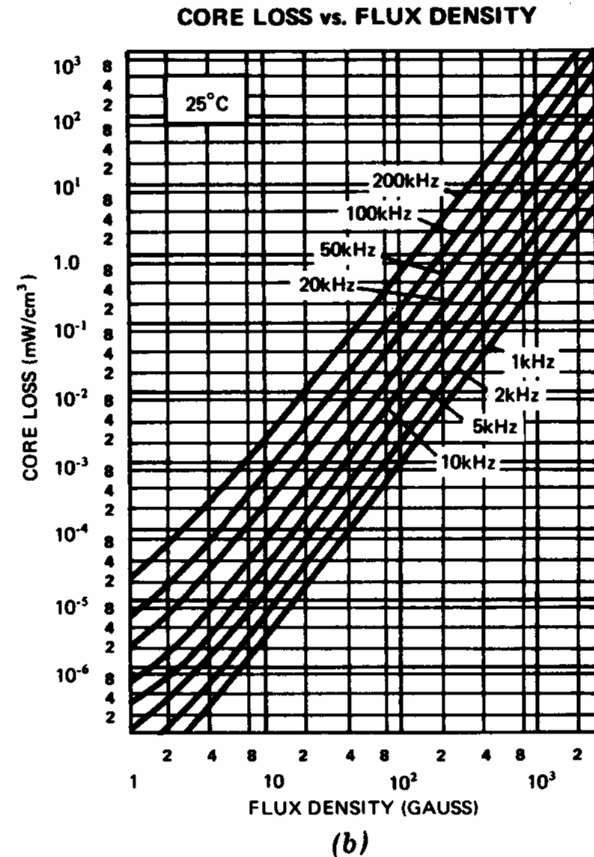


Figure 10-17 3C8 ferrite characteristic curves: (*a*) B−H loop; (*b*) core loss curves. (*Courtesy of Ferroxcube Division of Amperex Electronic Corporation.*)

- Several materials to choose from based on applications

Core Utilization in Various Converter Topologies

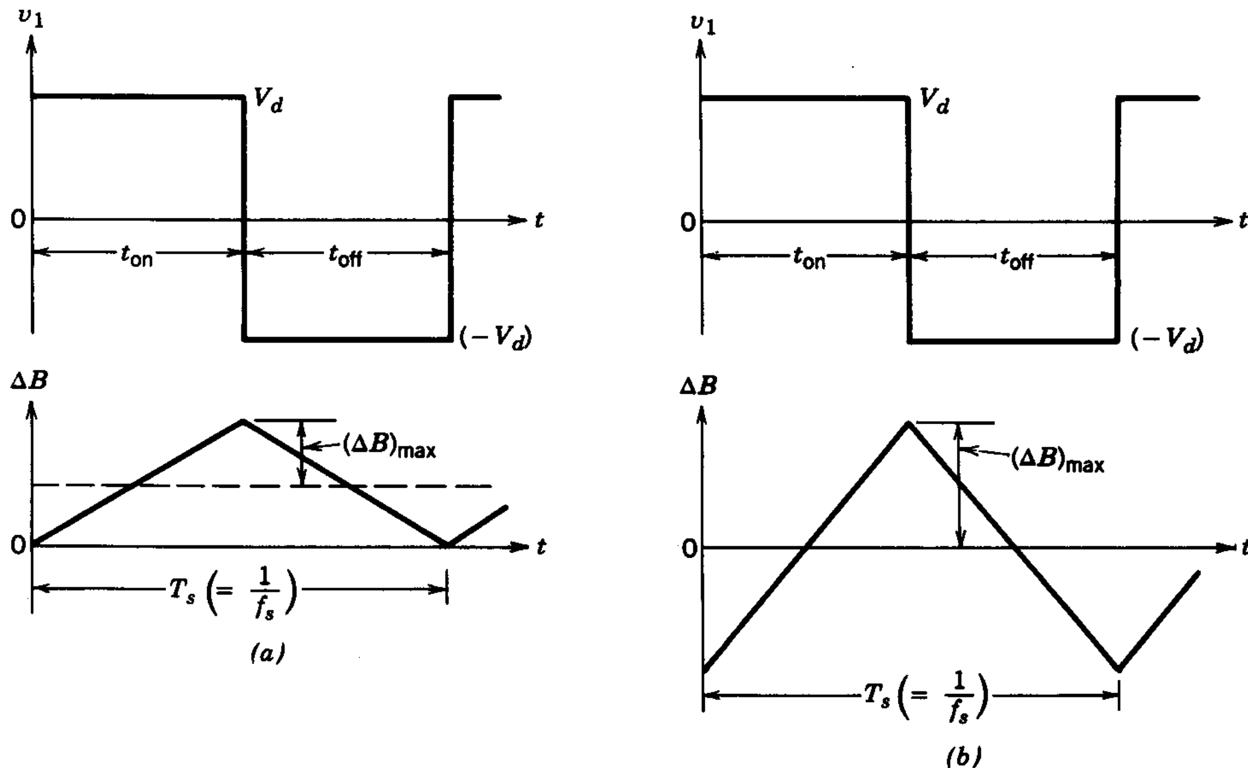


Figure 10-18 Core excitation: (*a*) forward converter, $D = 0.5$; (*b*) full-bridge converter, $D = 0.5$.

- At high switching frequencies, core losses limit excursion of flux density

Control to Regulate Voltage Output

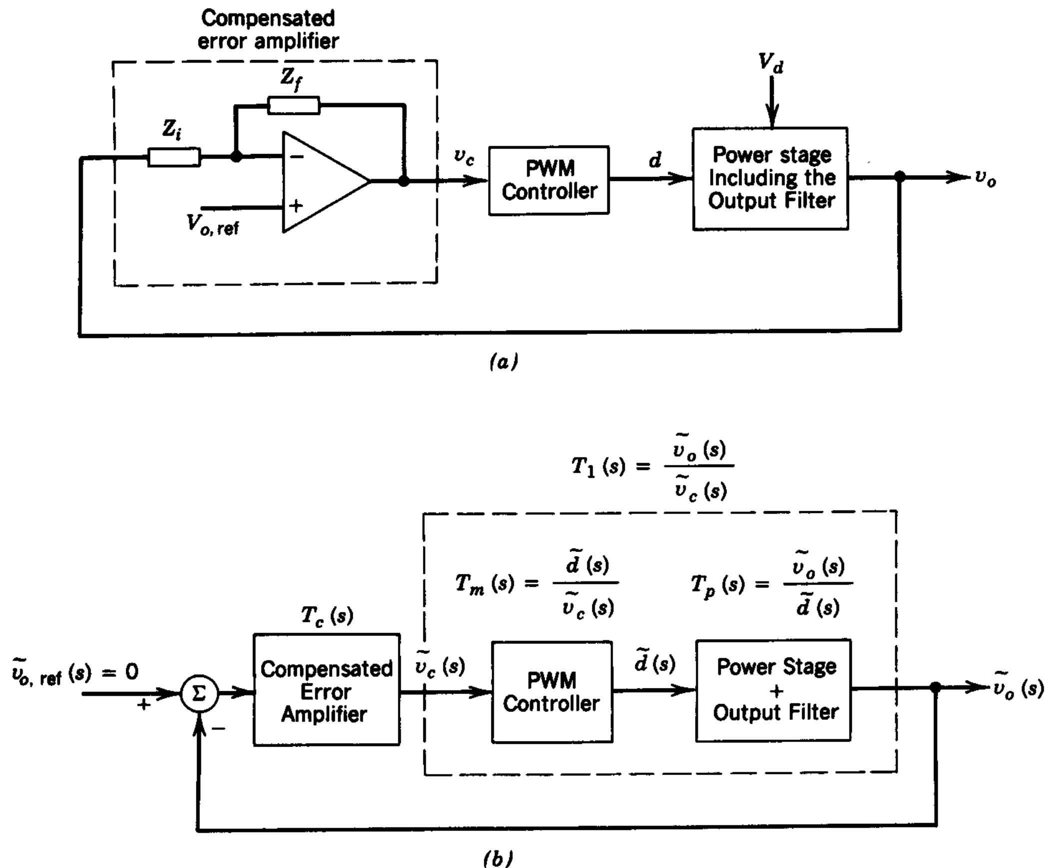


Figure 10-19 Voltage regulation: (*a*) feedback control system; (*b*) linearized feedback control system.

- Linearized representation of the feedback control system

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Forward Converter: An Example

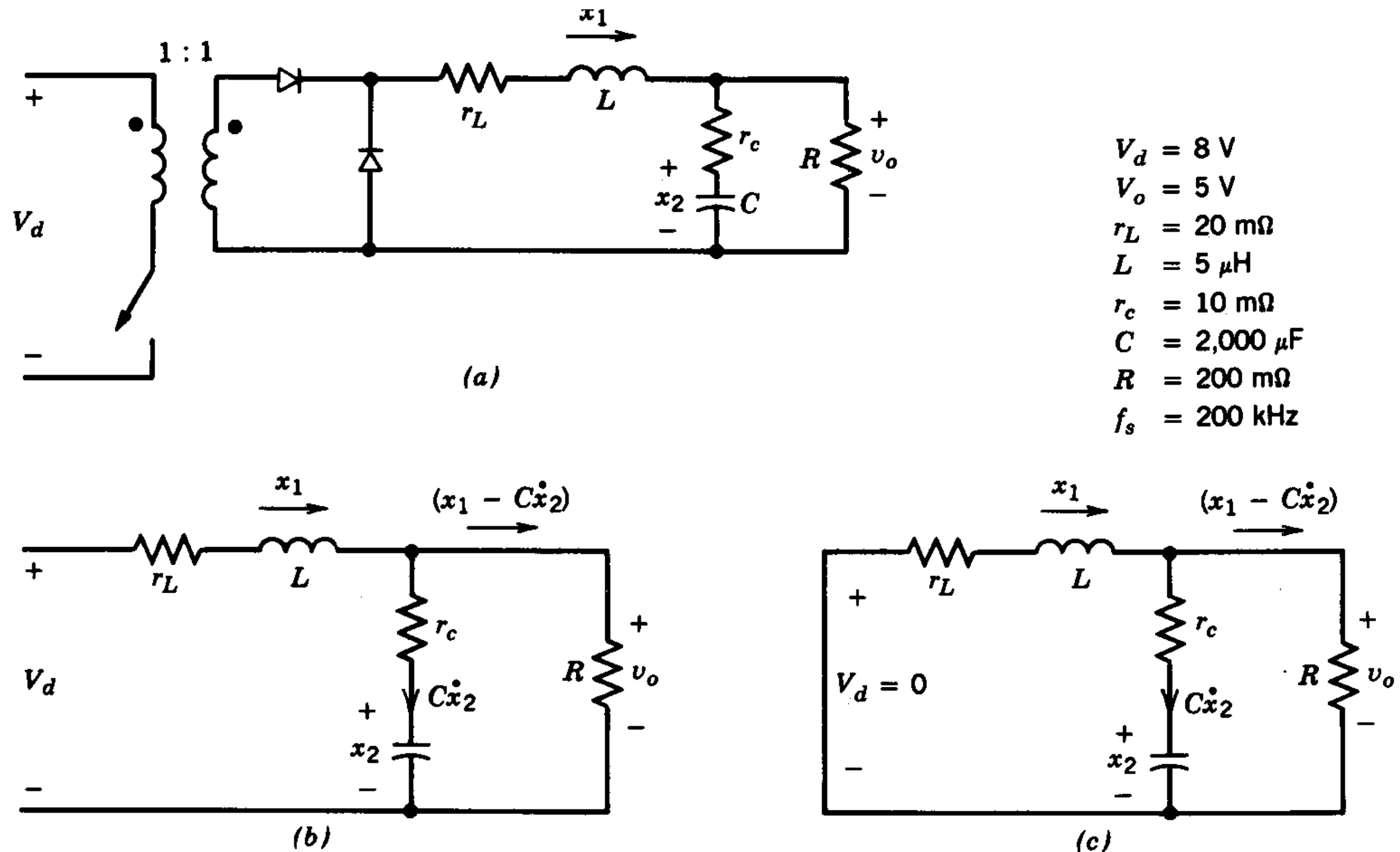

Figure 10-20 Forward converter: (*a*) circuit; (*b*) switch on; (*c*) switch off.

- The switch and the diode are assumed to be ideal

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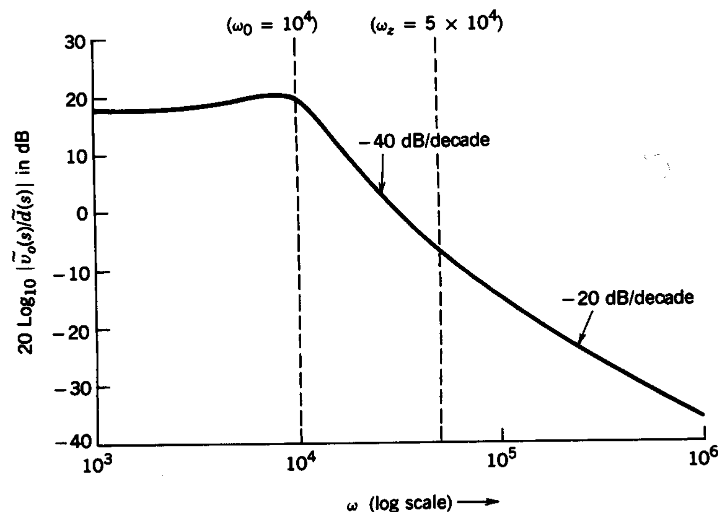
Forward Converter:Transfer Function Plots

- Example considered earlier



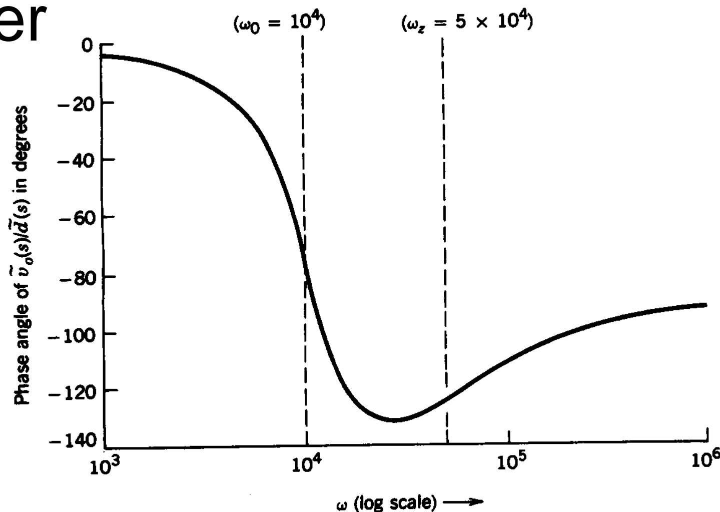


Figure 10-21 (*a*) Gain plot of the forward converter in Fig. 10-20*a*. (*b*) Phase plot of the forward converter in Fig. 10-20*a*.

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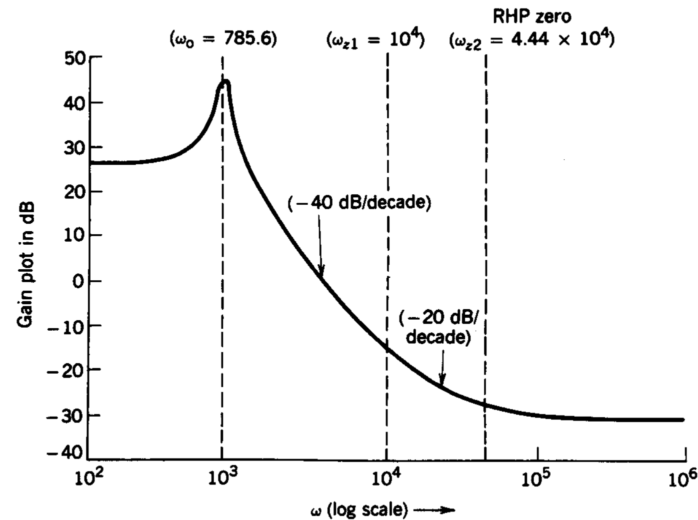
Flyback Converter:Transfer Function Plots

- An example



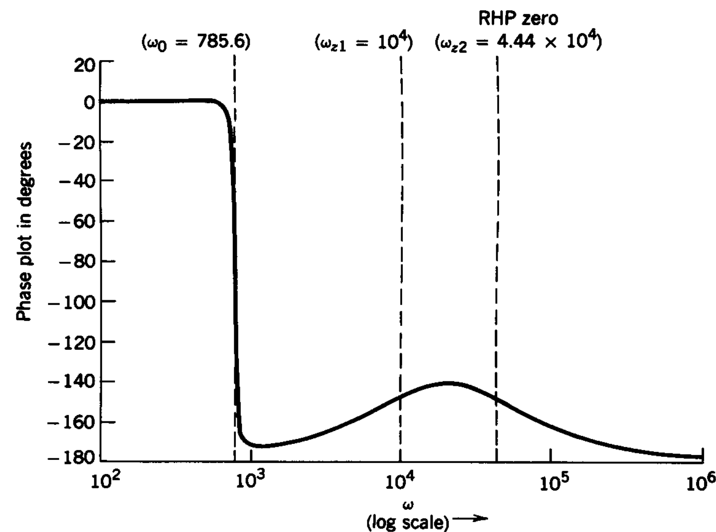


Figure 10-22 (*a*) Gain plot for a flyback converter. (*b*) Phase plot for a flyback converter.

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Linearizing the PWM Block

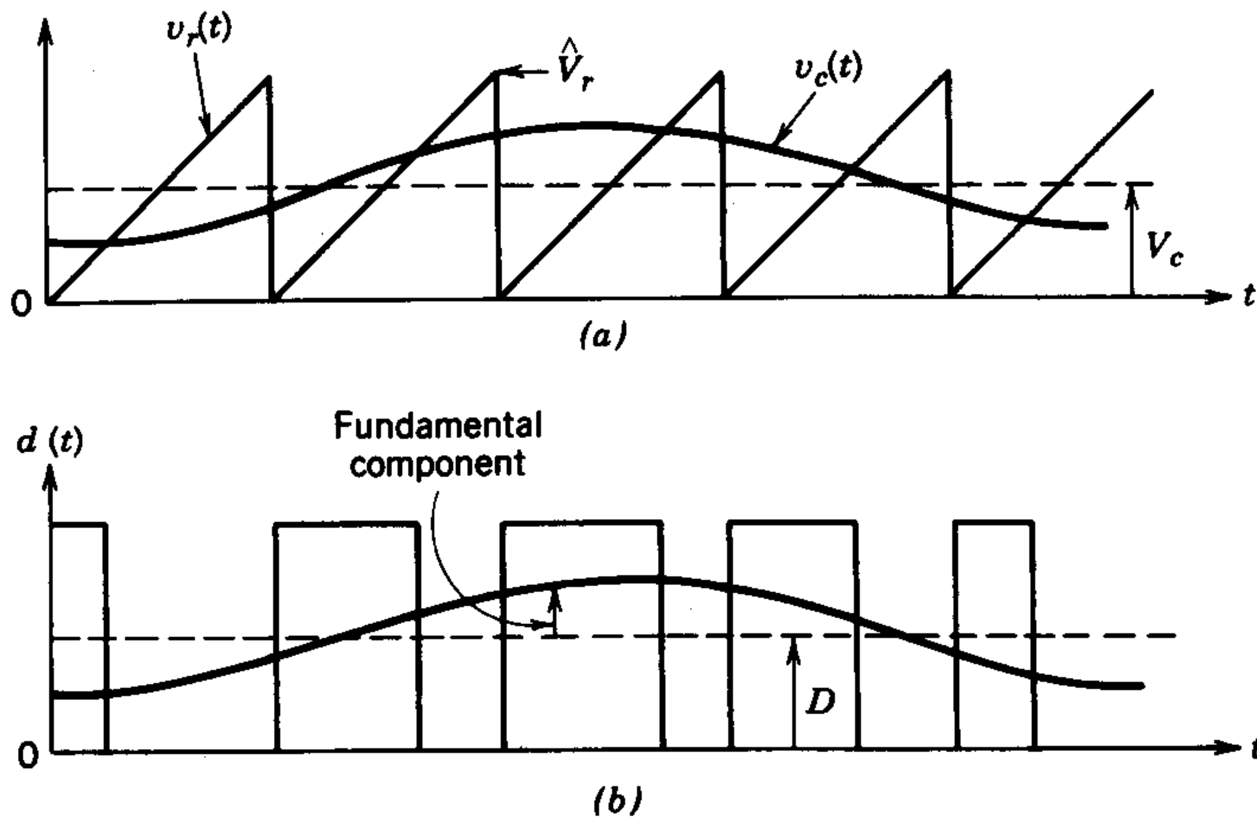

Figure 10-23 Pulse-width modulator.

- The transfer function is essentially a constant with zero phase shift

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Gain of the PWM IC

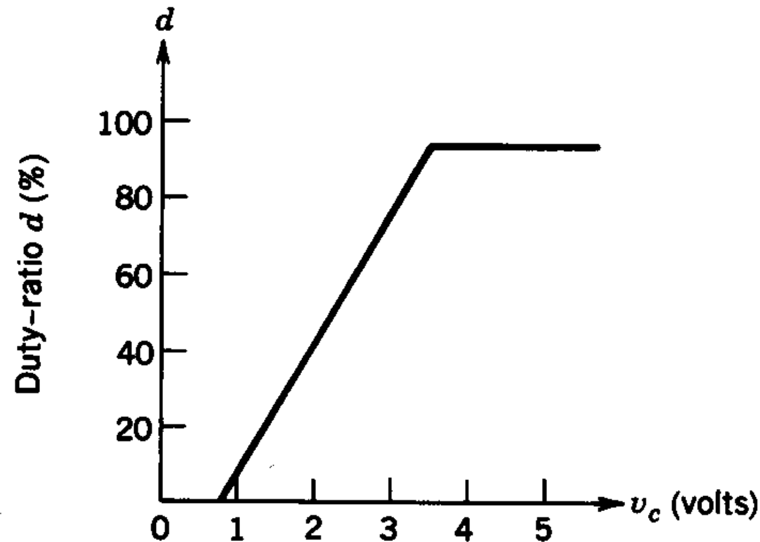

Figure 10-24 Pulse-width modulator transfer function.

- It is slope of the characteristic

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Typical Gain and Phase Plots of the Open-Loop Transfer Function

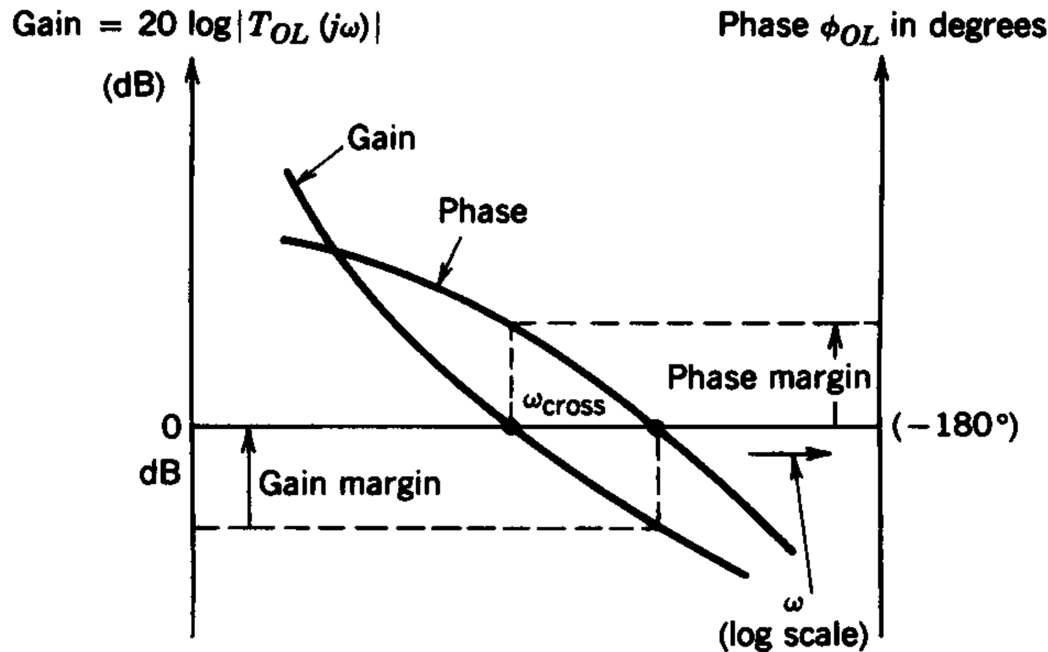

Figure 10-25 Gain and phase margins.

• Definitions of the crossover frequency, phase and gain margins

A General Amplifier for Error Compensation

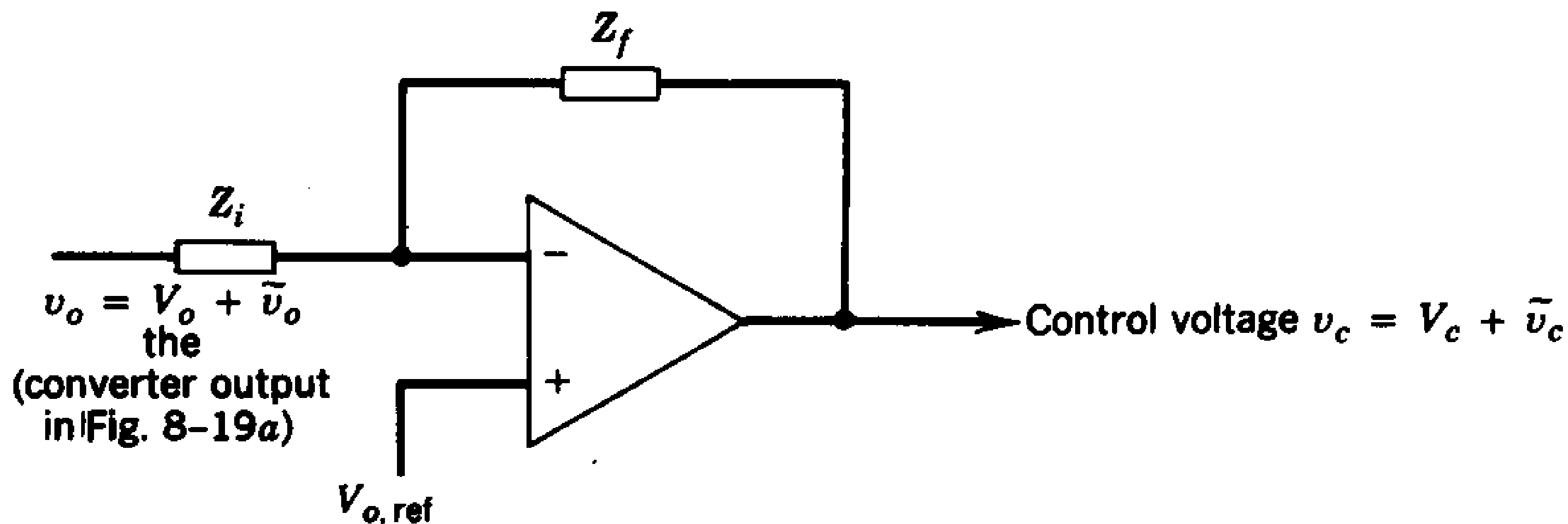

Figure 10-26 A general compensated error amplifier.

- Can be implemented using a single op-amp

Type-2 Error Amplifier

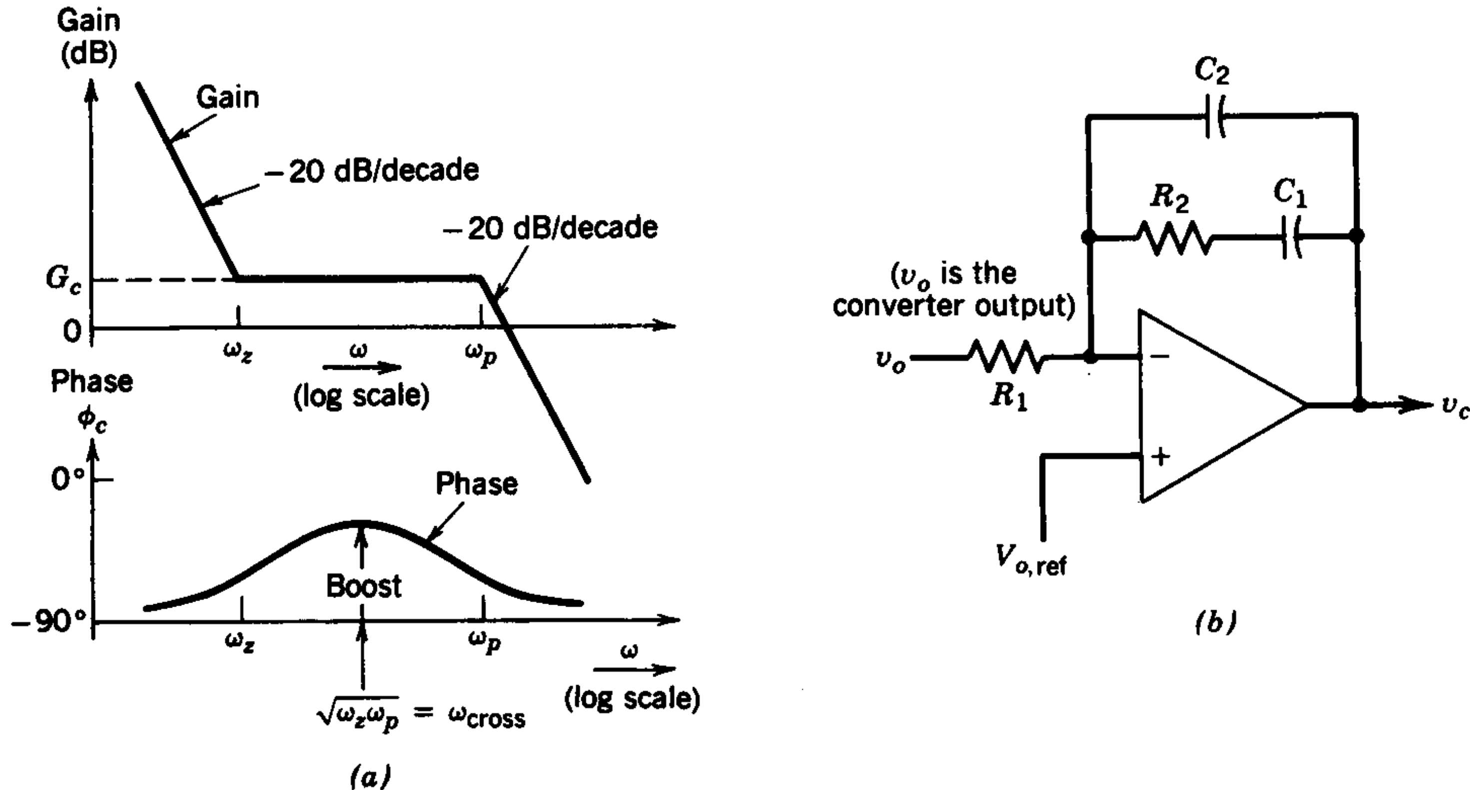

Figure 10-27 Error amplifier.

- Shows phase boost at the crossover frequency

Voltage Feed-Forward

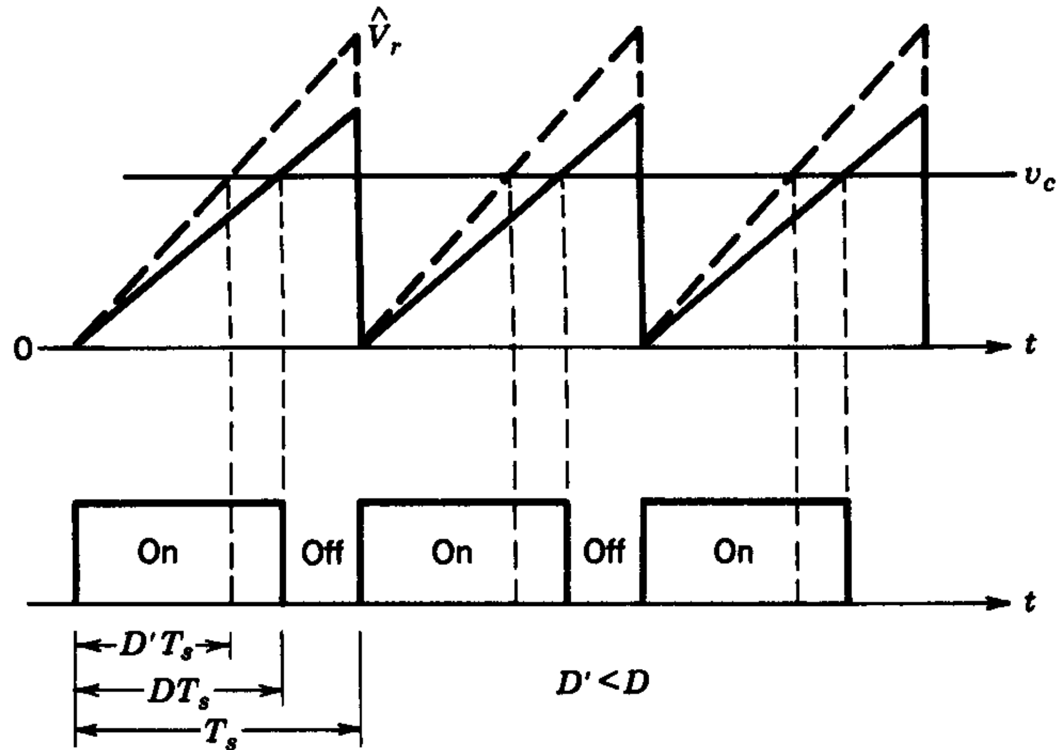

Figure 10-28 Voltage feed-forward: effect on duty ratio.

- Makes converter immune from input voltage variations

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Voltage versus Current Mode Control

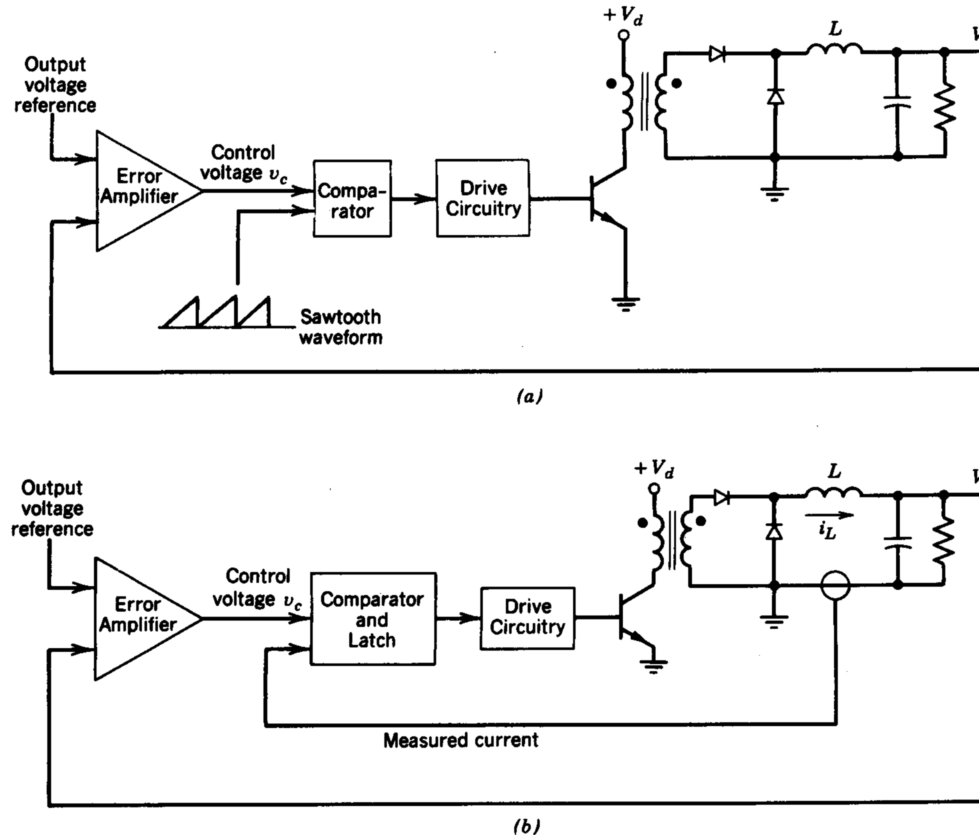

Figure 10-29 PWM duty ratio versus current-mode control: (*a*) PWM duty ratio control; (*b*) current-mode control.

- Regulating the output voltage is the objective in both modes of control

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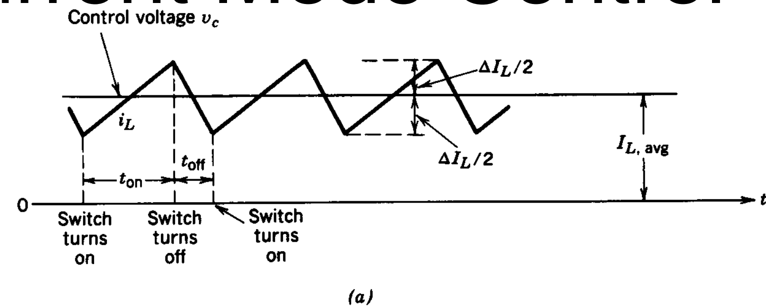
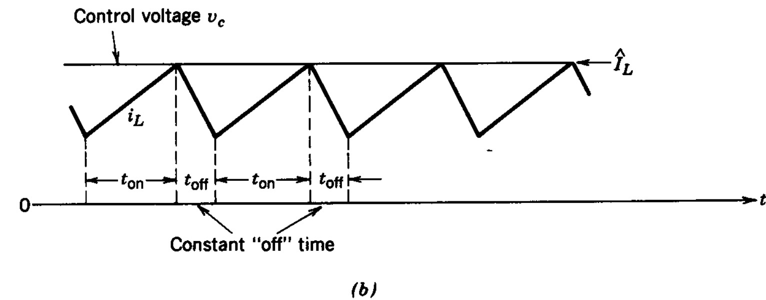
Various Types of Current Mode Control





- Constant frequency, peak-current mode control is used most frequently

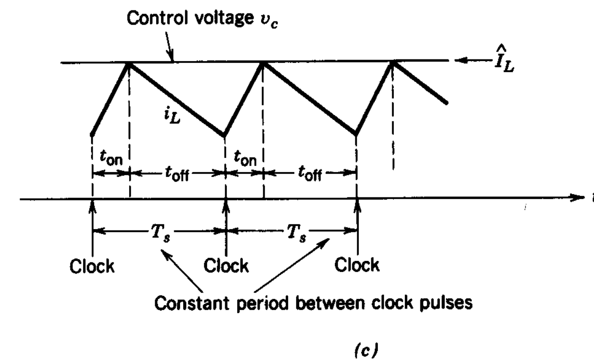


Figure 10-30 Three types of current-mode control: (*a*) tolerance band control; (*b*) constant-off-time control; (*c*) constant frequency with turn-on at clock time.

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Peak Current Mode Control

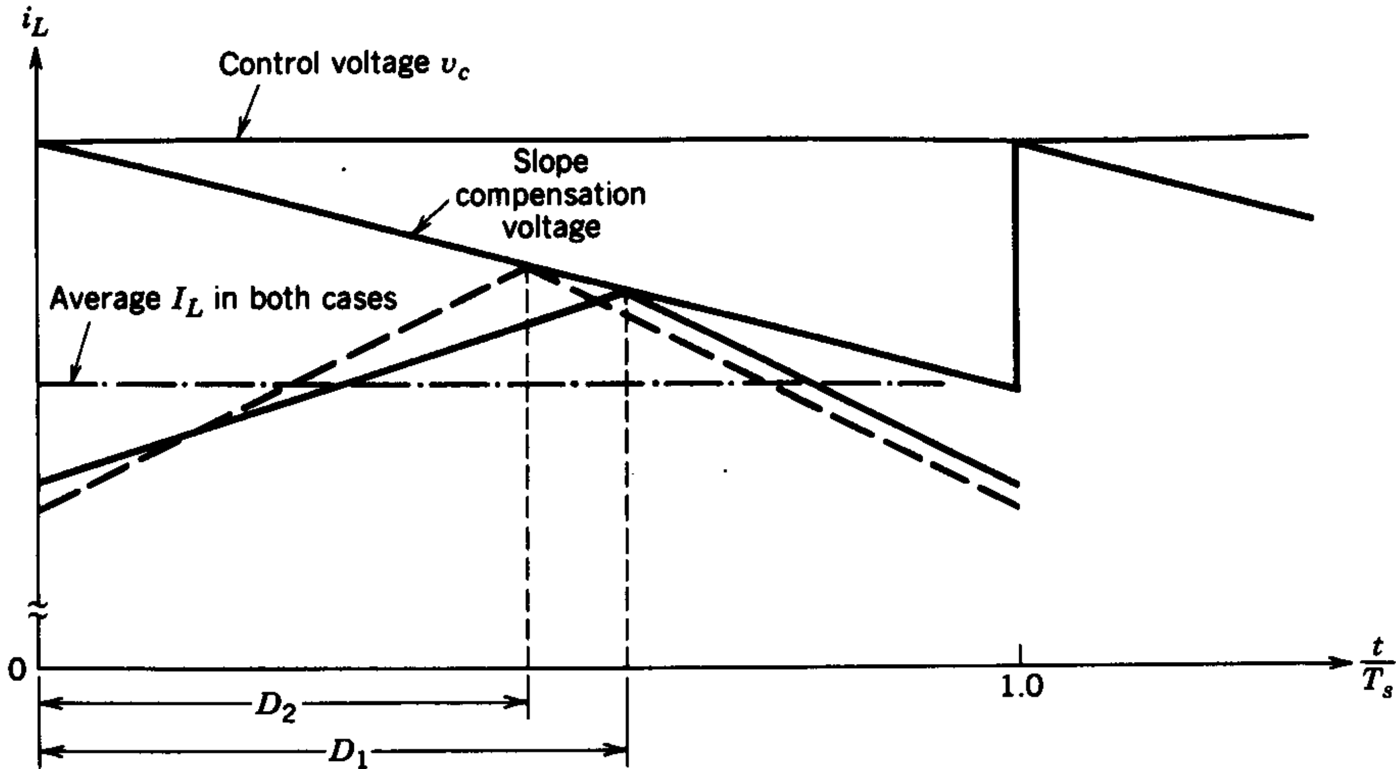

Figure 10-31 Slope compensation in current-mode control (D_2 is smaller for a higher input voltage with a constant V_o).

- Slope compensation is needed

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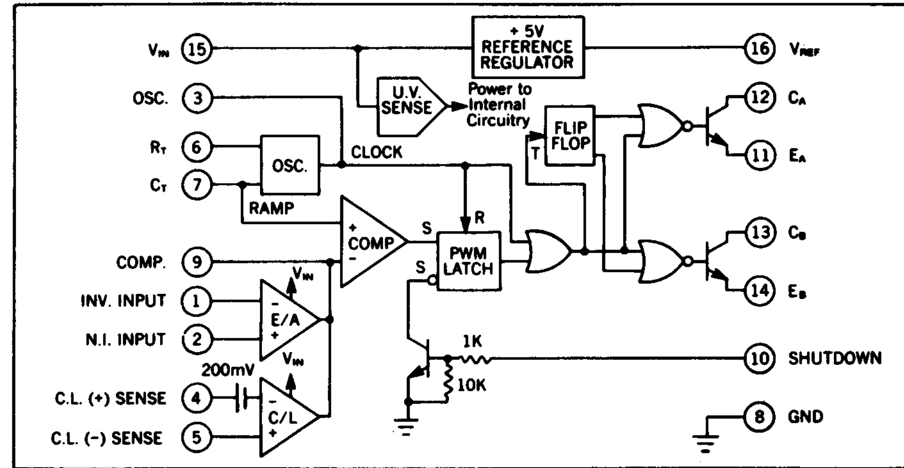
A Typical PWM Control IC



- Many safety control functions are built in

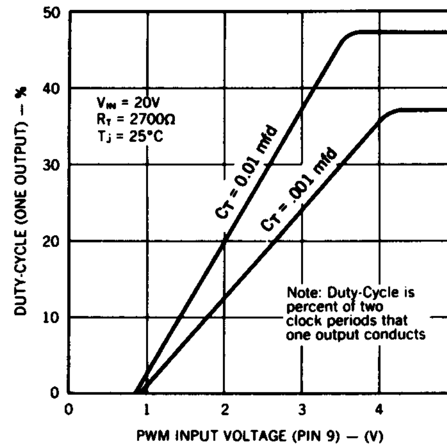


Figure 10-32 Pulse-width modulator UC1524A: (*a*) block diagram; (*b*) transfer function. (*Courtesy of Unitrode Integrated Circuits Corp.*)

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Current Limiting

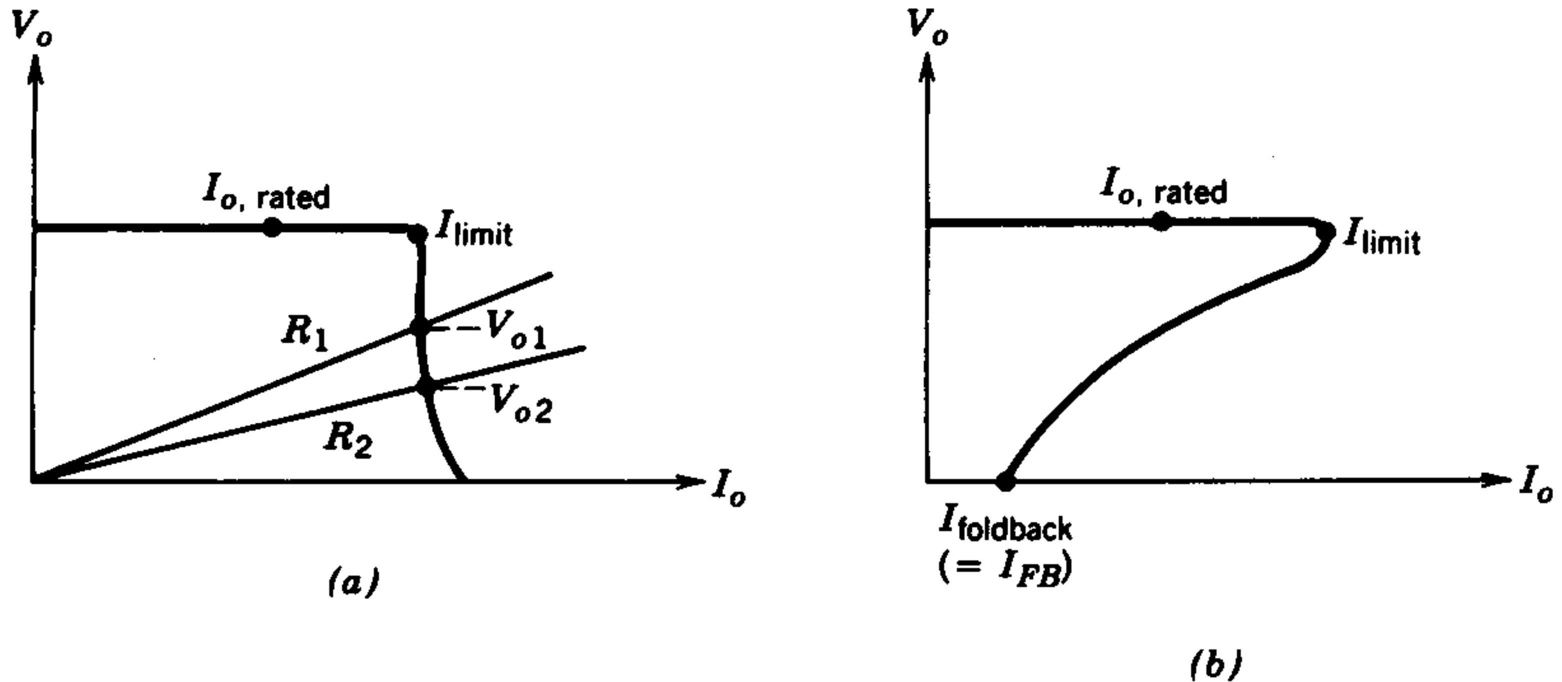
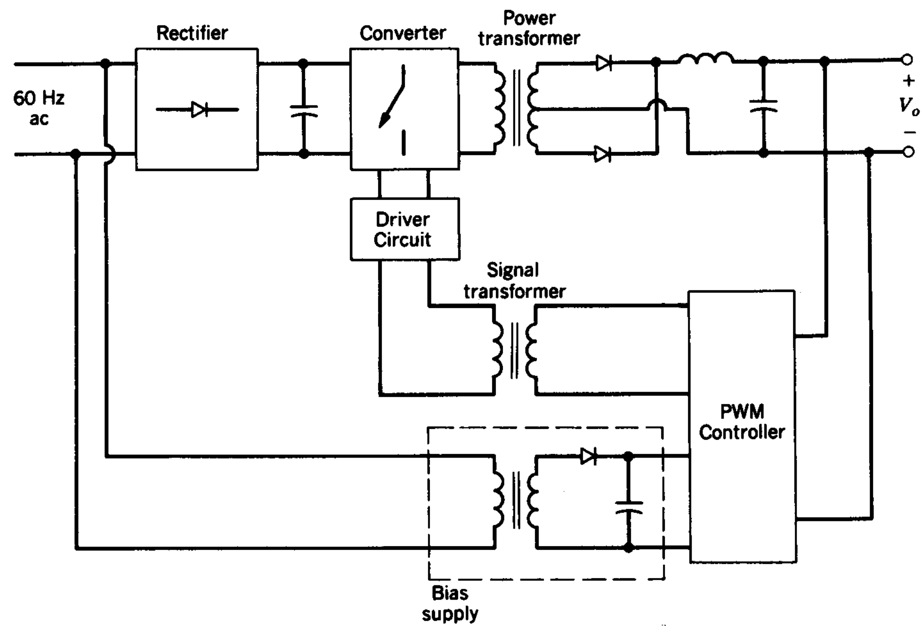


Figure 10-33 Current limiting: (*a*) constant current limiting; (*b*) foldback current limiting.

- Two options are shown

Implementing Electrical Isolation in the Feedback Loop

- Two ways are shown



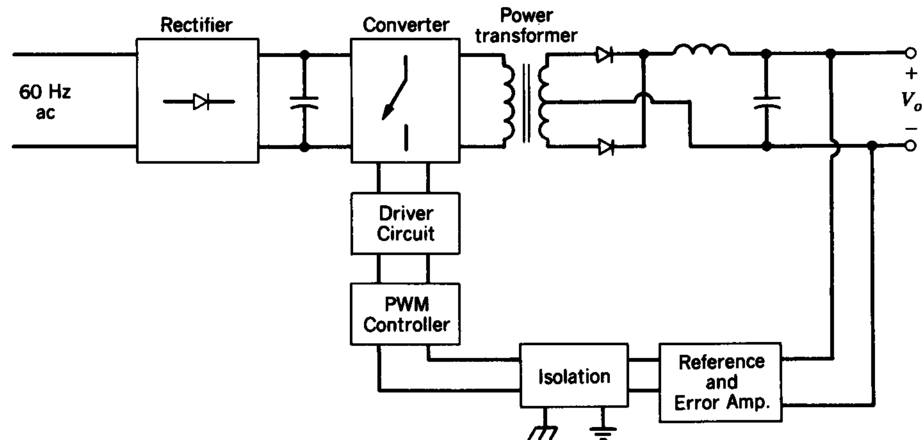


Figure 10-34 Electrical isolation in the feedback loop: (*a*) secondary-side control; (*b*) primary-side control.

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Implementing Electrical Isolation in the Feedback Loop

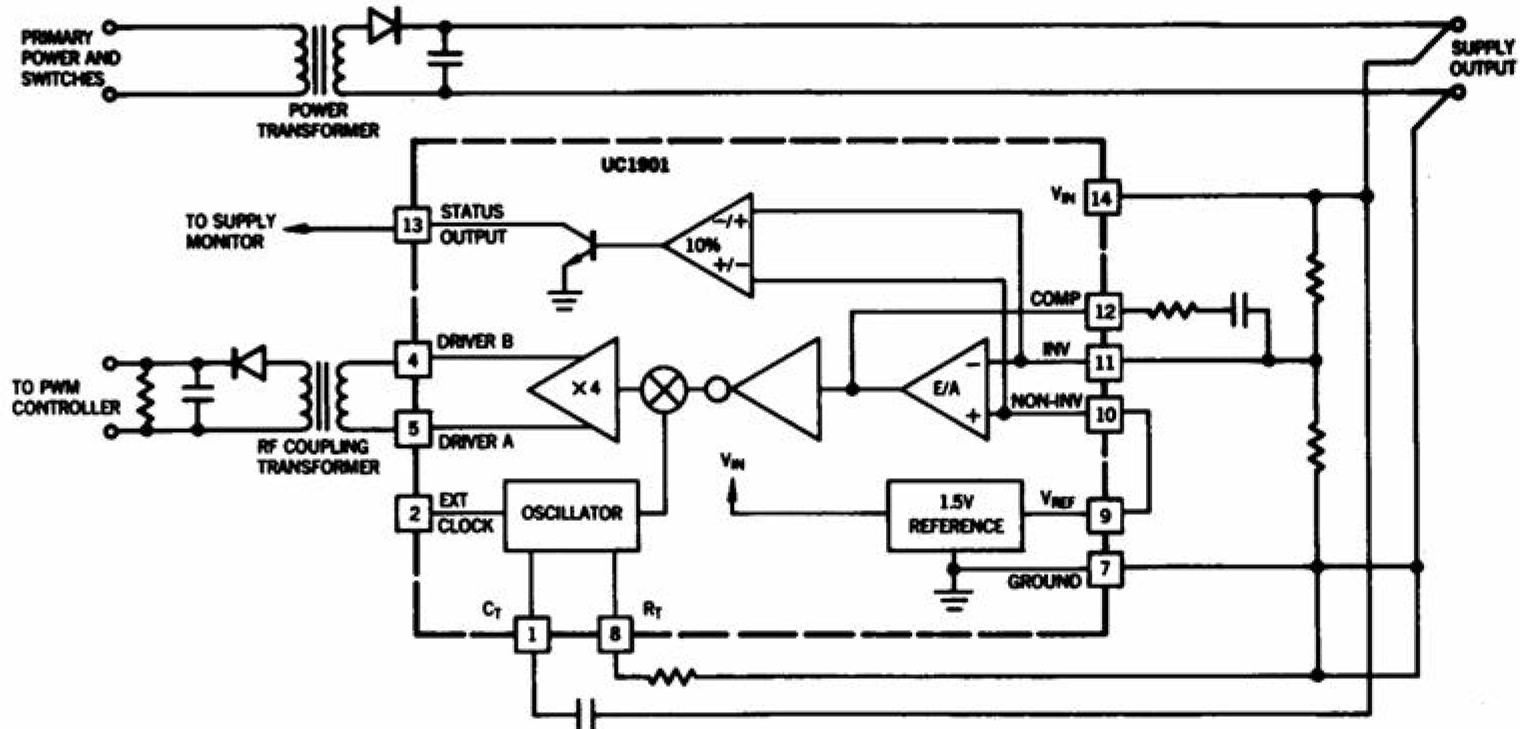

Figure 10-35 Isolated feedback generator UC1901. (*Courtesy of Unitrode Integrated Circuits Corp.*)

- A dedicated IC for this application is available

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Input Filter

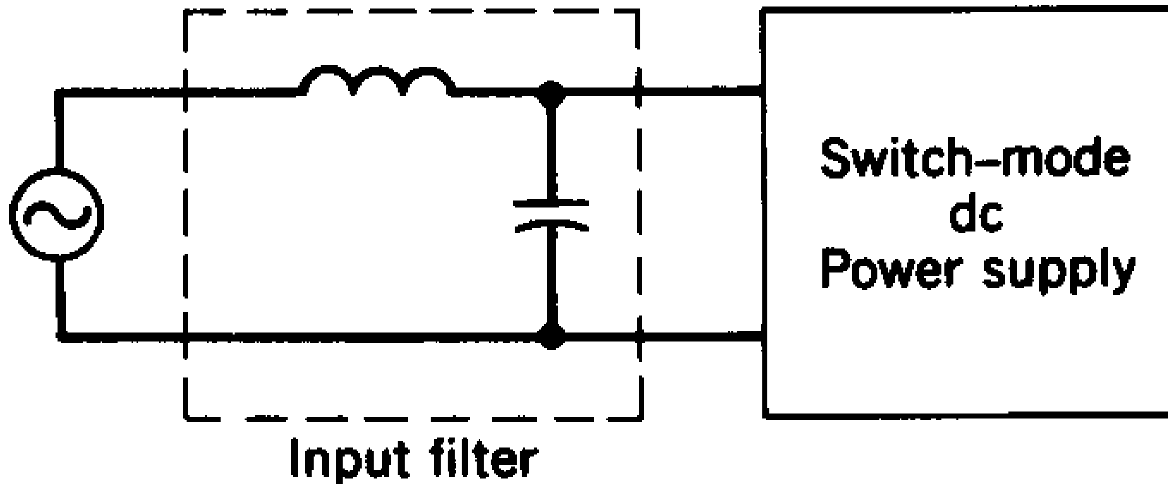

Figure 10-36 Input filter.

- Needed to comply with the EMI and harmonic limits

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ESR of the Output Capacitor

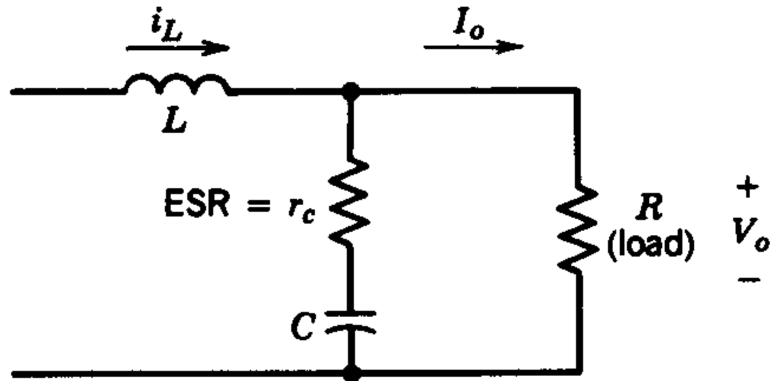

Figure 10-37 ESR in the output capacitor.

- ESR often dictates the peak-peak voltage ripple

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Chapter 11

Power Conditioners and Uninterruptible Power Supplies

Chapter 11 Power Conditioners and Uninterruptible Power Supplies **354**

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11-2 Power Line Disturbances 354
11-3 Power Conditioners 357
11-4 Uninterruptible Power Supplies (UPSs) 358
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- Becoming more of a concern as utility de-regulation proceeds

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Distortion in the Input Voltage

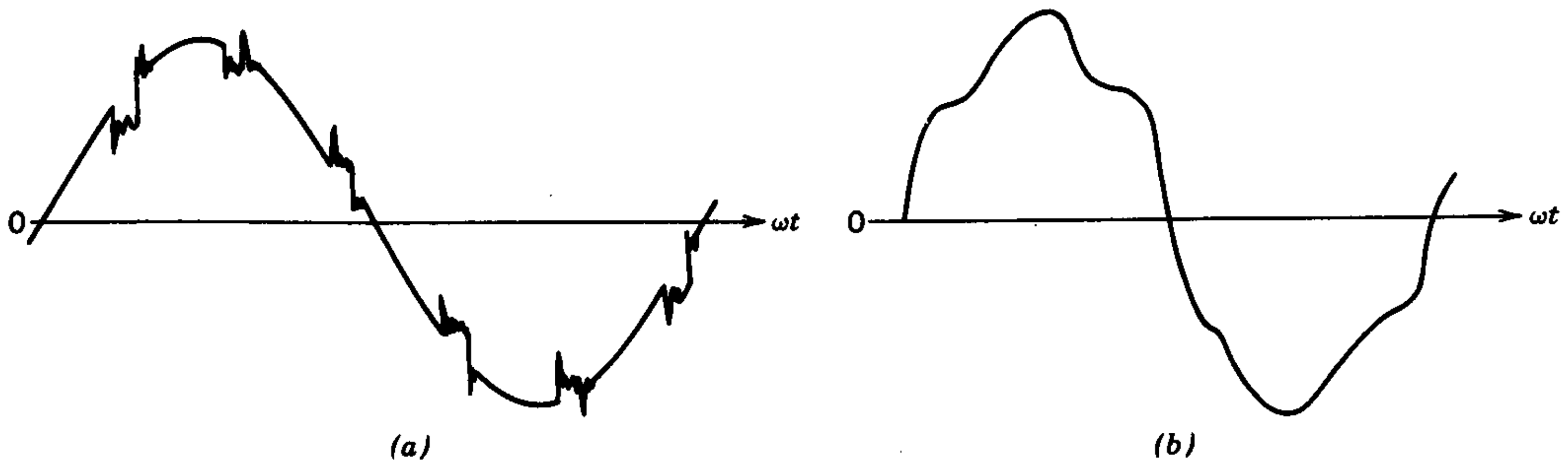

Figure 11-1 Possible distortions in input voltage: *(a)* chopped voltage waveform; *(b)* distorted voltage waveform due to harmonics.

- The voltage supplied by the utility may not be sinusoidal

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Typical Voltage Tolerance Envelope for Computer Systems

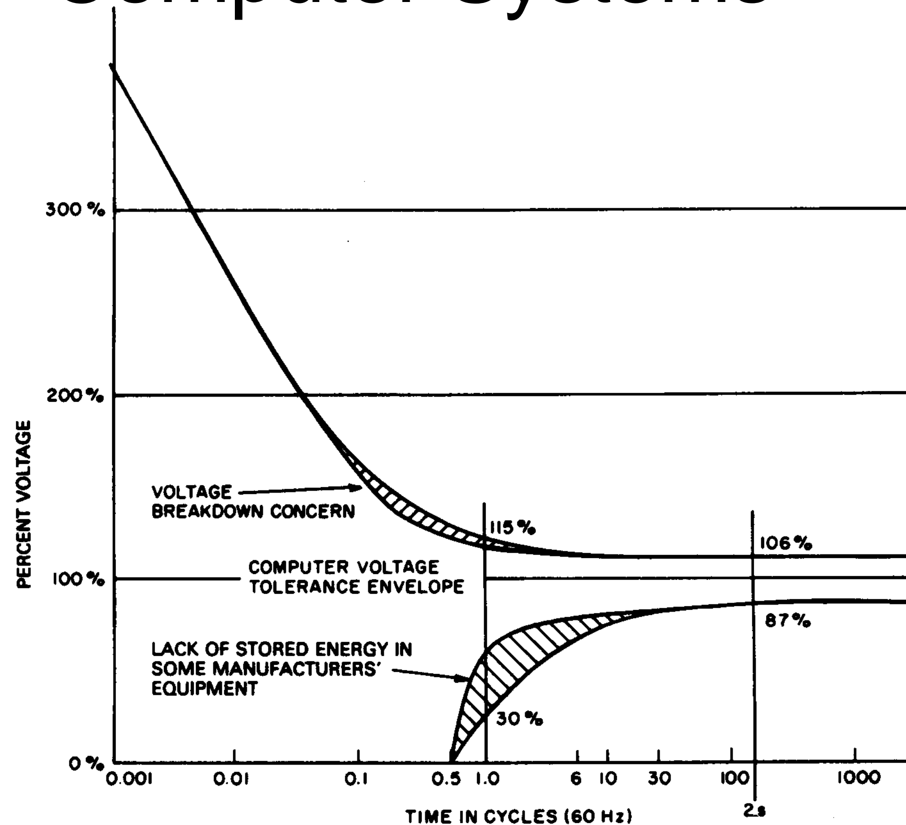

Figure 11-2 Typical computer system voltage tolerance envelope. (*Source:* IEEE Std. 446, "Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications.")

- This has been superceded by a more recent standard

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Typical Range of Input Power Quality

Table 11-1 Typical Range of Input Power Quality and Load Parameters of Major Computer Manufacturers

Parameters[a]	*Range or Maximum*
1. Voltage regulation, steady state	+5, −10 to +10%, −15% (ANSI C84.1—1970 is +6, −13%)
2. Voltage disturbances	
a. Momentary undervoltage	−25 to −30% for less than 0.5 s, with −100% acceptable for 4–20 ms
b. Transient overvoltage	+150 to 200% for less than 0.2 ms
3. Voltage harmonic distortion[b]	3–5% (with linear load)
4. Noise	No standard
5. Frequency variation	60 Hz ± 0.5 Hz to ±1 Hz
6. Frequency rate of change	1 Hz/s (slew rate)
7. 3φ, Phase voltage unbalance[c]	2.5–5%
8. 3φ, Load unbalance[d]	5–20% maximum for any one phase
9. Power factor	0.8–0.9
10. Load demand	0.75–0.85 (of connected load)

[a]Parameters 1, 2, 5, and 6 depend on the power source, while parameters 3, 4, and 7 are the product of an interaction of source and load, and parameters 8, 9, and 10 depend on the computer load alone.

[b]Computed as the sum of all harmonic voltages added vectorially.

[c]Computed as follows:

$$\textit{Percent}\text{ phase voltage unbalance} = \frac{3(V_{max} - V_{min})}{V_a + V_b + V_c} \times 100$$

[d]Computed as difference from average single-phase load.

Source: IEEE Std. 446, "Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications."

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Electronic Tap Changers

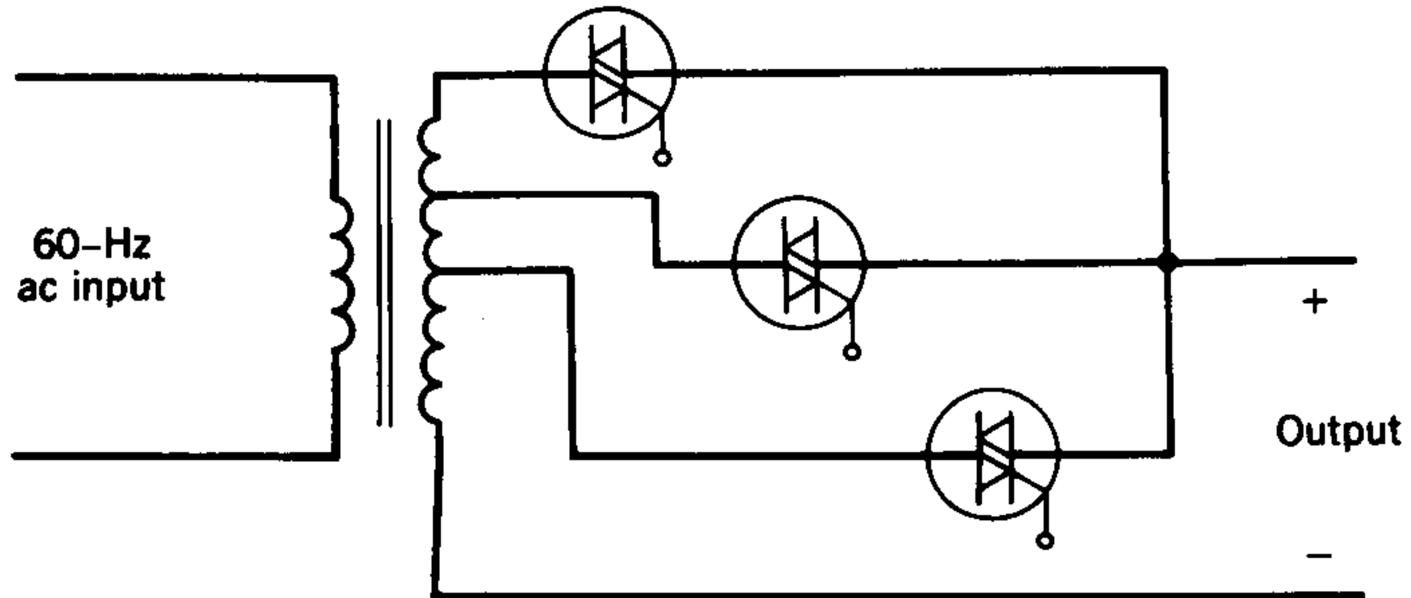

Figure 11-3 Electronic tap changer.

- Controls voltage magnitude by connecting the output to the appropriate transformer tap

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Uninterruptible Power Supplies (UPS)

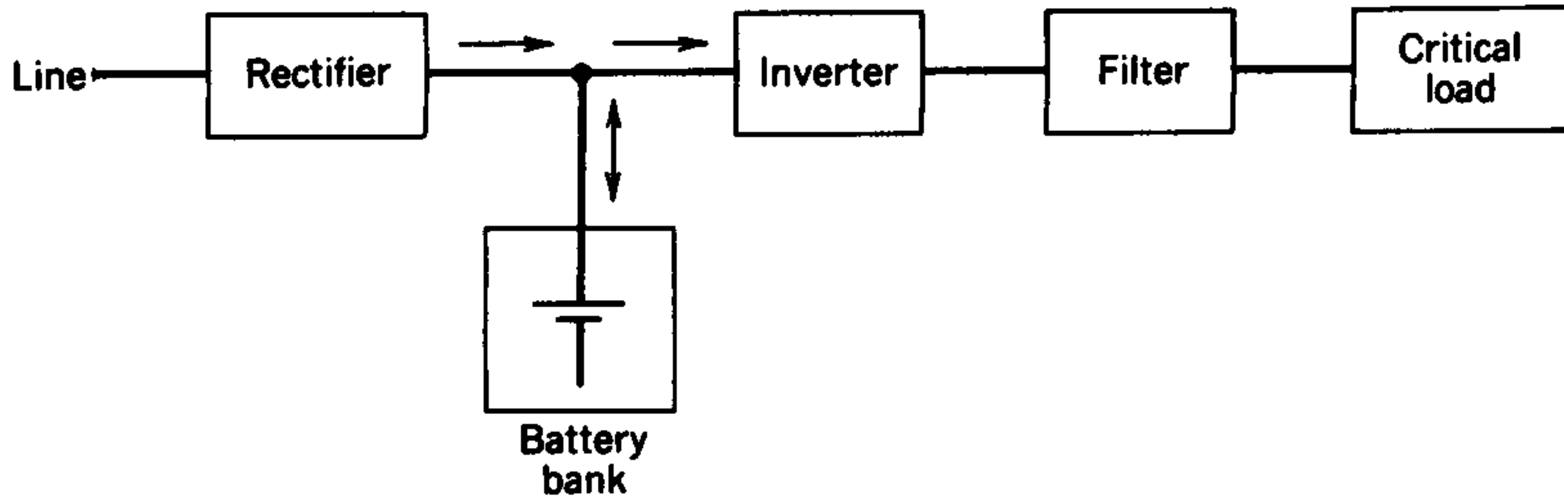

Figure 11-4 A UPS block diagram.

- Block diagram; energy storage is shown to be in batteries but other means are being investigated

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UPS: Possible Rectifier Arrangements

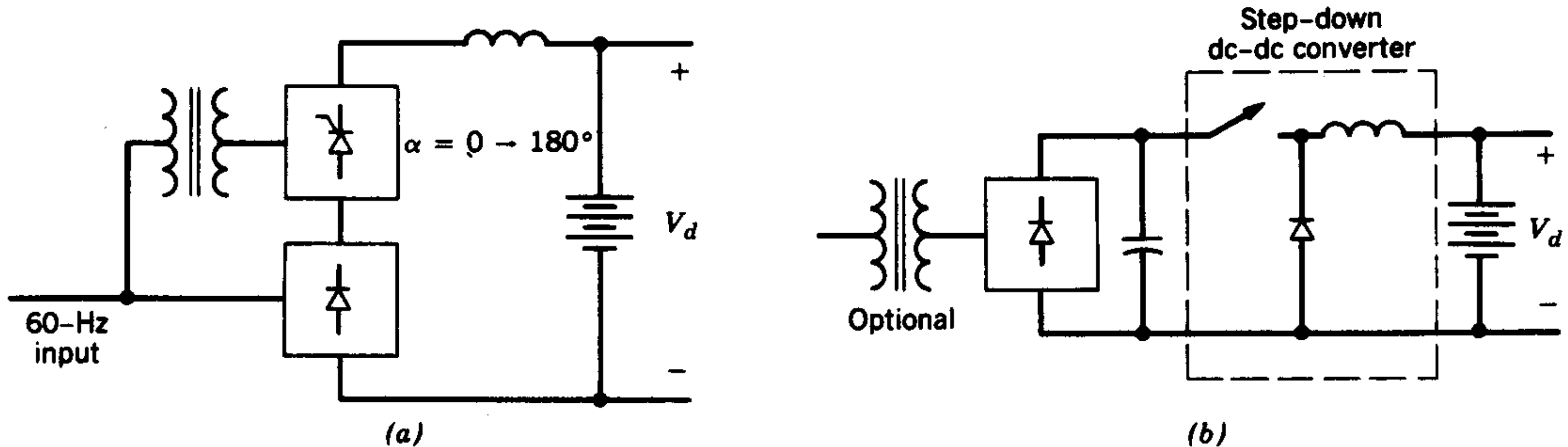

Figure 11-5 Possible rectifier arrangements.

- The input normally supplies power to the load as well as charges the battery bank

UPS: Another Possible Rectifier Arrangement

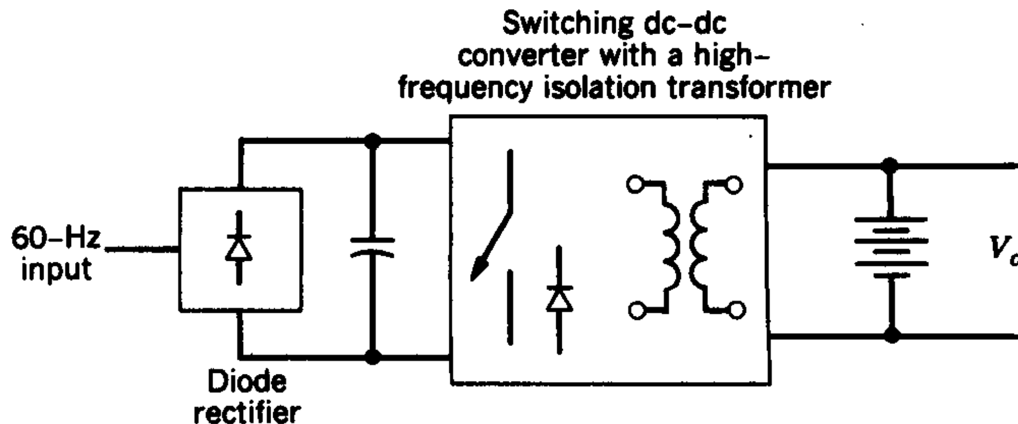

Figure 11-6 Rectifier consisting of a high-frequency isolation transformer.

- Consists of a high-frequency isolation transformer

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UPS: Another Possible Input Arrangement

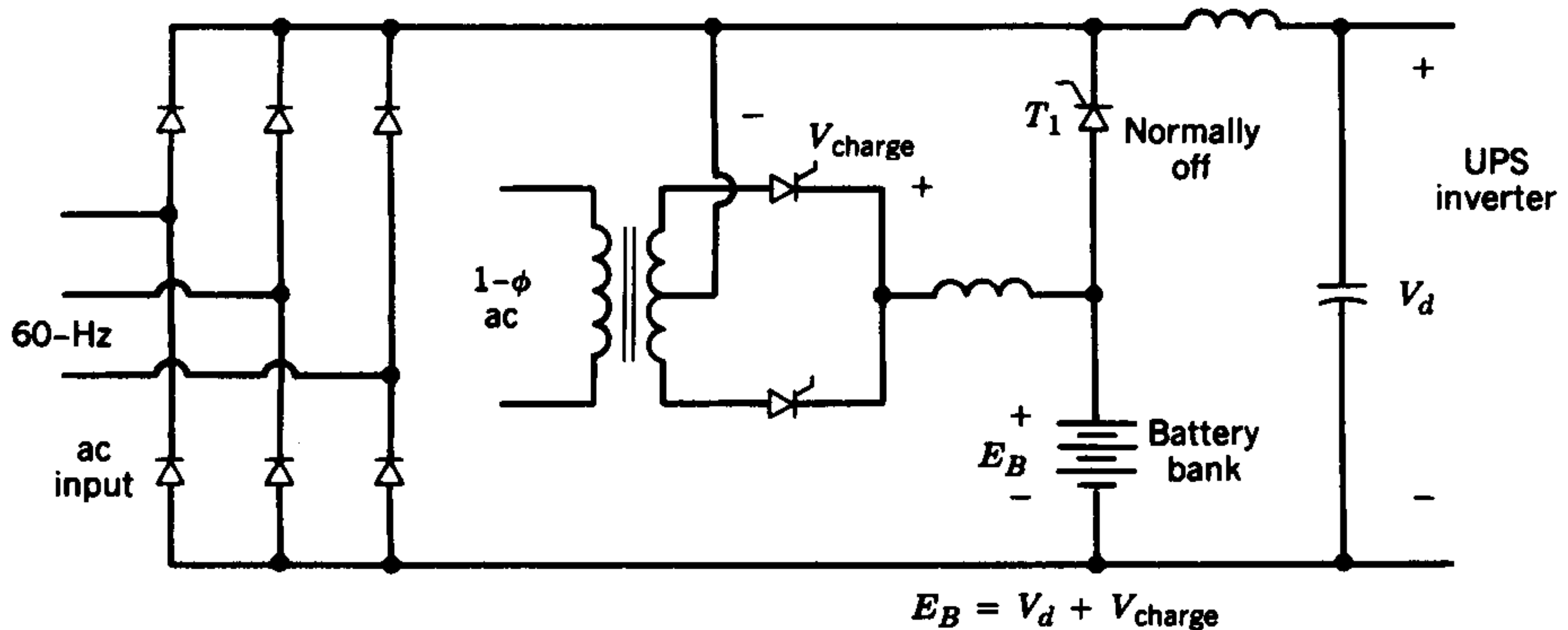

Figure 11-7 A rectifier with a separate battery charger circuit.

- A separate small battery charger circuit

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Battery Charging Waveforms as Function of Time

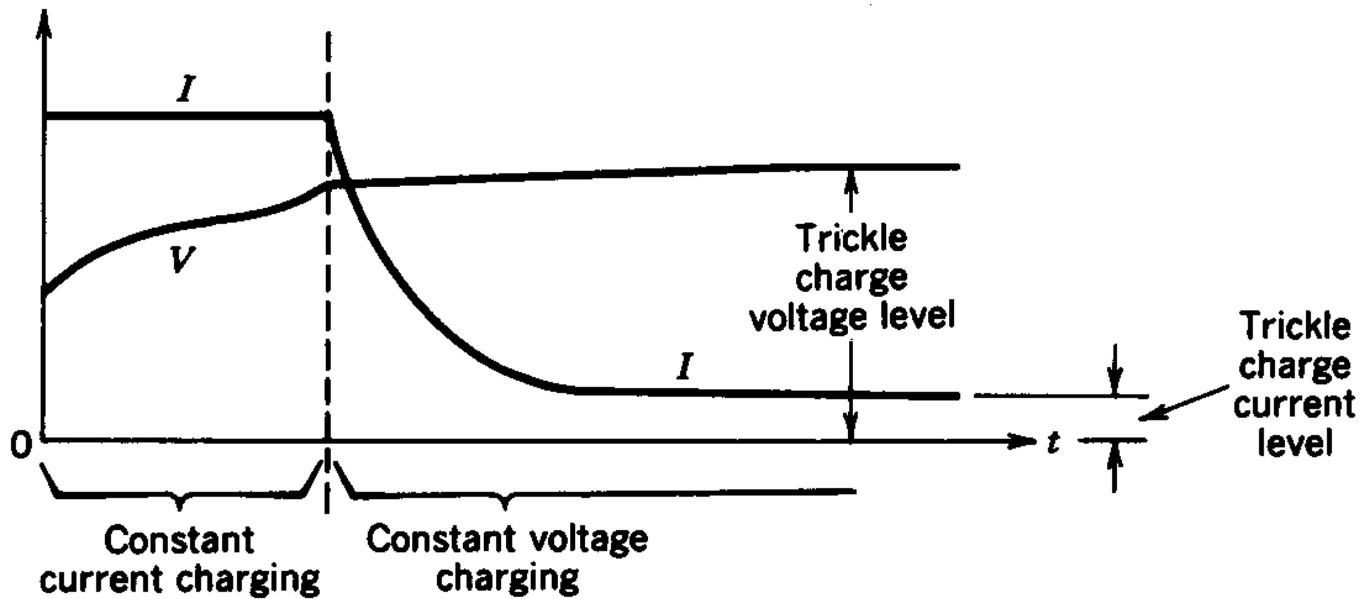

Figure 11-8 Charging of a battery after a line outage causes battery discharge.

- Initially, a discharged battery is charged with a constant current

UPS: Various Inverter Arrangements

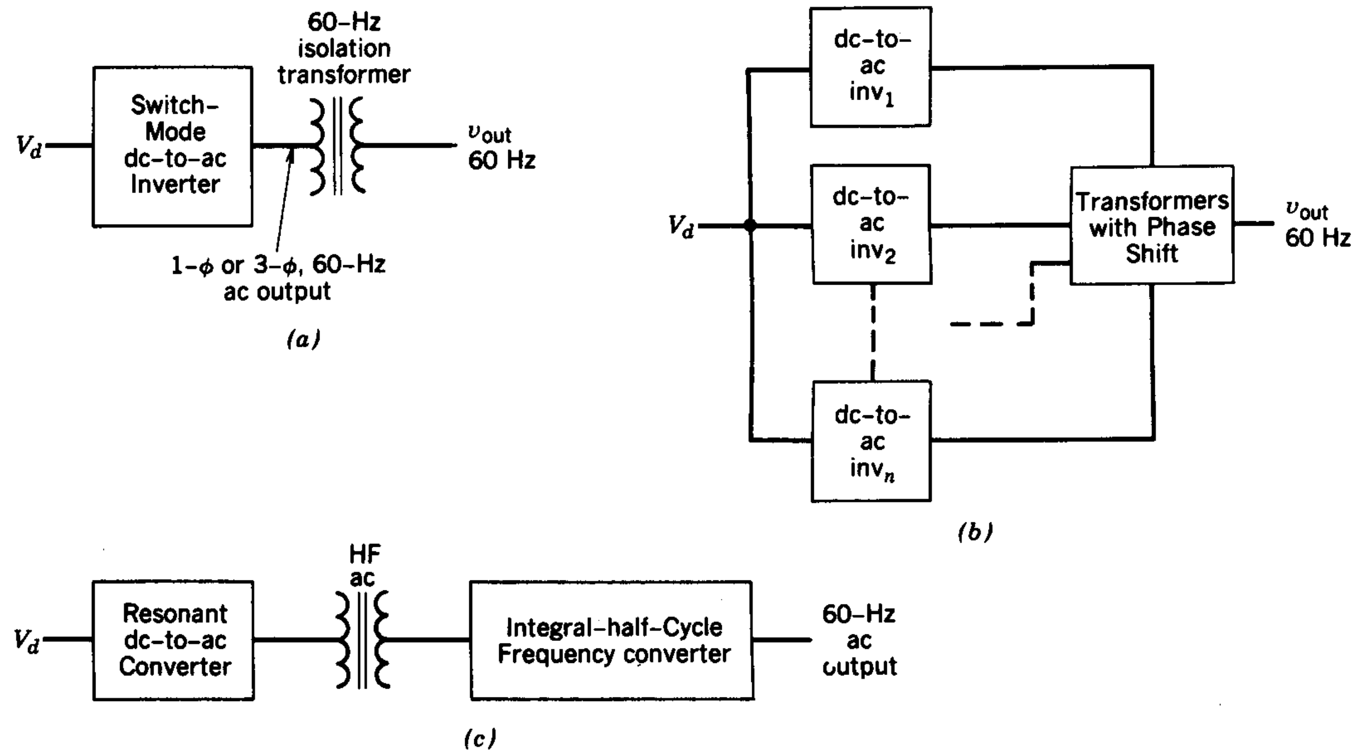

Figure 11-9 Various inverter arrangements.

- Depends on applications, power ratings

UPS: Control

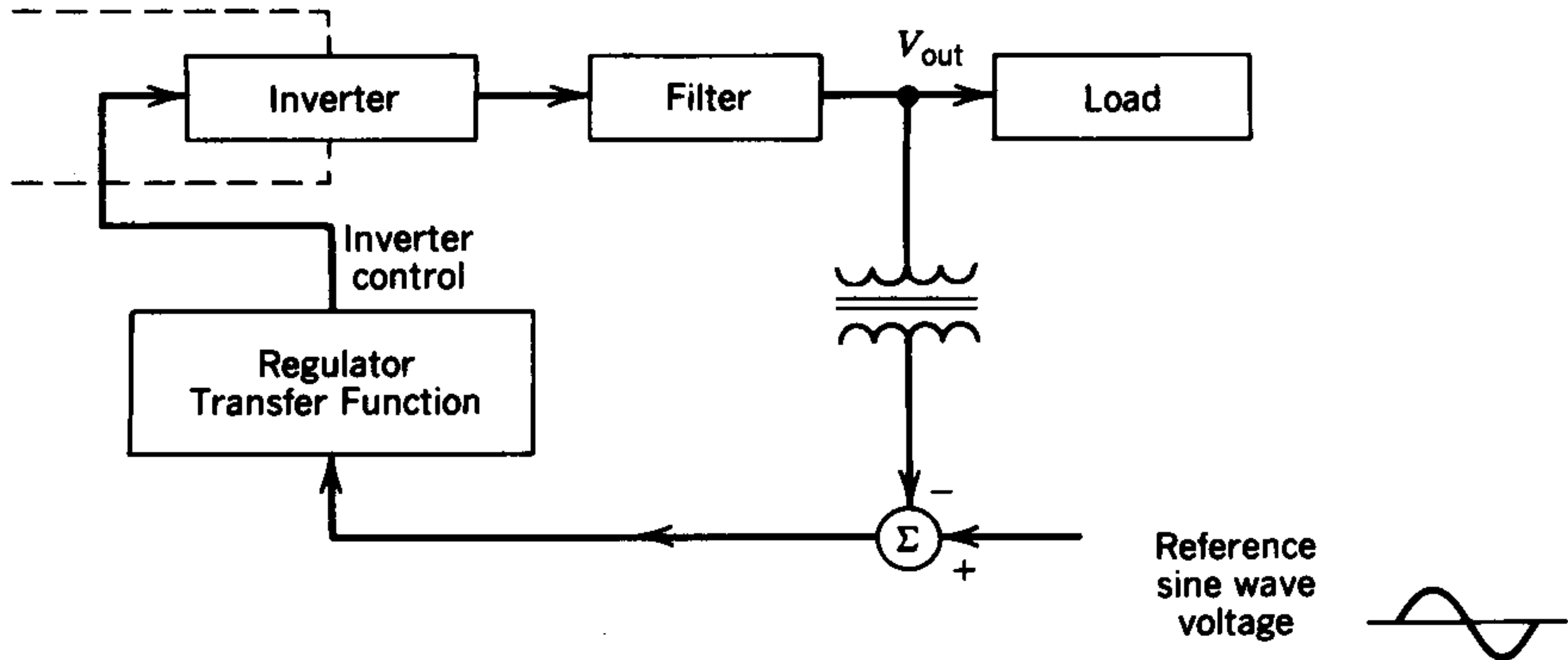

Figure 11-10 Uninterruptible power supply control.

- Typically the load is highly nonlinear and the voltage output of the UPS must be as close to the desired sinusoidal reference as possible

UPS Supplying Several Loads

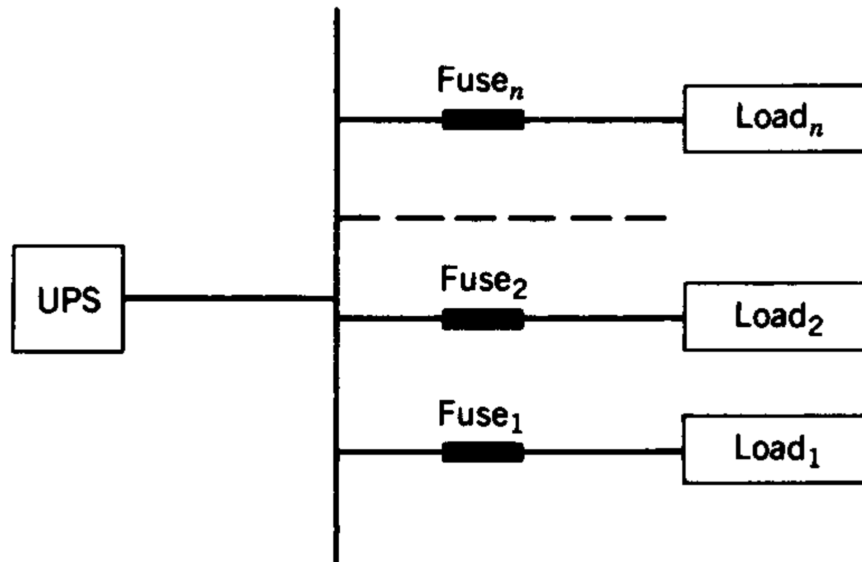

Figure 11-11 A UPS supplying several loads.

- With higher power UPS supplying several loads, malfunction within one load should not disturb the other loads

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Another Possible UPS Arrangement

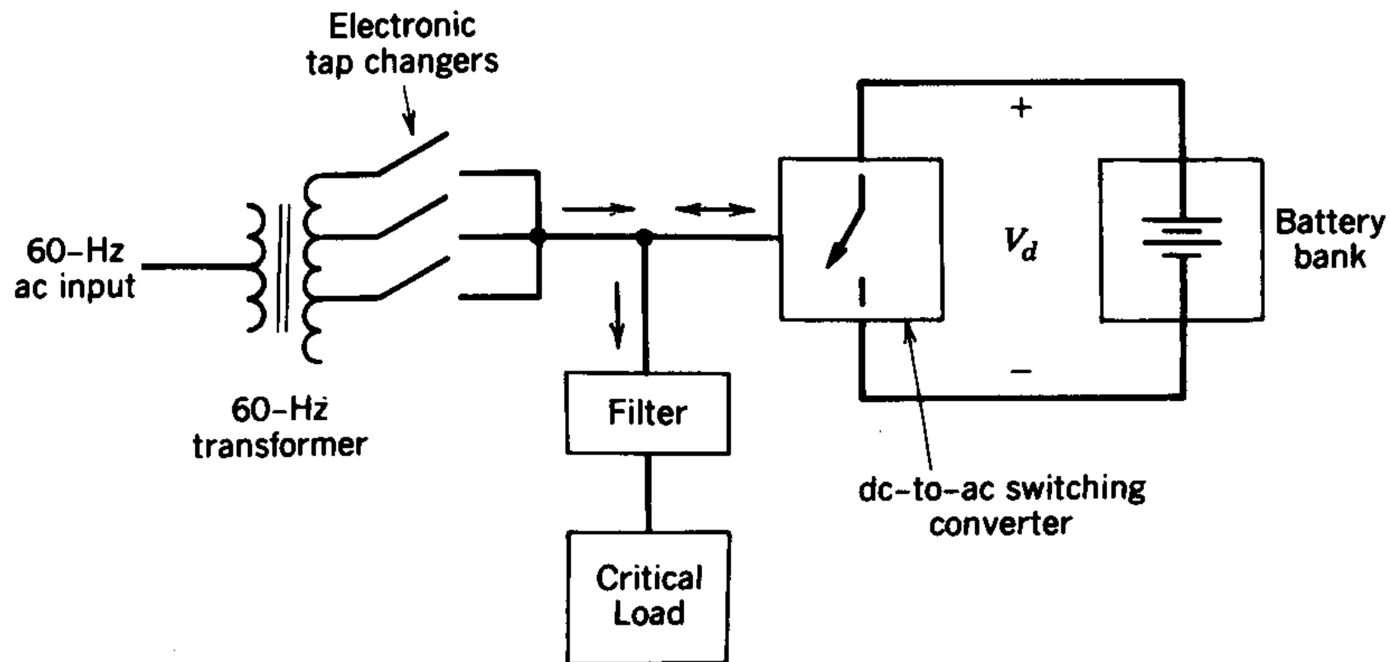

Figure 11-12 A UPS arrangement where the functions of battery charging and inverter are combined.

- Functions of battery charging and the inverter are combined

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UPS: Using the Line Voltage as Backup

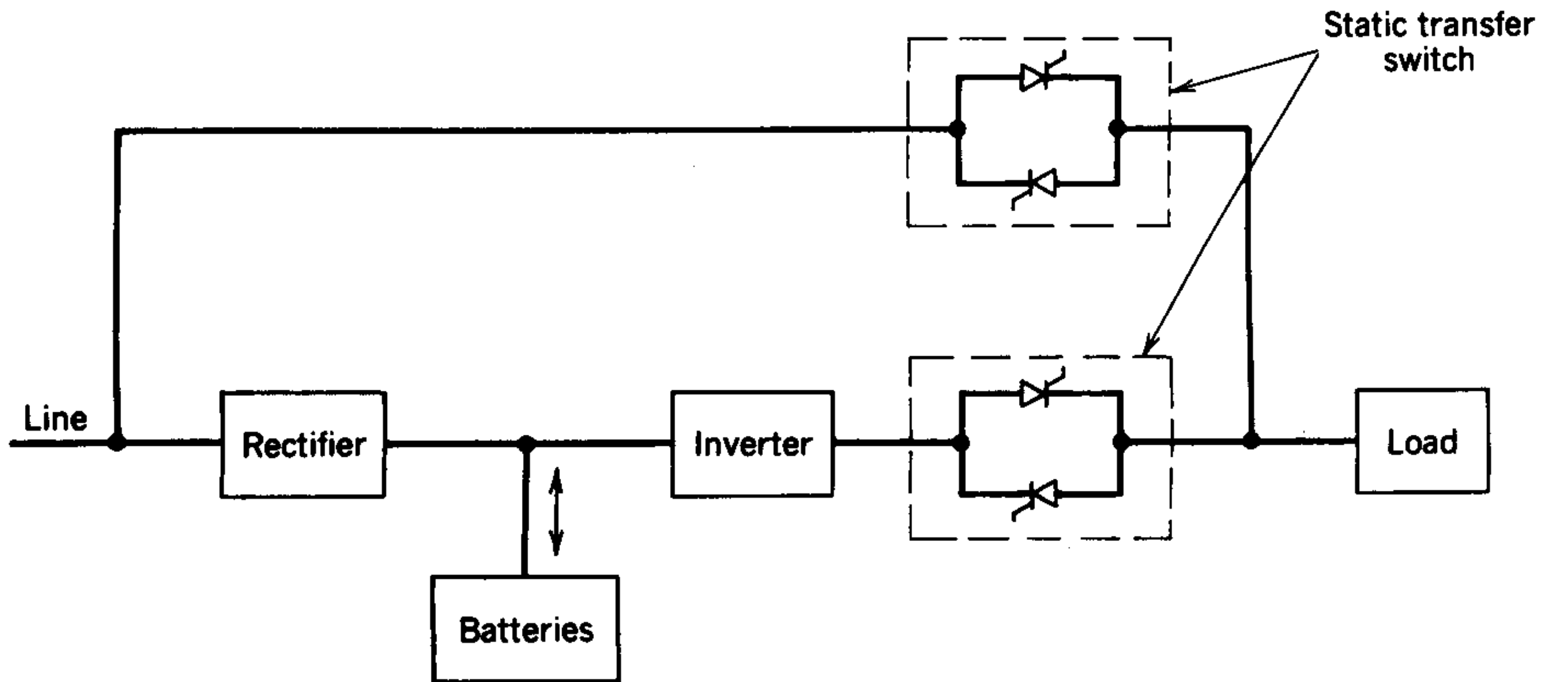

Figure 11-13 Line as backup.

- Needs static transfer switches

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Chapter 12

Introduction to Motor Drives

Chapter 12 Introduction to Motor Drives **367**

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12-2 Criteria for Selecting Drive Components 368
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- Motor drives are one of the most important applications of power electronics

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Control Structure of Drives

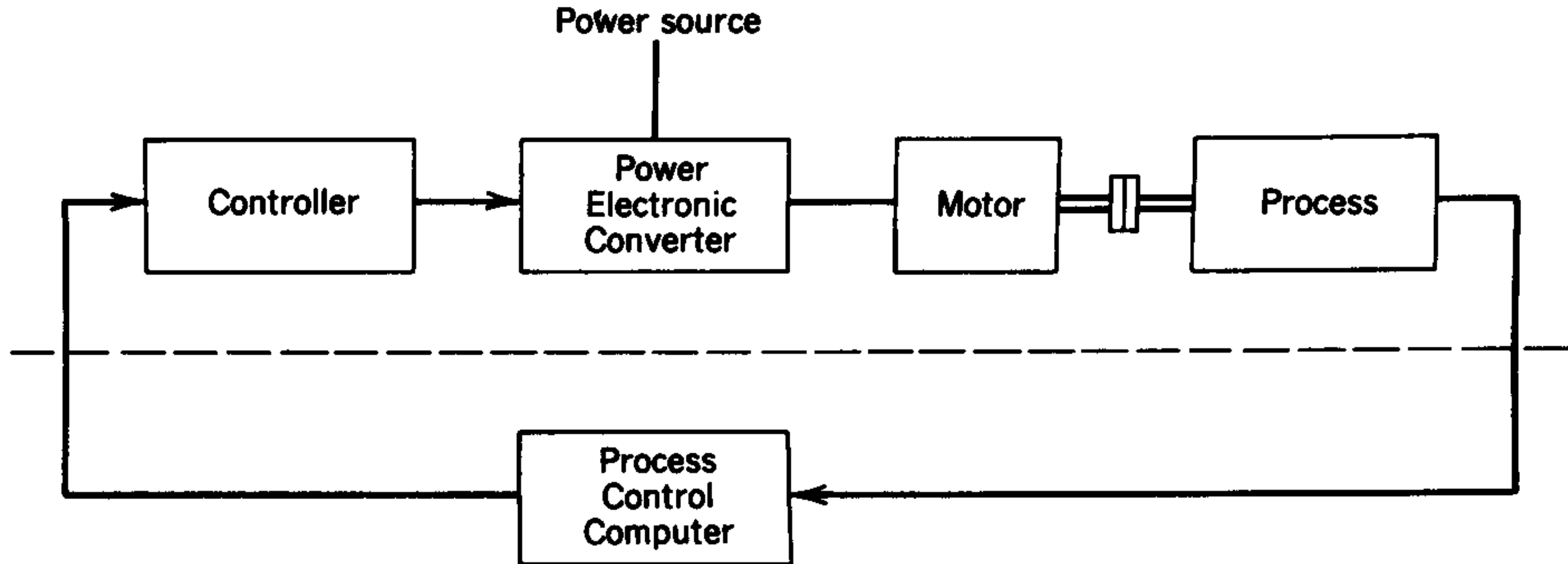

Figure 12-1 Control of motor drives.

- Very general description

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Servo Drives

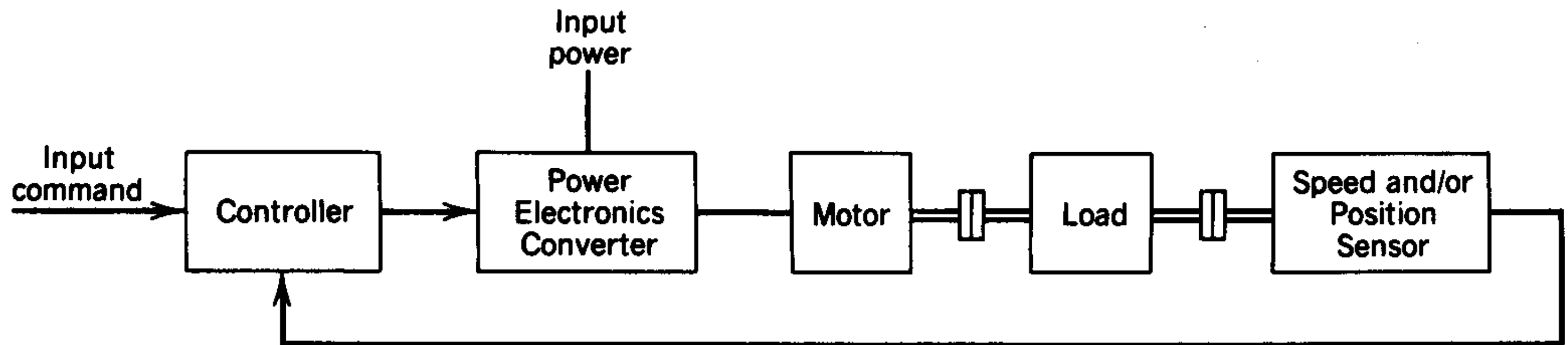

Figure 12-2 Servo drives.

- The basic structure is the same regardless of the drive that is selected

An Example of Adjustable Speed Drives

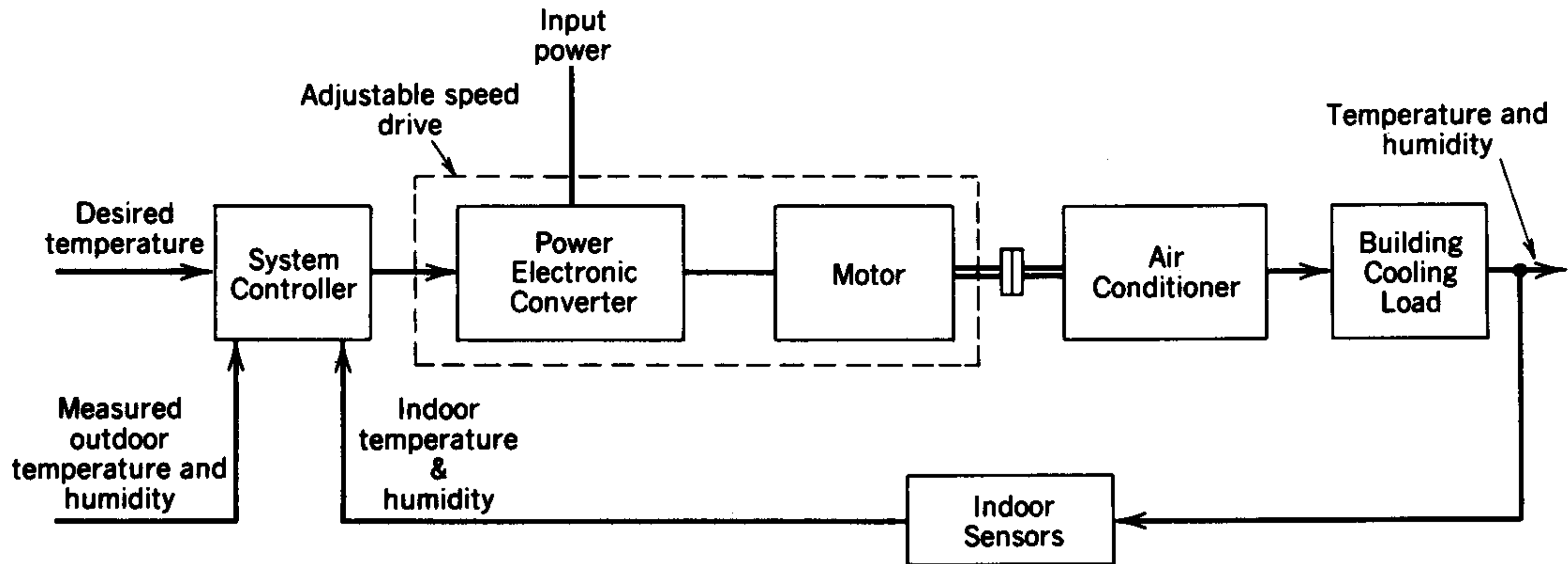

Figure 12-3 Adjustable-speed drive in an air conditioning system.

- The speed of the drive response is not important here

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A Representation of the Load on a Drive

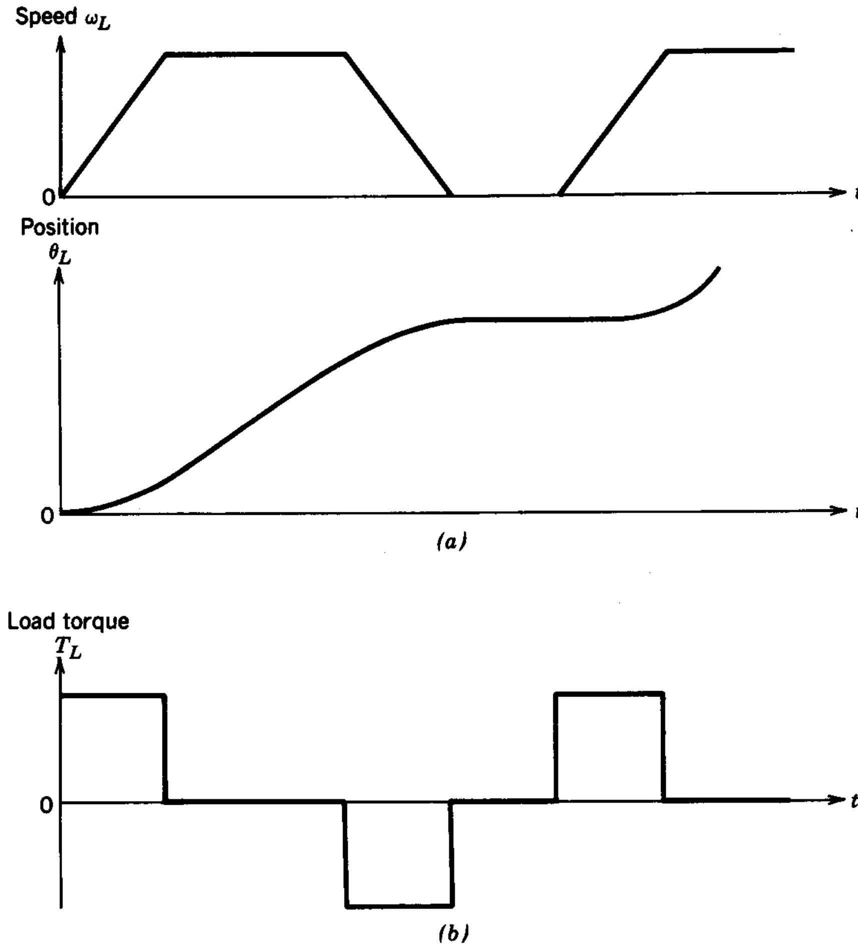

Figure 12-4 Load profile: (*a*) load–motion profile; (*b*) load–torque profile (assuming a purely inertial load).

- This cycle may repeat continuously

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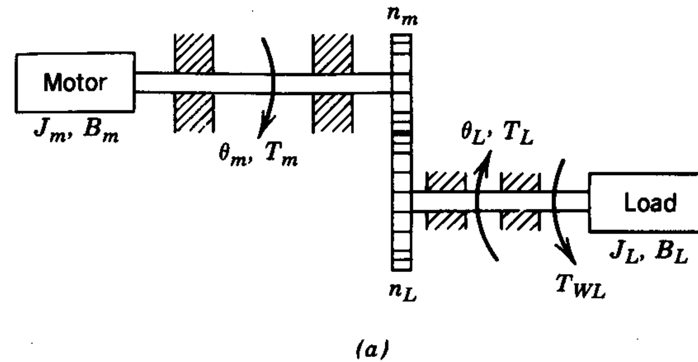
Two Coupling Mechanisms



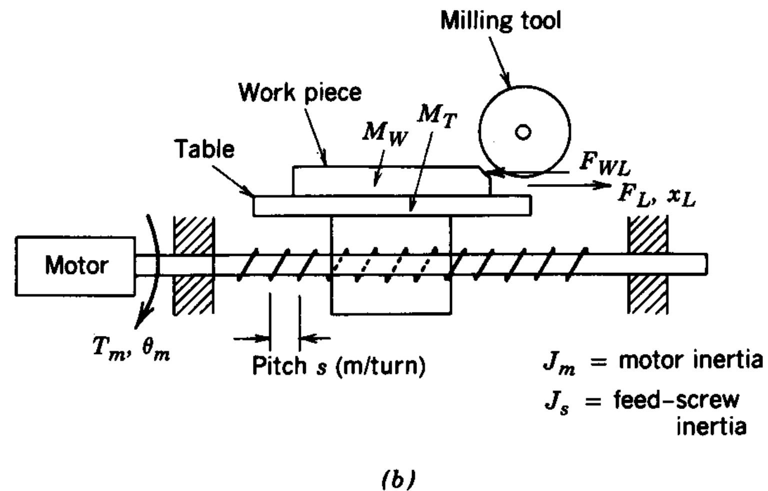


Figure 12-5 Coupling mechanisms: (*a*) gear; (*b*) feed screw.

- Commonly used

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Instantaneous Waveforms of Torque and Current

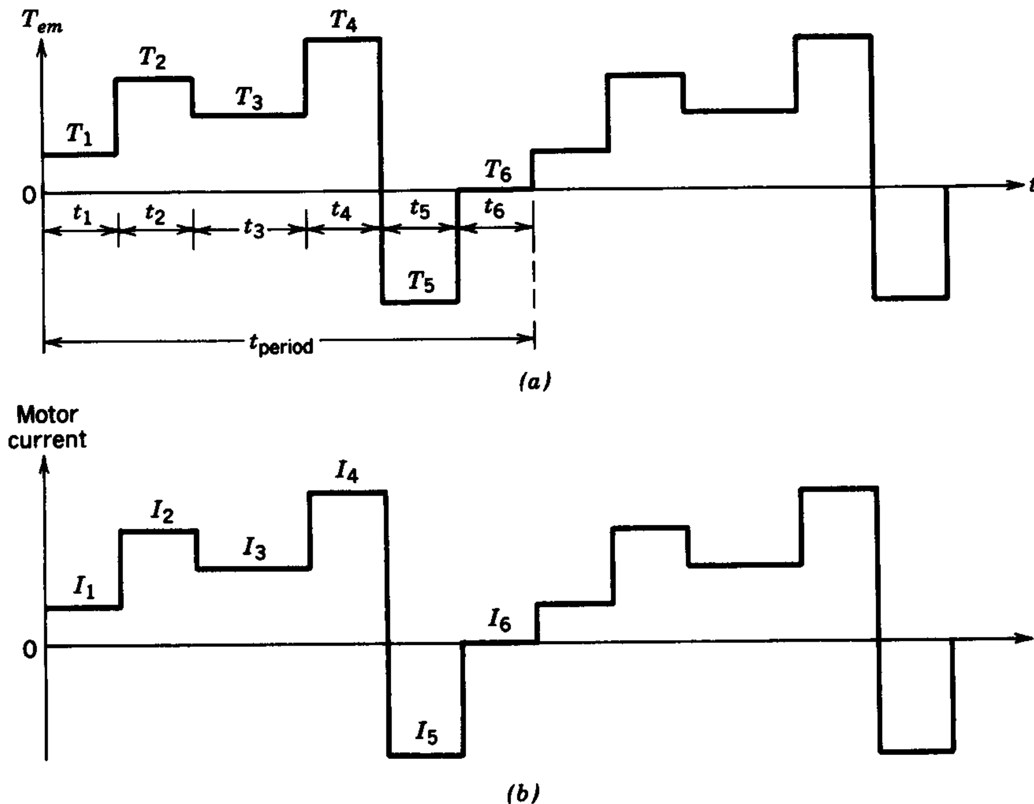

Figure 12-6 Motor torque and current.

- Their RMS values may determine the limit

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Simplified Circuit of a Drive

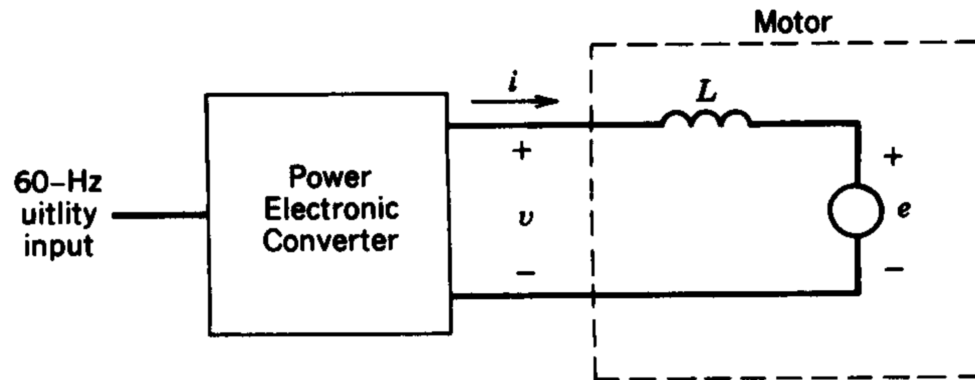

Figure 12-7 Simplified circuit of a motor drive.

- Allows discussion of various parameters and operating conditions on losses and ratings

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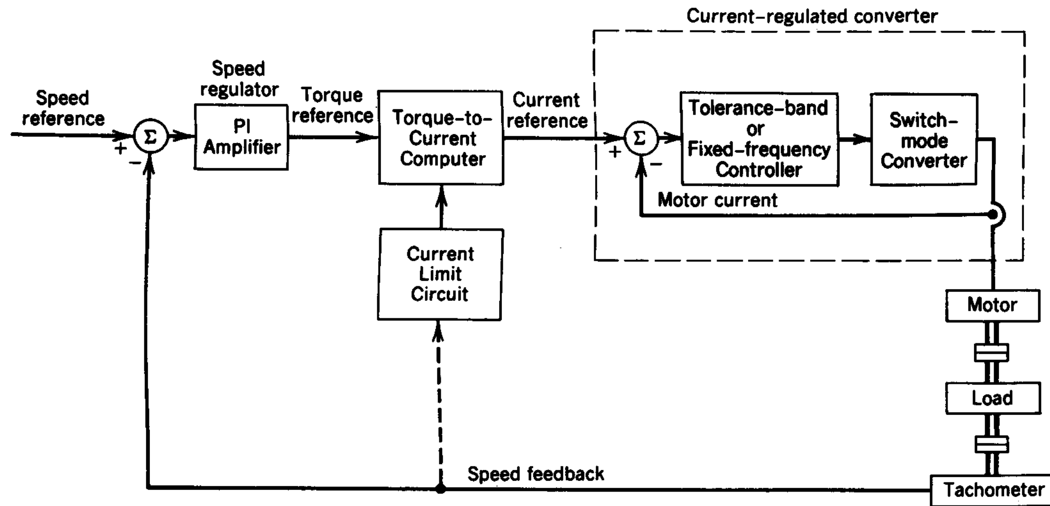
Control of Servo Drives



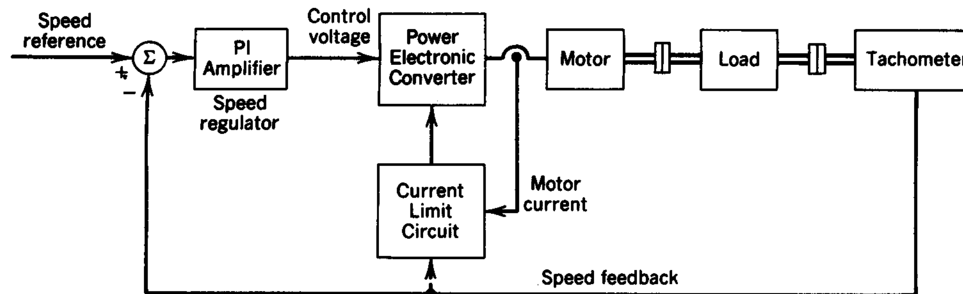


Figure 12-8 Control of servo drives: (*a*) inner current loop; (*b*) no inner current loop.

- The structure is application dependent

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Limiters in the Control Structure

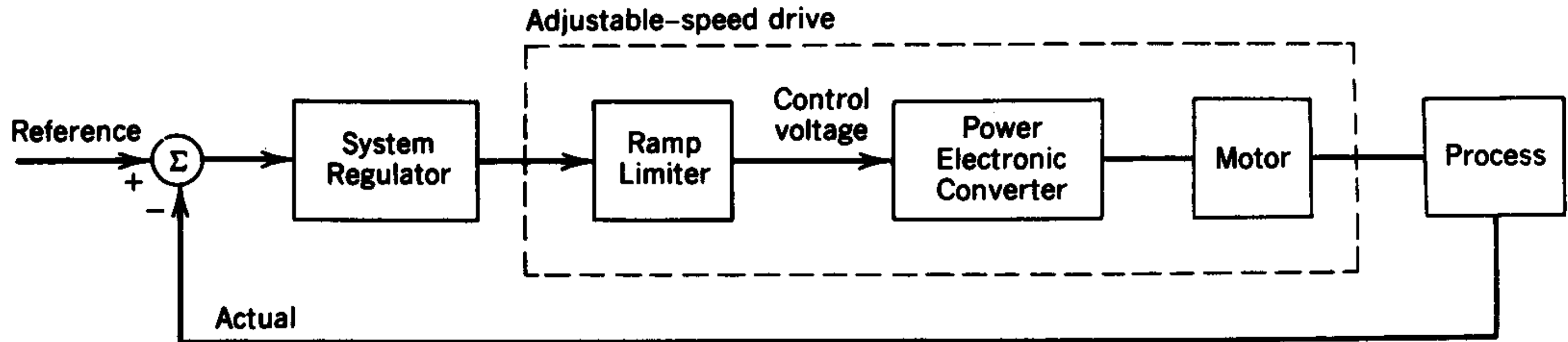

Figure 12-9 Ramp limiter to limit motor current.

- By providing ramp limiters, for example, drive can be prevented from “triping” under sudden changes

Chapter 13

DC-Motor Drives

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13-4 dc Motors with a Separately Excited Field Winding 381
13-5 Effect of Armature Current Waveform 382
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- These drives continue to be used

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DC-Motor Structure

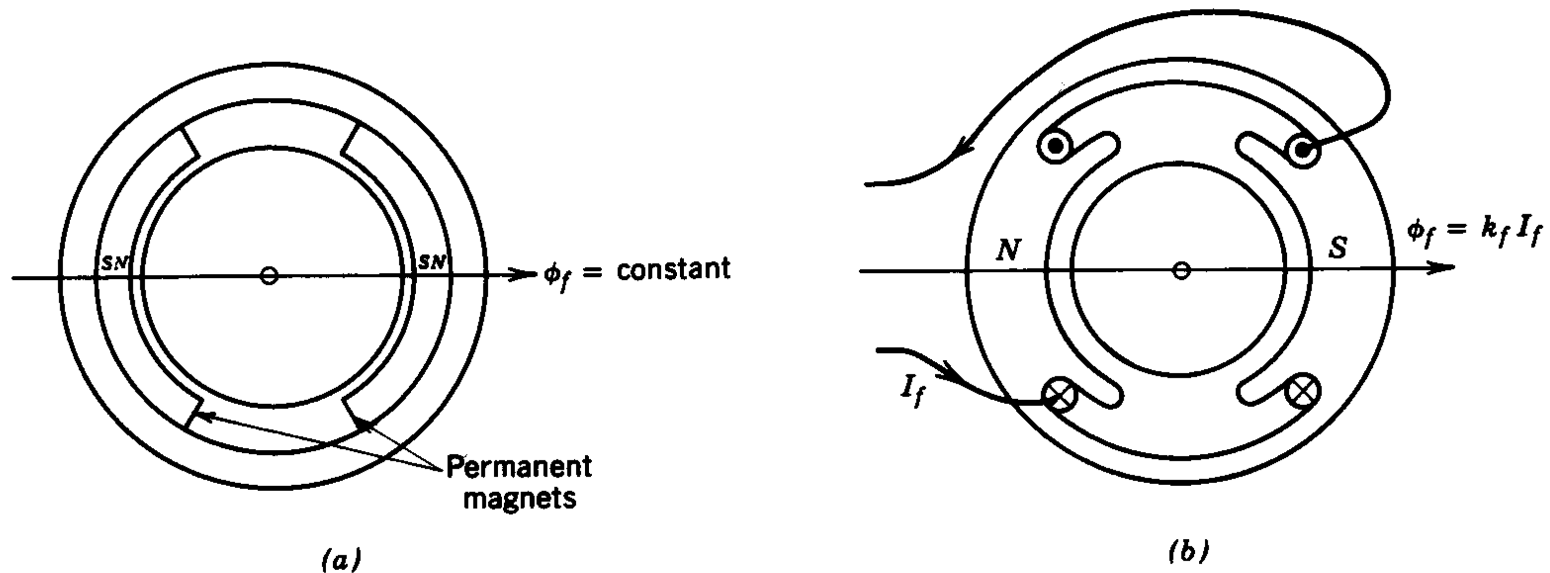

Figure 13-1 A dc motor: (*a*) permanent-magnet motor; (*b*) dc motor with a field winding.

- With permanent magnets or a wound field

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DC-Motor Equivalent Circuit

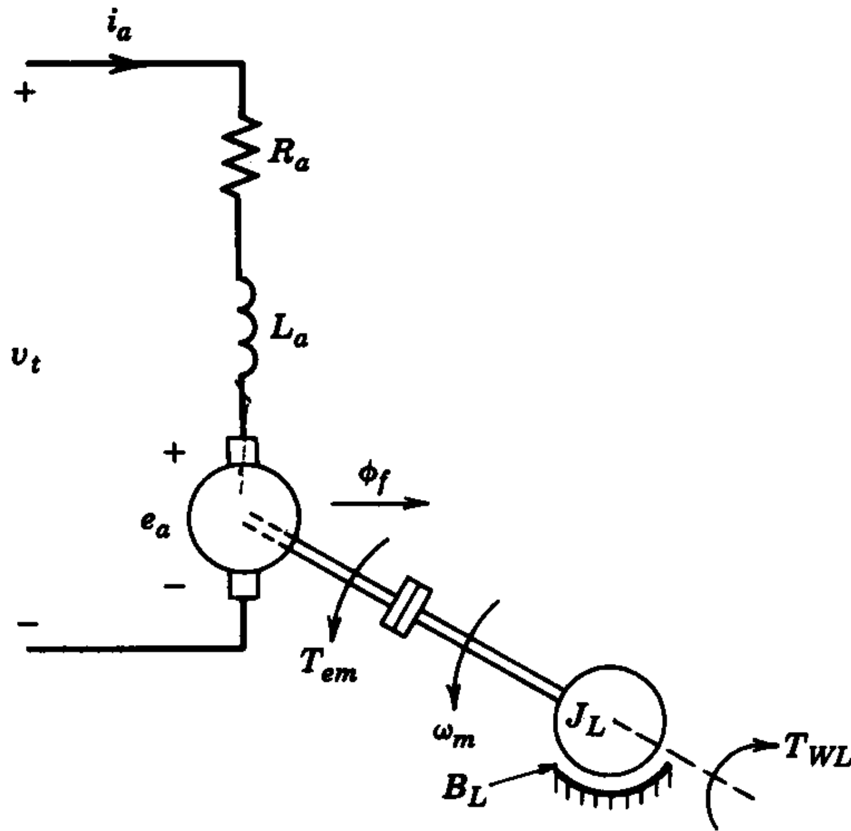

Figure 13-2 A dc motor equivalent circuit.

- The mechanical system can also be represented as an electrical circuit

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Four-Quadrant Operation of DC-Motor Drives

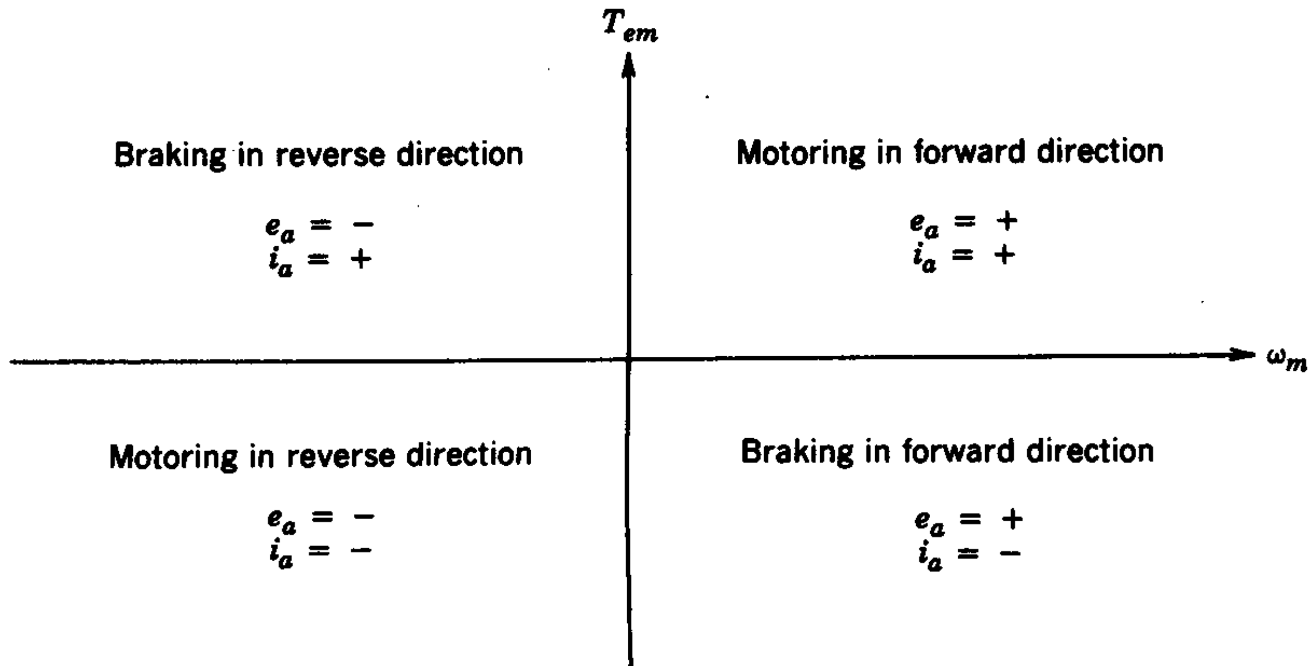

Figure 13-3 Four-quadrant operation of a dc motor.

- High performance drives may operate in all four quadrants

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DC-Motor Drive Torque-Speed Characteristics and Capabilities

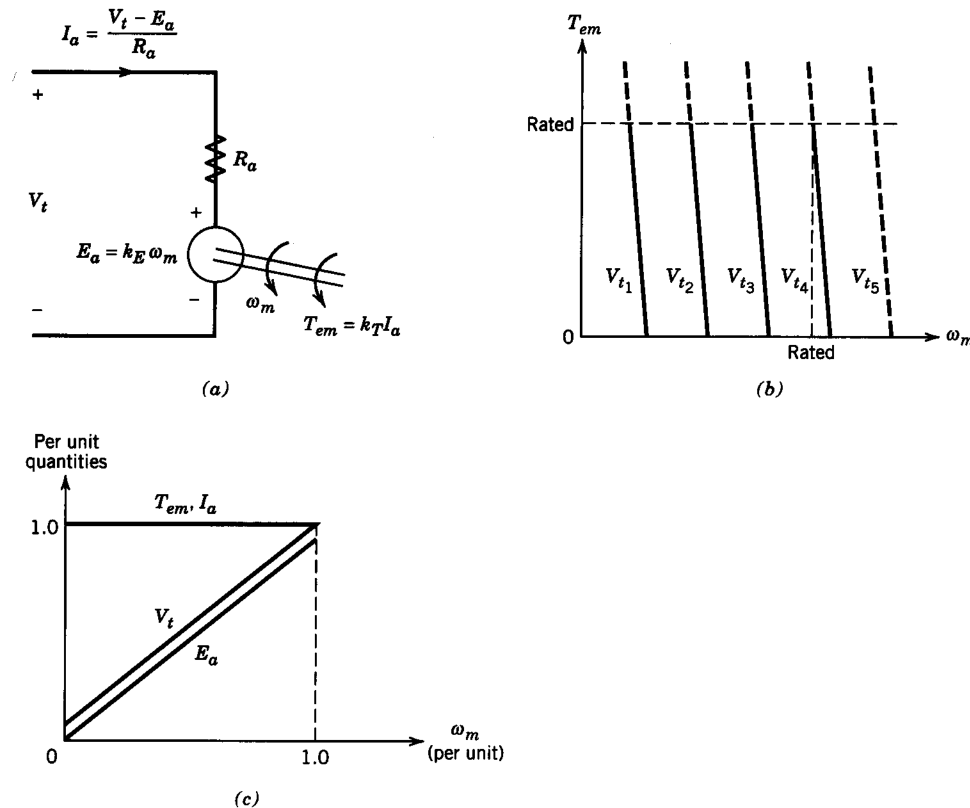

Figure 13-4 Permanent-magnet dc motor: (*a*) equivalent circuit; (*b*) torque-speed characteristics: $V_{t5} > V_{t4} > V_{t3} > V_{t2} > V_{t1}$, where V_{t4} is the rated voltage; (*c*) continuous torque–speed capability.

- With permanent magnets

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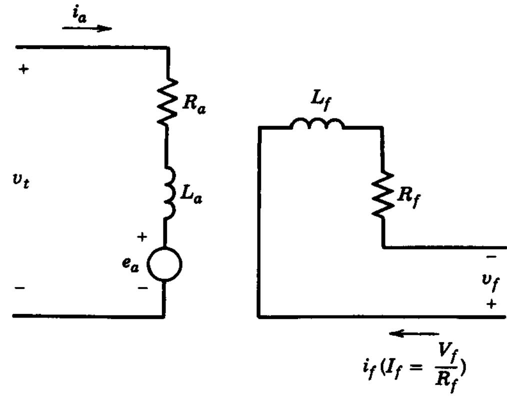
DC-Motor Drive Capabilities



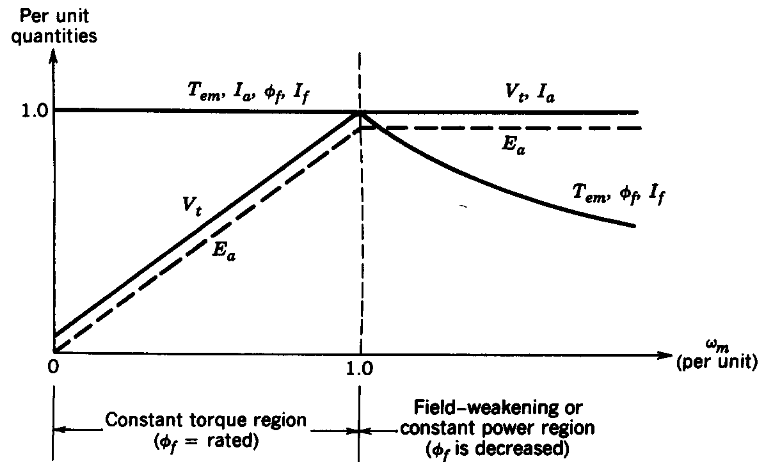


Figure 13-5 Separately excited dc motor: (*a*) equivalent circuit; (*b*) continuous torque–speed capability.

- Separately-Excited field

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Controlling Torque, Speed and Position

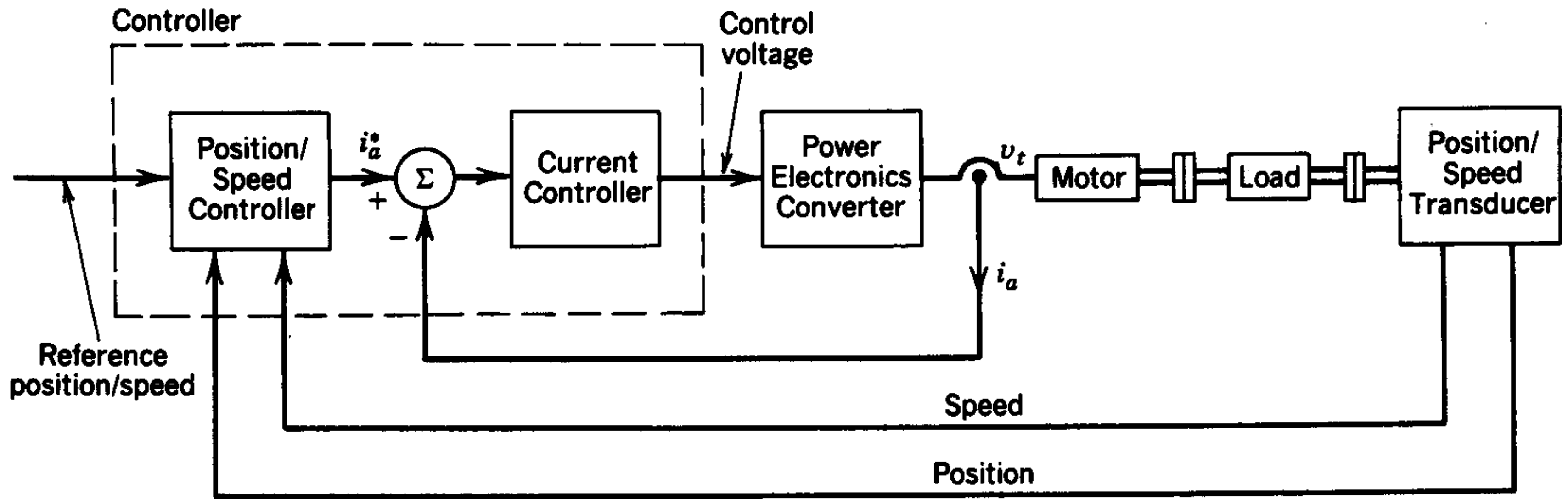

Figure 13-6 Closed-loop position/speed dc servo drive.

- Cascaded control is commonly used

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Small-Signal Representation of DC Machines

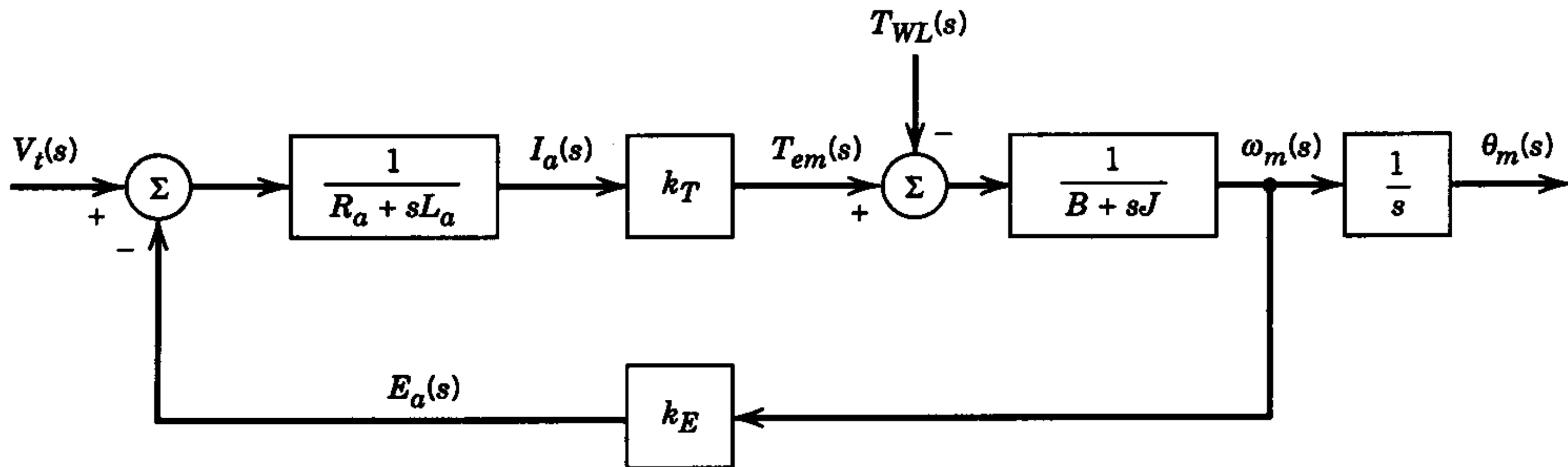

Figure 13-7 Block diagram representation of the motor and load (without any feedback).

- Around a steady state operating point

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Electrical Time-Constant of the DC Machine

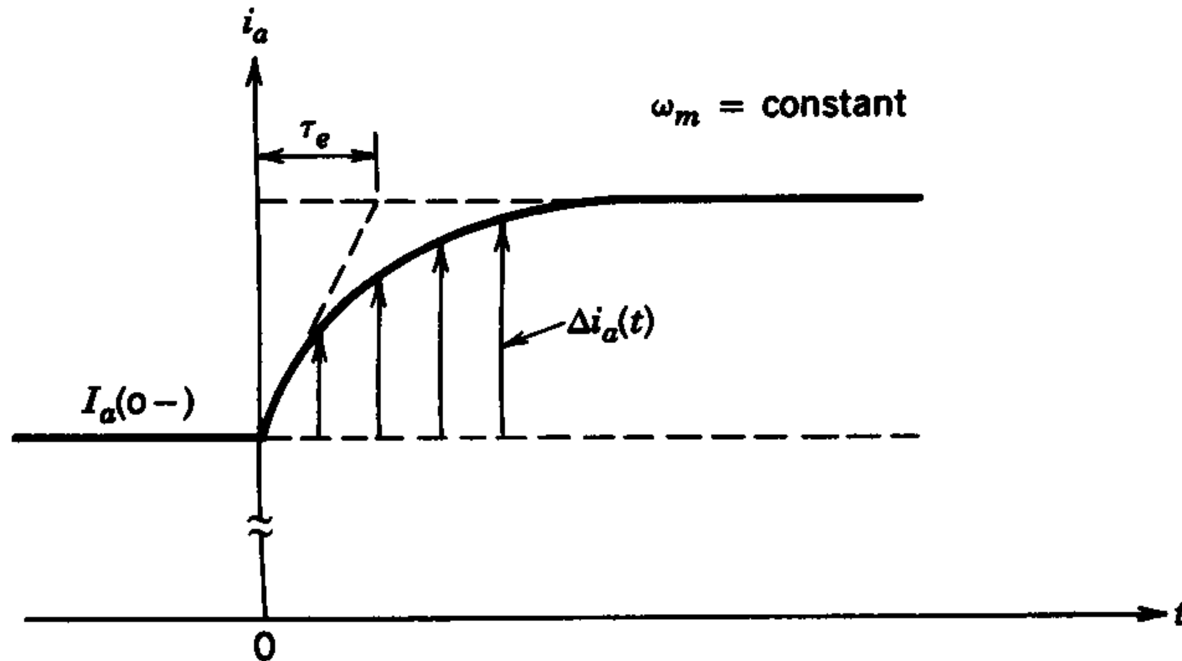

Figure 13-8 Electrical time constant τ_e; speed ω_m is assumed to be constant.

- The speed is assumed constant

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Mechanical Time-Constant of the DC Machine

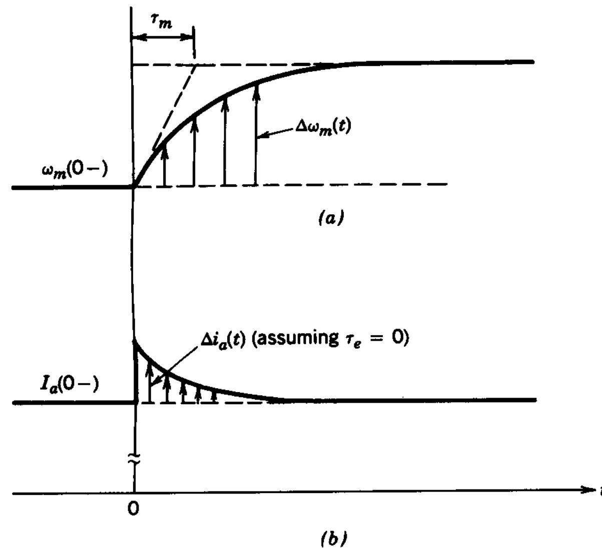

Figure 13-9
Mechanical time constant τ_m; load torque is assumed to be constant.

- The load-torque is assumed constant

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DC-Motor Drive: Four-Quadrant Capability

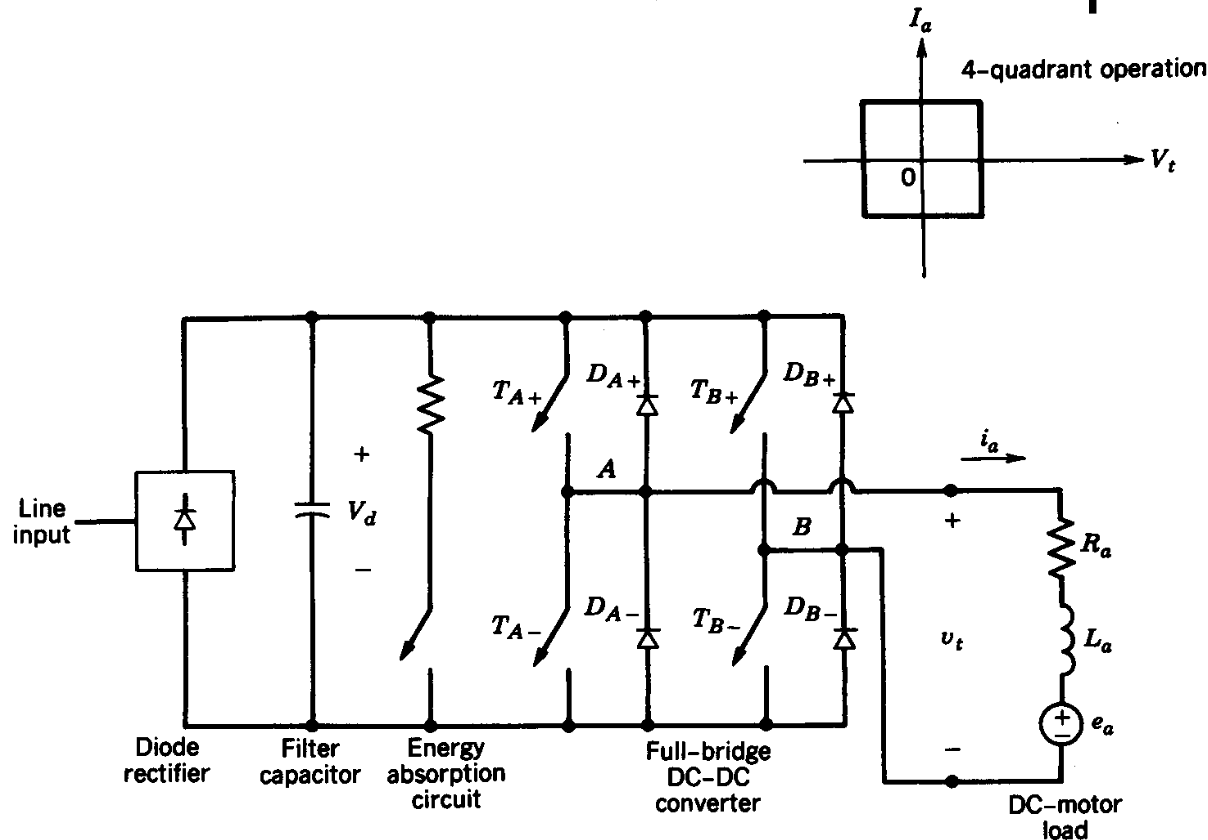

Figure 13-10 A dc motor servo drive; four-quadrant operation.

- If a diode-rectifier is used, the energy recovered during regenerative braking is dissipated in a resistor

Ripple in the Armature Current

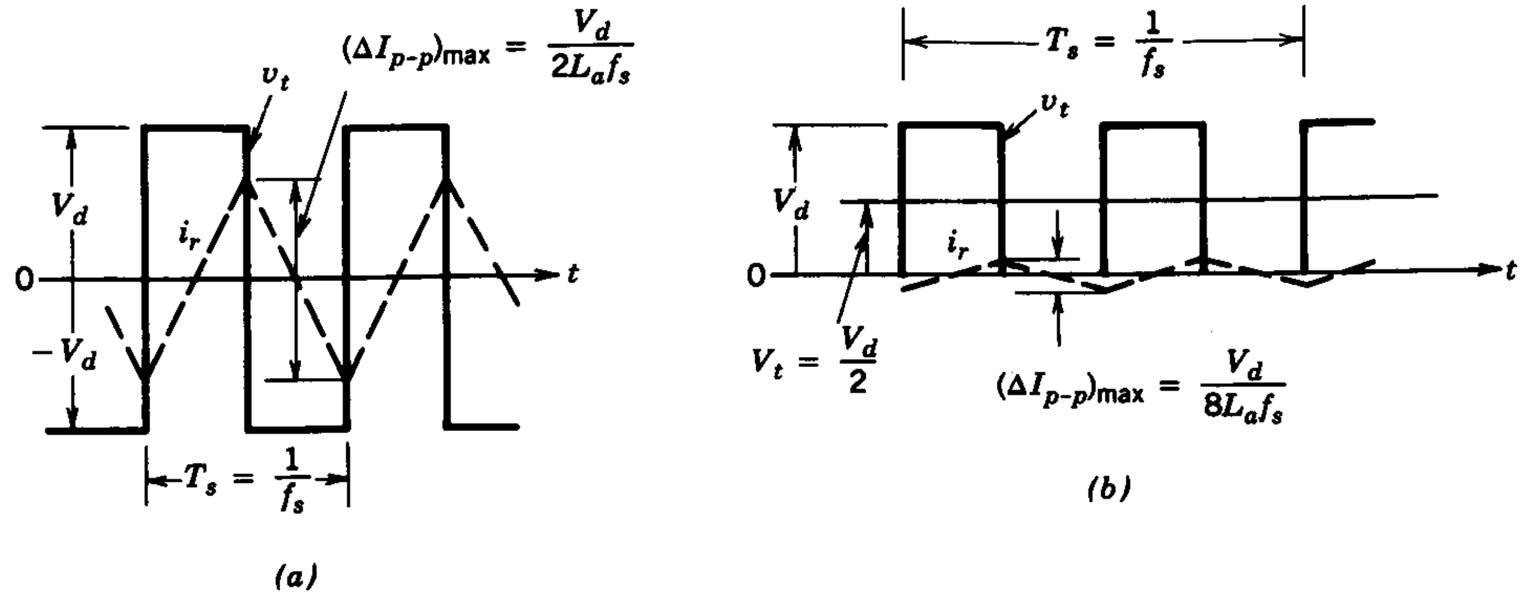

Figure 13-11 Ripple i_r in the armature current: (*a*) PWM bipolar voltage switching, $V_t = 0$; (*b*) PWM unipolar voltage switching, $V_t = ½V_d$.

- Bi-polar and uni-polar voltage switchings

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Control of Servo Drives

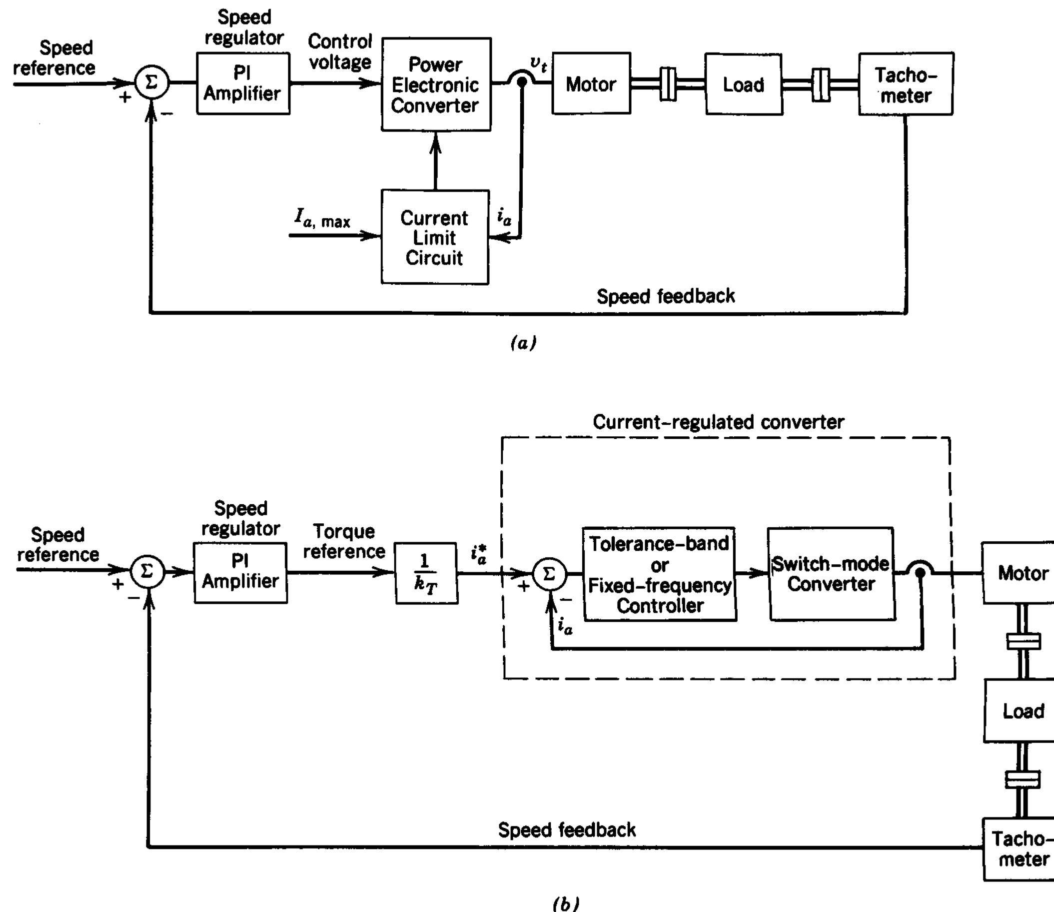

Figure 13-12 Control of servo drives: (*a*) no internal current-control loop; (*b*) internal current-control loop.

- A concise coverage is presented in "Electric Drives: An Integrative Approach" by N. Mohan (www.MNPERE.com)

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Effect of Blanking Time

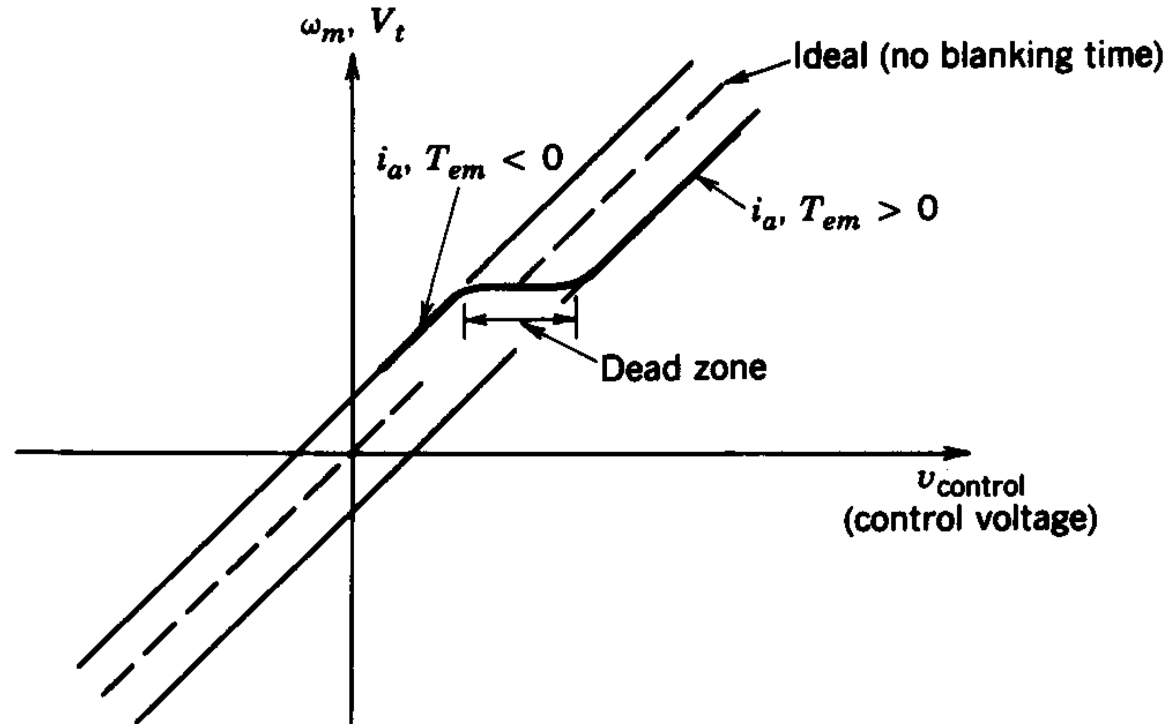

Figure 13-13 Effect of blanking time.

- Non-linearity is introduced

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Converters for Limited Operational Capabilities

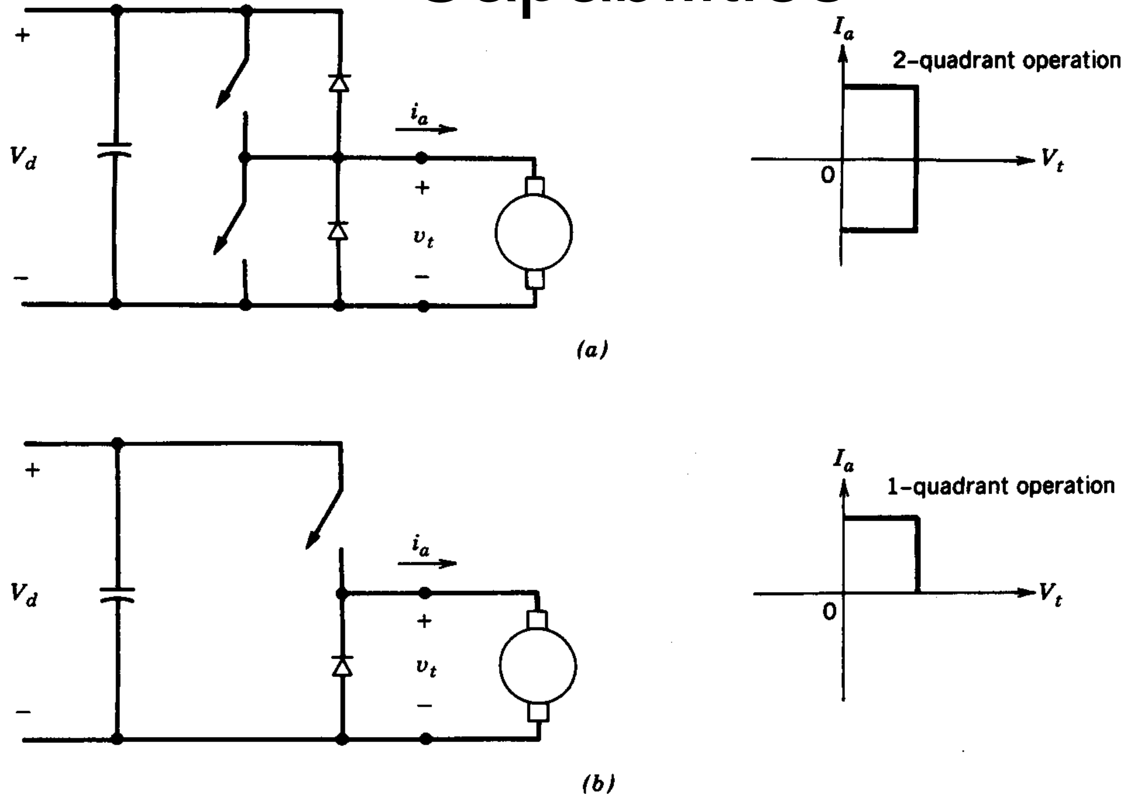

Figure 13-14 (*a*) Two-quadrant operation; (*b*) single-quadrant operation.

- Two switches for 2-quadrant operation and only one switch for 1-quadrant operation

Line-Controlled Converters for DC Drives

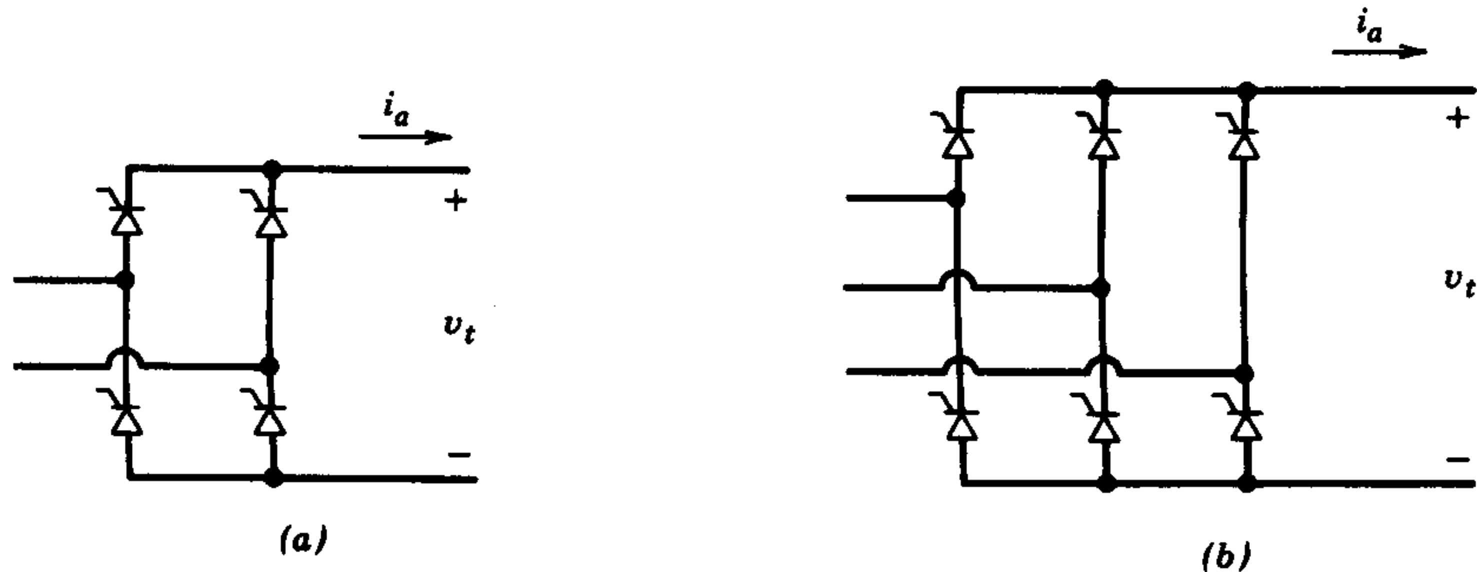

Figure 13-15 Line-frequency-controlled converters for dc motor drives: (*a*) single-phase input; (*b*) three-phase input.

- Large low-frequency ripple in the dc output of converters

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Four Quadrant Operation using Line Converters

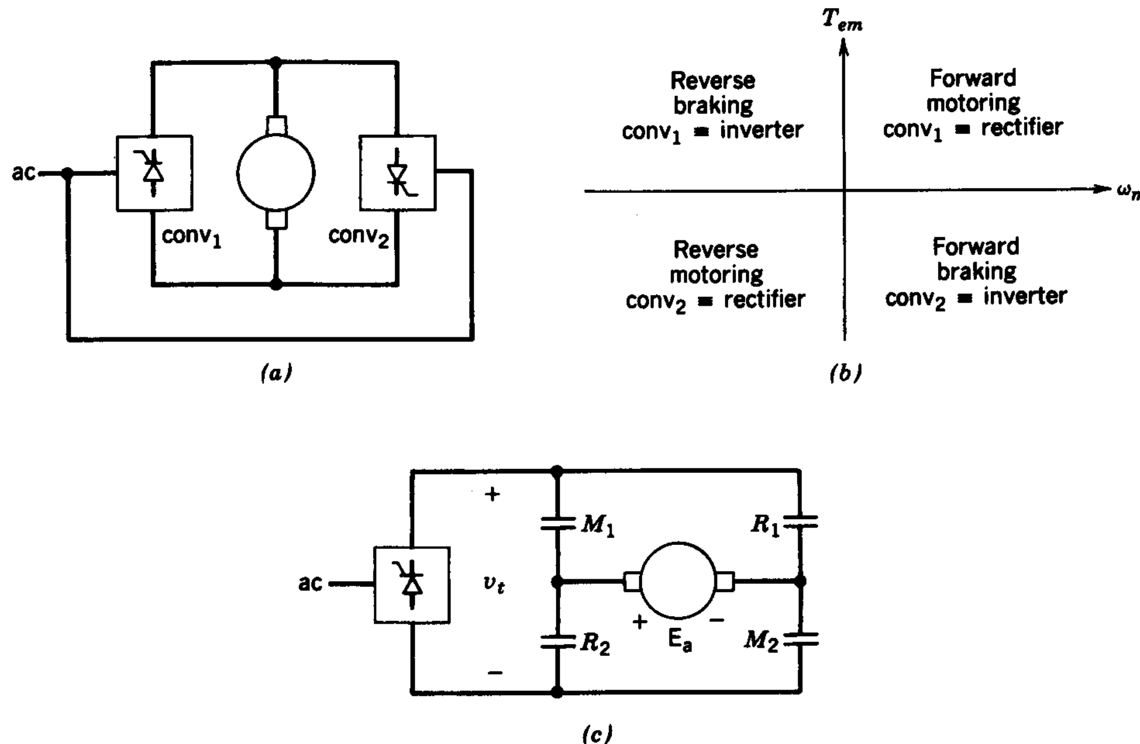

Figure 13-16 Line-frequency-controlled converters for four-quadrant operation: (*a*) back-to-back converters for four-quadrant operation (without circulating current); (*b*) converter operation modes; (*c*) contactors for four-quadrant operation.

- Two options to achieve 4-quadrant operation

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Effect of Discontinuous Current Conduction

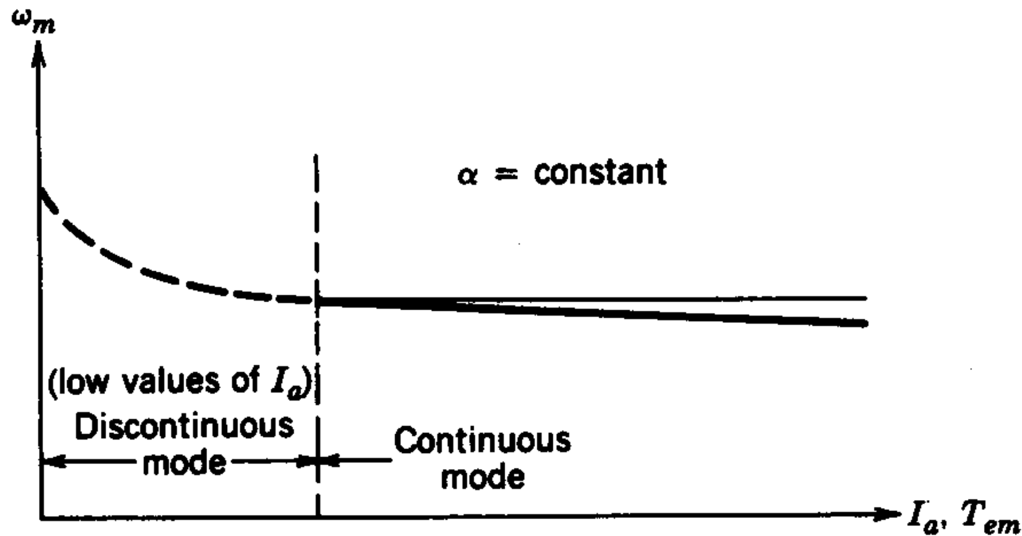

Figure 13-17 Effect of discontinuous i_a on ω_m.

- Speed goes up unless it is controlled

Open-Loop Speed Control

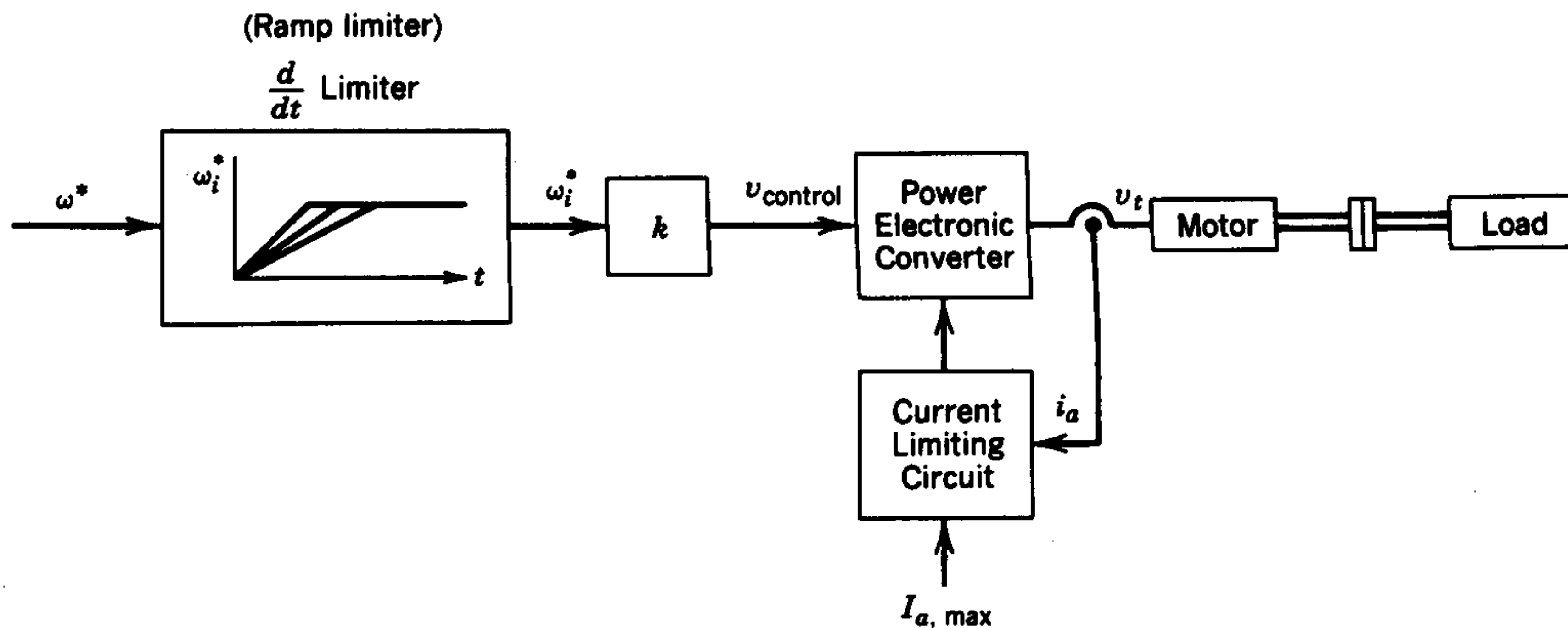

Figure 13-18 Open-loop speed control.

- Adequate for general-purpose applications

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DC Drive Characteristics and Capabilities

• Line current in switch-mode and line-converter drives

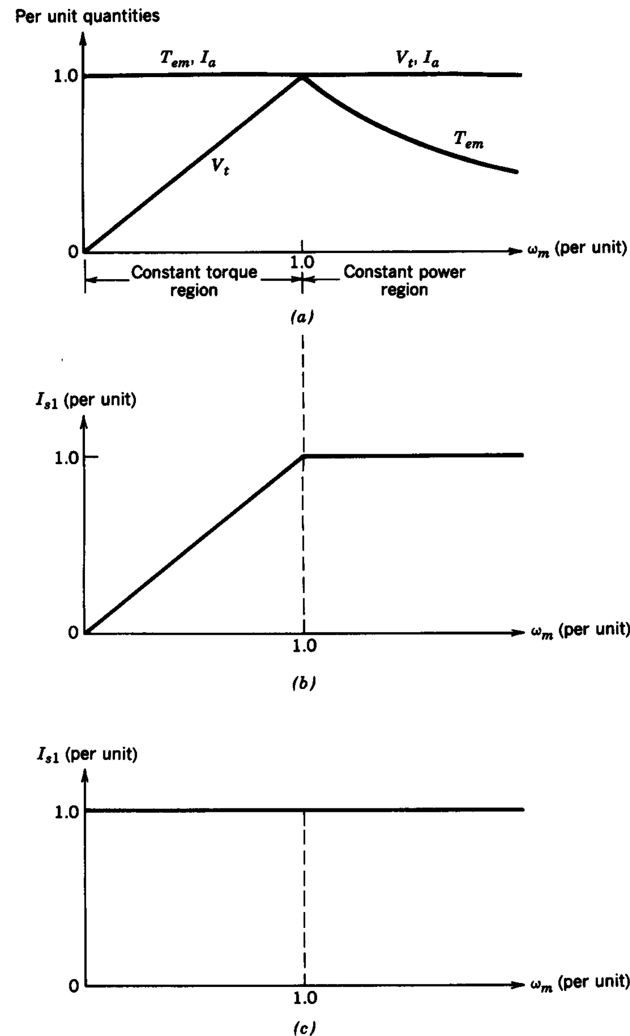

Figure 13-19 Line current in adjustable-speed dc drives: (*a*) drive capability; (*b*) switch-mode converter drive; (*c*) line-frequency thyristor converter drive.

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Chapter 14

Induction Motor Drives

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- Extremely large potential as adjustable speed drives

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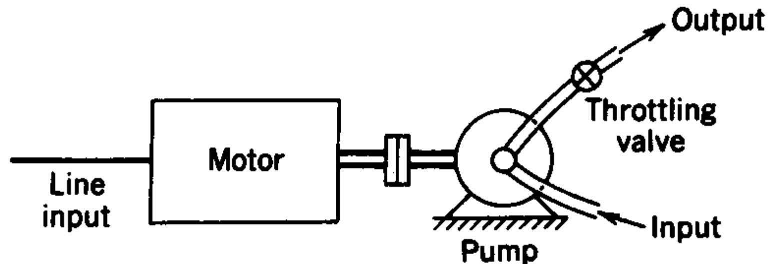
Pump Application: Adjustable Flow rate



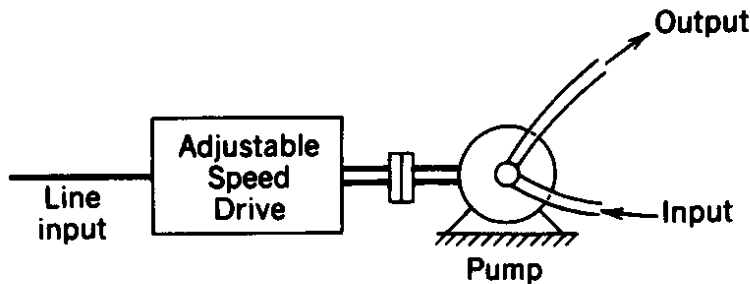


Figure 14-1 Centrifugal pump: (*a*) constant-speed drive: (*b*) adjustable-speed drive.

- Fixed versus adjustable speed drive

Per-Phase Representation

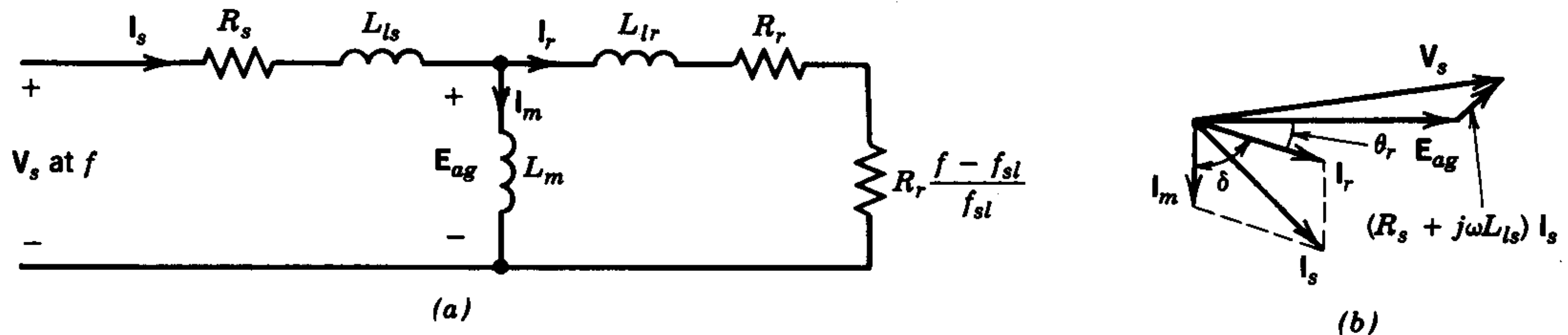


Figure 14-2 Per-phase representation: (*a*) equivalent circuit; (*b*) phasor diagram.

- Assuming sinusoidal steady state

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Important Relationships in an Induction Machine

Table 14-1 Important Relationships

$\omega_s = k_7 f$
$s = \dfrac{\omega_s - \omega_r}{\omega_s}$
$f_{sl} = sf$
$\%P_r = \dfrac{f_{sl}}{f - f_{sl}}$
$V_s \simeq k_3 \phi_{ag} f$
$I_r \simeq k_5 \phi_{ag} f_{sl}$
$T_{em} \simeq k_6 \phi_{ag}^2 f_{sl}$
$I_m = k_8 \phi_{ag}$ (from Eq. 14-5)
$I_s \simeq \sqrt{I_m^2 + I_r^2}$

- Not necessary for our purposes to know the exact expressions for constants used here

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Torque-Speed Characteristics

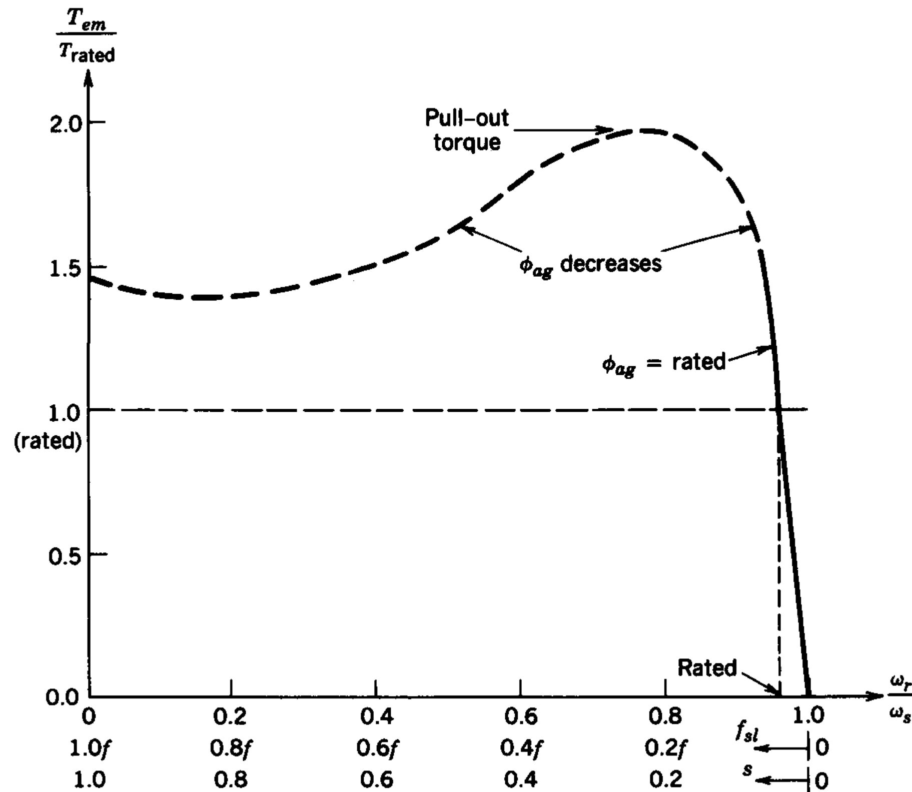

Figure 14-3 A typical torque–speed characteristic; V_s and f are constant at their rated values.

- The linear part of the characteristic is utilized in adjustable speed drives

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Plot of Normalized Rotor Current

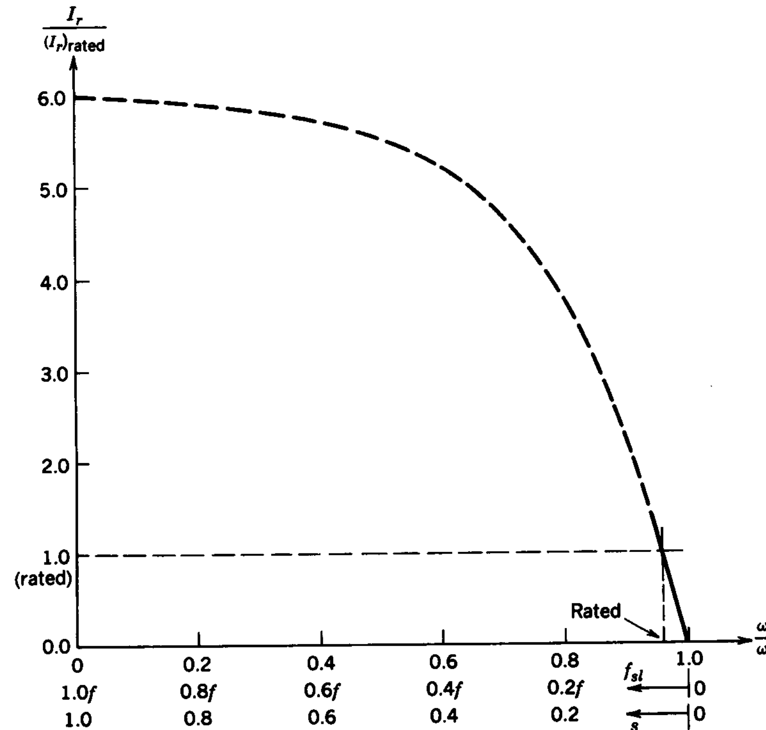

Figure 14-4 Plot of I_r versus f_{sl}; V_s and f are constant at their rated values.

- It increases with slip and slip frequency

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Acceleration Torque at Startup

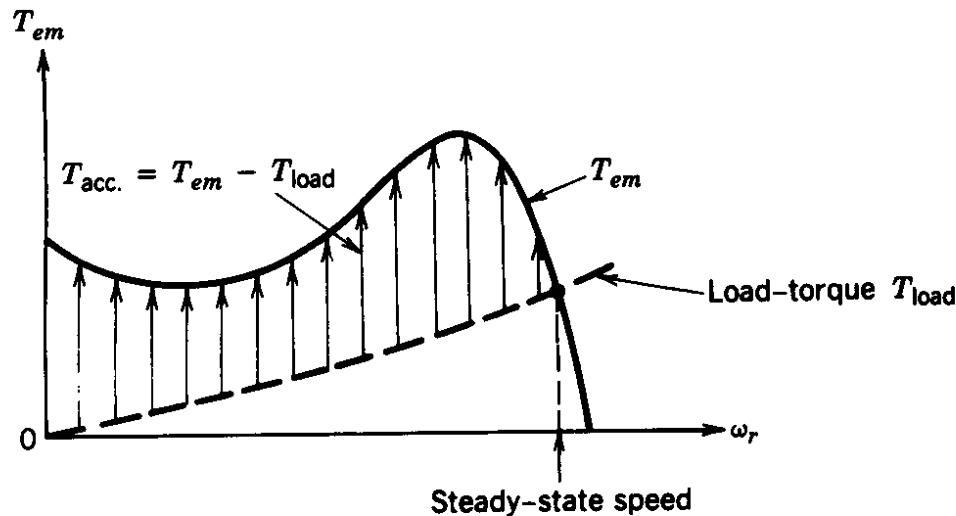

Figure 14-5 Motor start-up; V_s and f are constant at their rated values.

- Intersection represents the equilibrium point

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Torque Speed Characteristics at various Frequencies of Applied Voltage

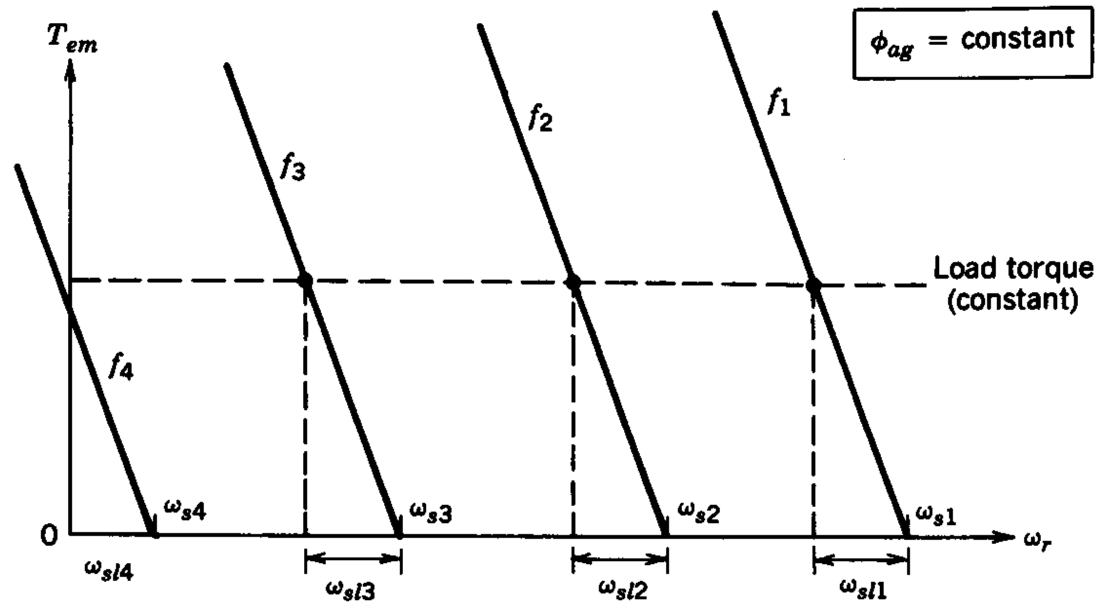

Figure 14-6 Torque–speed characteristics at small slip with a constant ϕ_{ag}; constant load torque.

- The air gap flux is kept constant

Adjusting Speed of a Centrifugal Load

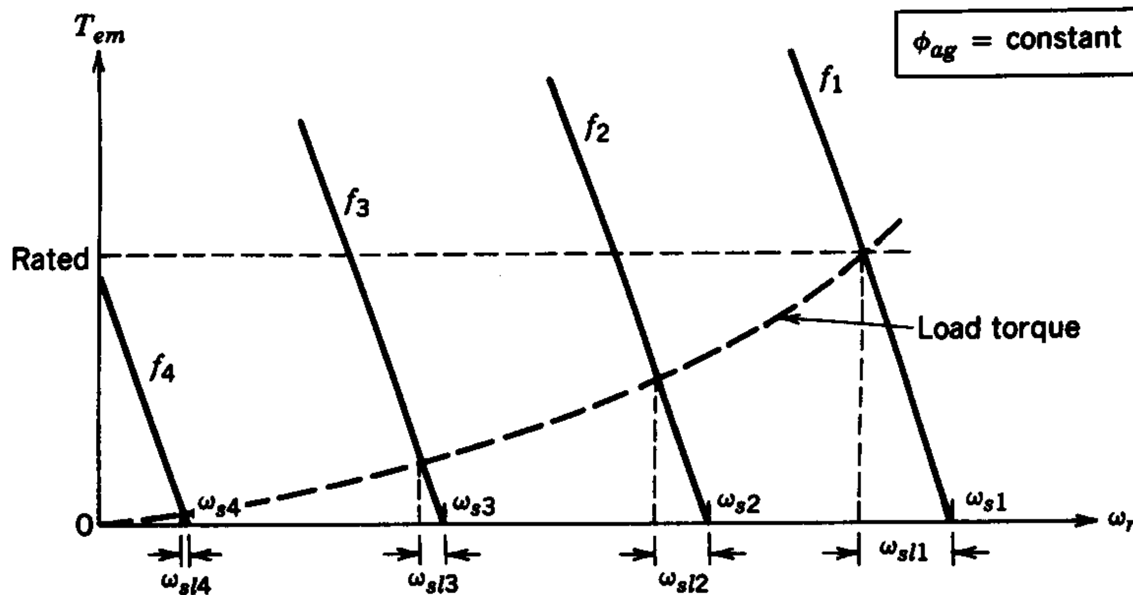

Figure 14-7 Centrifugal load torque; torque varies as the speed squared.

- The load torque is proportional to speed squared

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Frequency at Startup

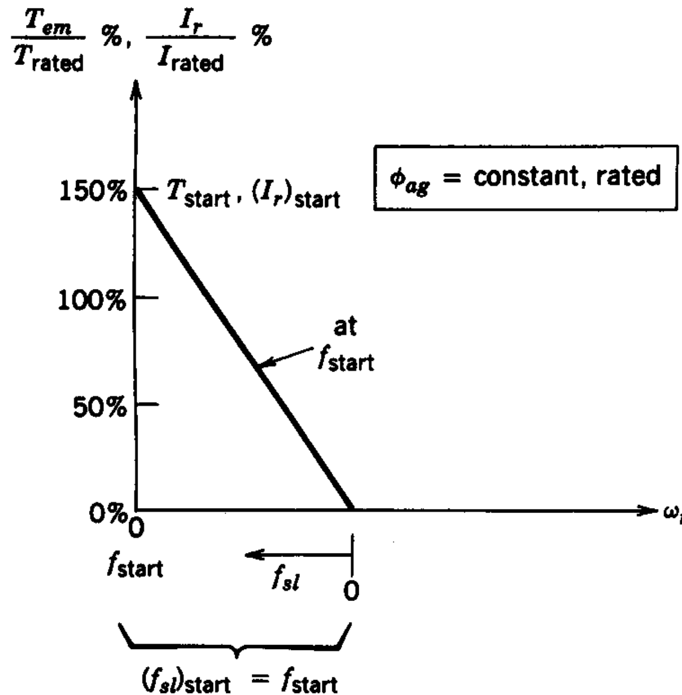

Figure 14-8 Frequency at start-up.

- The torque is limited to limit current draw

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Increasing Speed at Startup

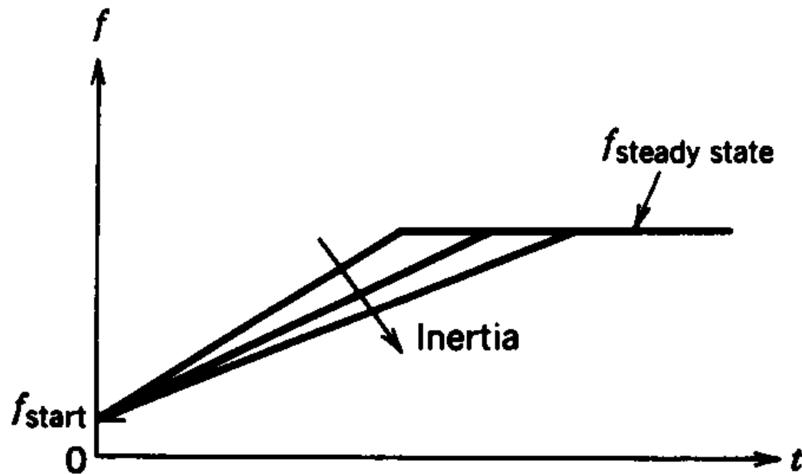

Figure 14-9 Ramping of frequency f at start-up.

- The ramp rate of frequency depends on load inertia

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Phasor Diagram at Small Value of Slip Frequency

Figure 14-10 Phasor diagram at a small value of f_{sl}.

- The rotor branch is assumed to be purely resistive

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Voltage Boost to Keep Air Gap Flux at its Rated Value

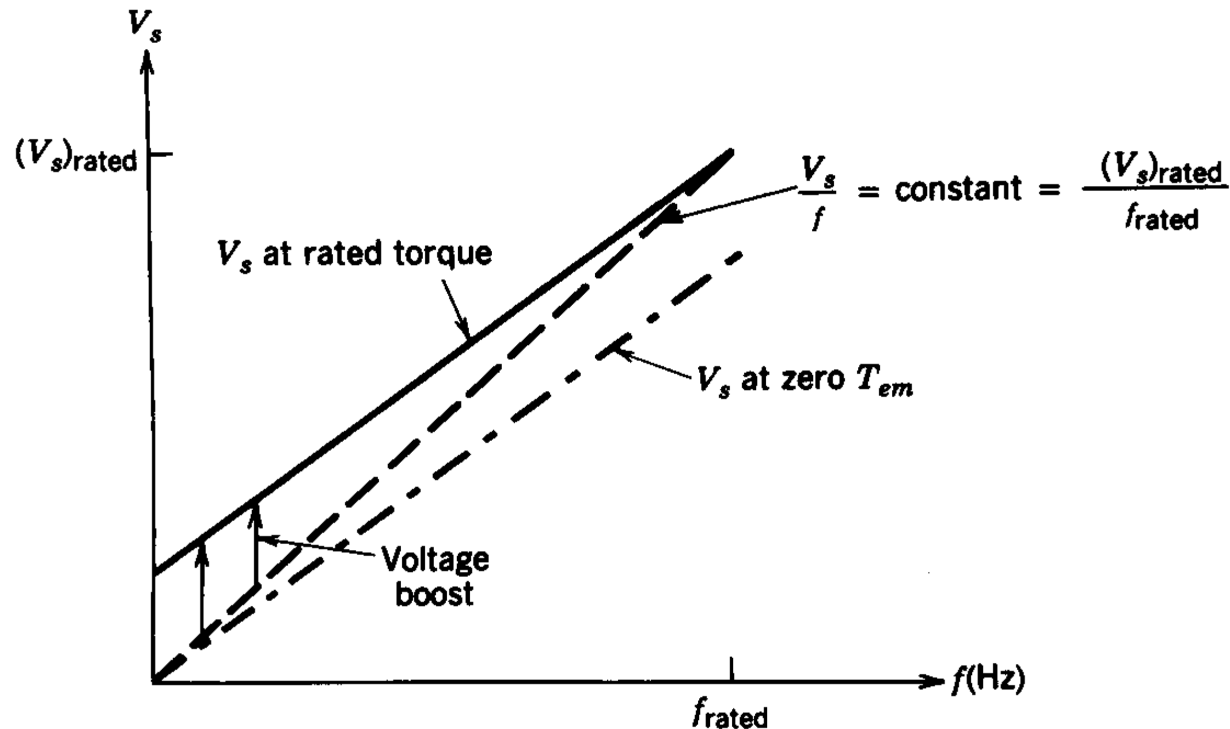

Figure 14-11 Voltage boost required to keep ϕ_{ag} constant.

- Depends on the torque loading of the machine

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Induction Motor Drive Capability Curves

- Mainly two regions

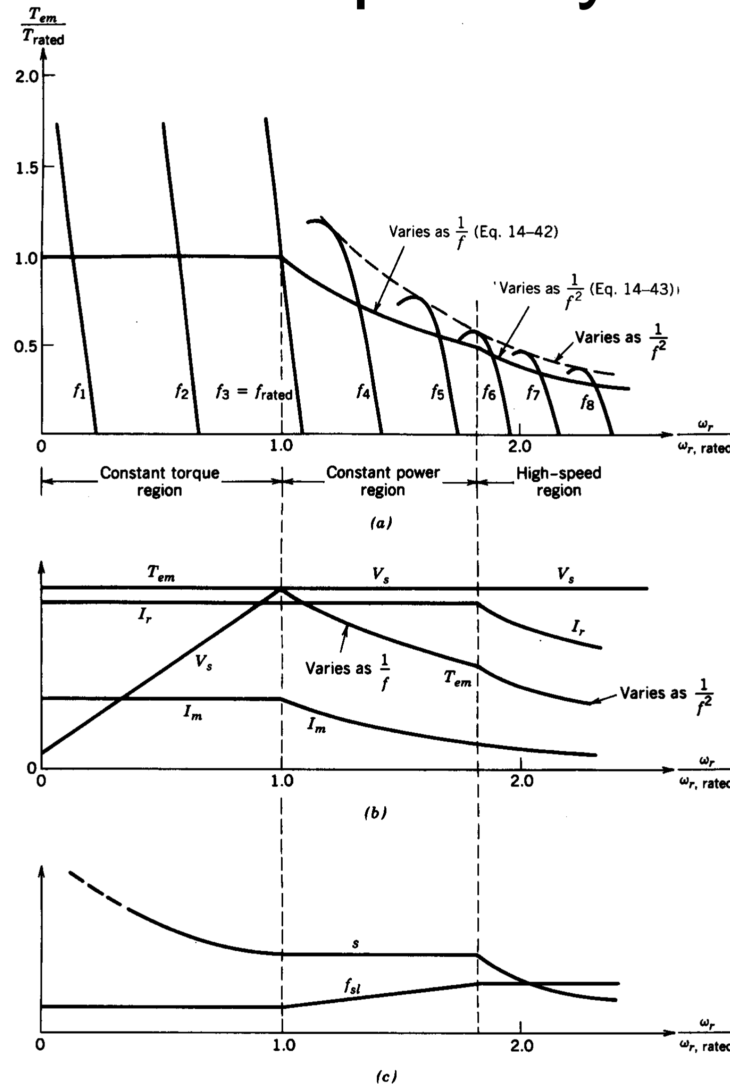

Figure 14-12 Induction motor characteristics and capabilities.

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Generator Mode of Operation

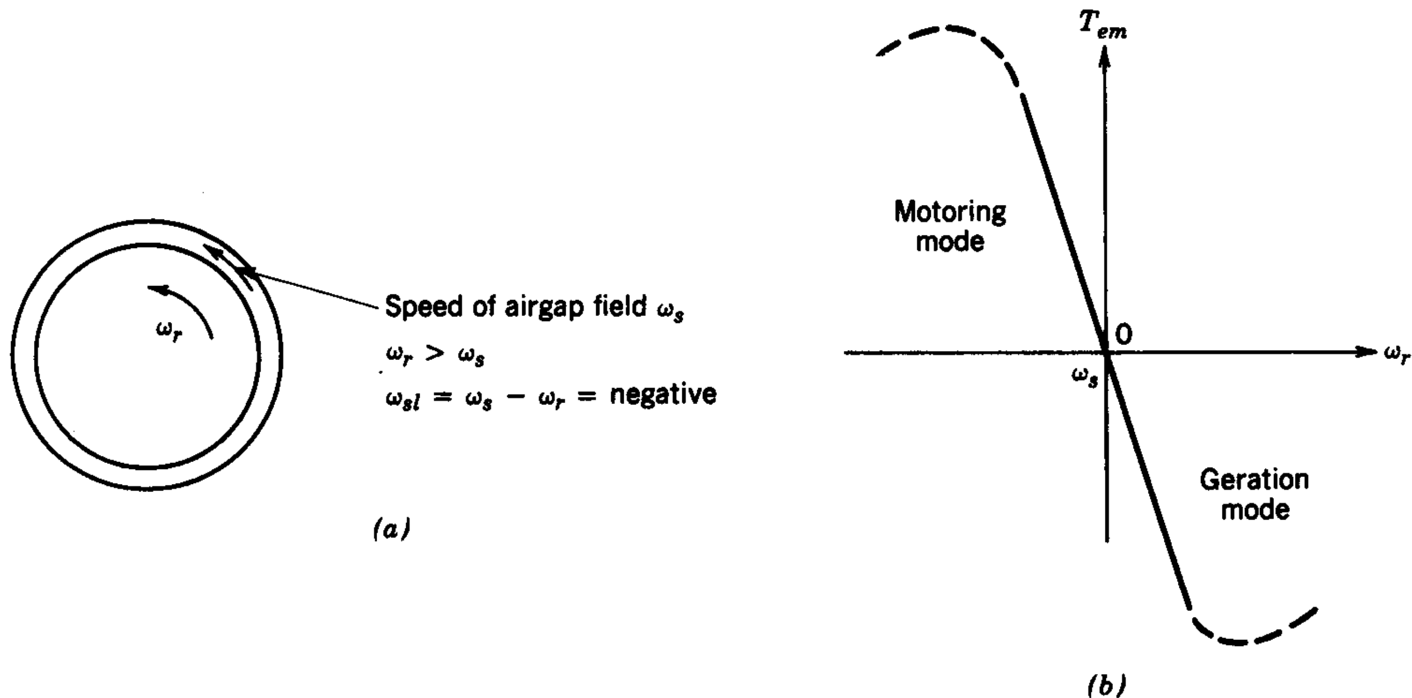

Figure 14-13 Generation mode.

- Rotor speeds exceed the synchronous speed

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Regenerative Braking Mode to Slow Down

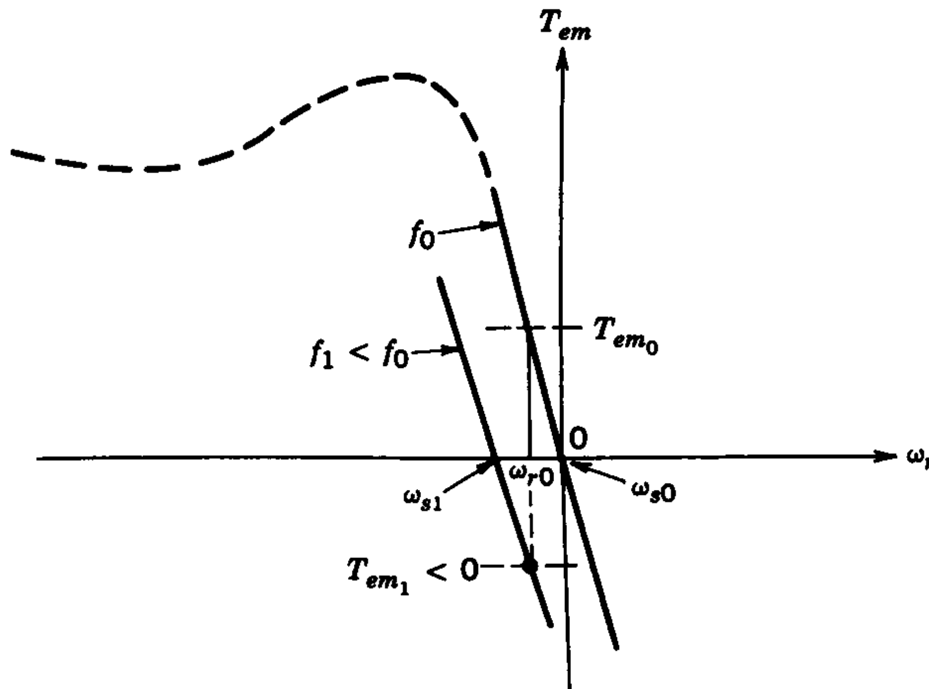

Figure 14-14 Braking (initial motor speed is ω_{r0} and the applied frequency is instantaneously decreased from f_0 to f_1).

- Machine is made to go into the generator mode

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Per-Phase Equivalent Circuit at Harmonic Frequencies

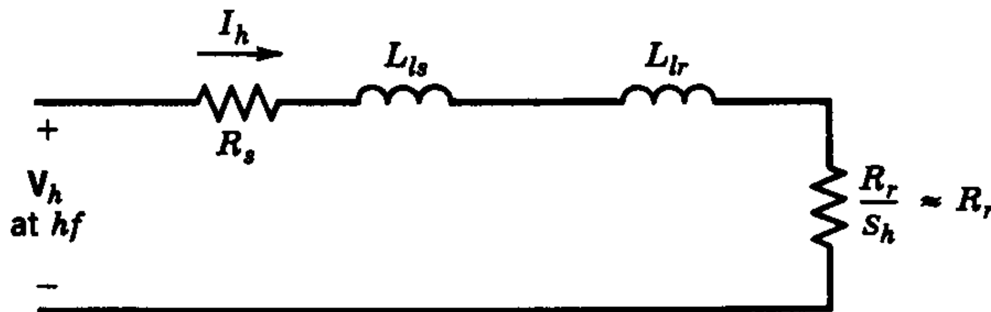

Figure 14-15 Per-phase harmonic equivalent circuit.

- The magnetizing branch is ignored

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Torque Pulsations due to Harmonics

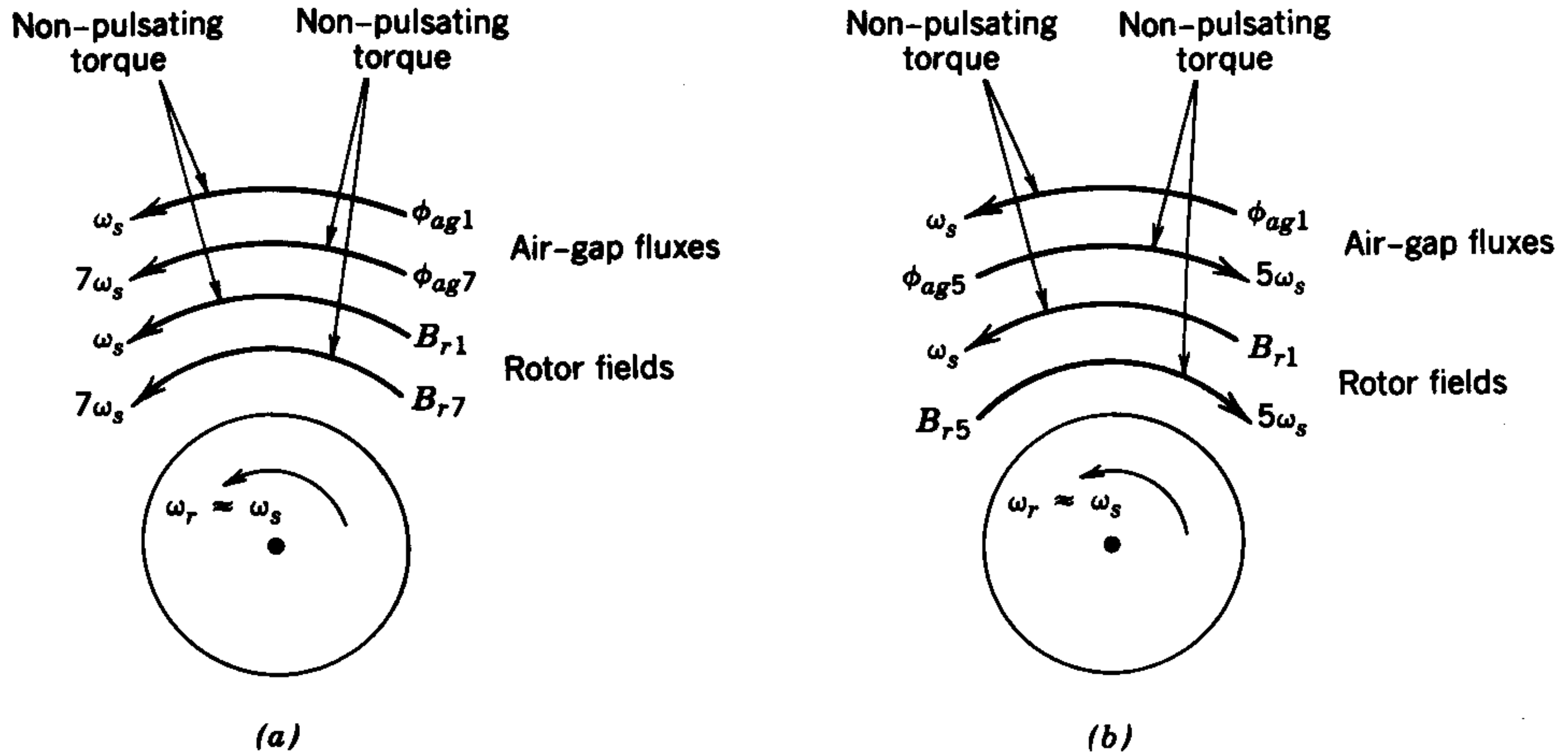


Figure 14-16 Torque pulsations: (*a*) seventh harmonic; (*b*) fifth harmonic.

- Rotations of fields due to the fifth and the seventh harmonics are in opposite directions

Classification of Converter Systems

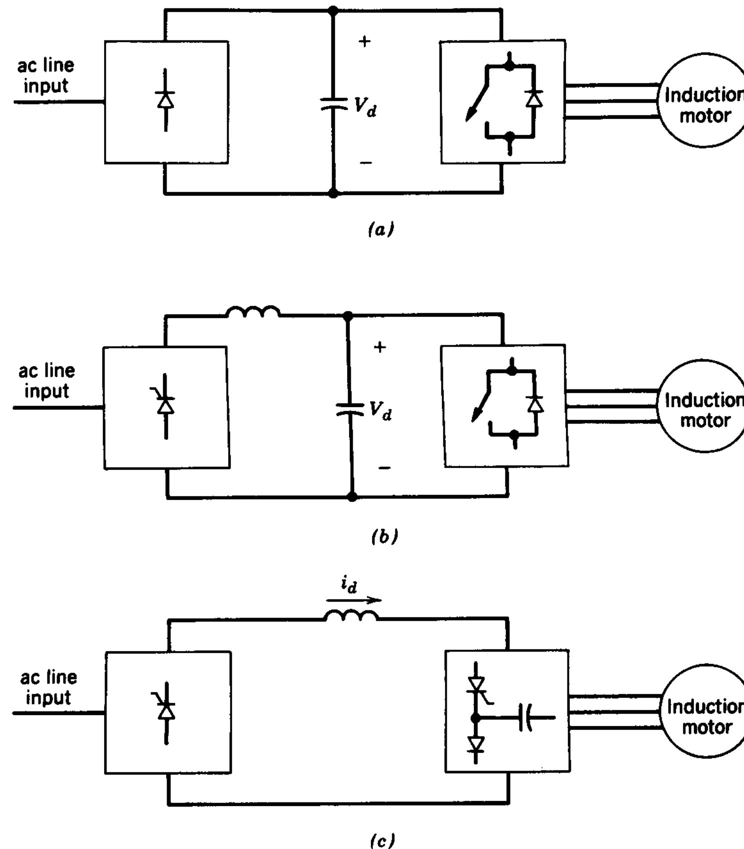
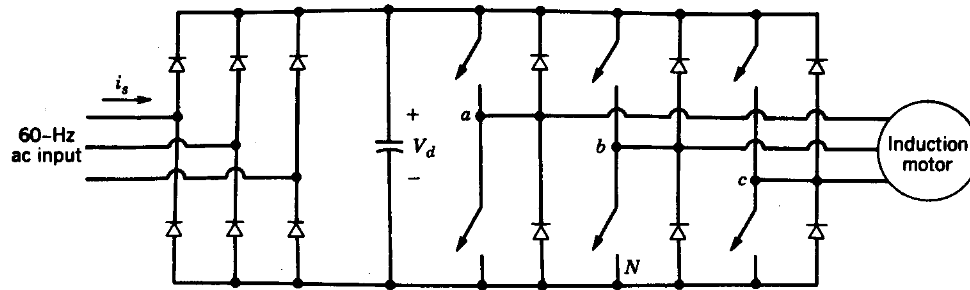


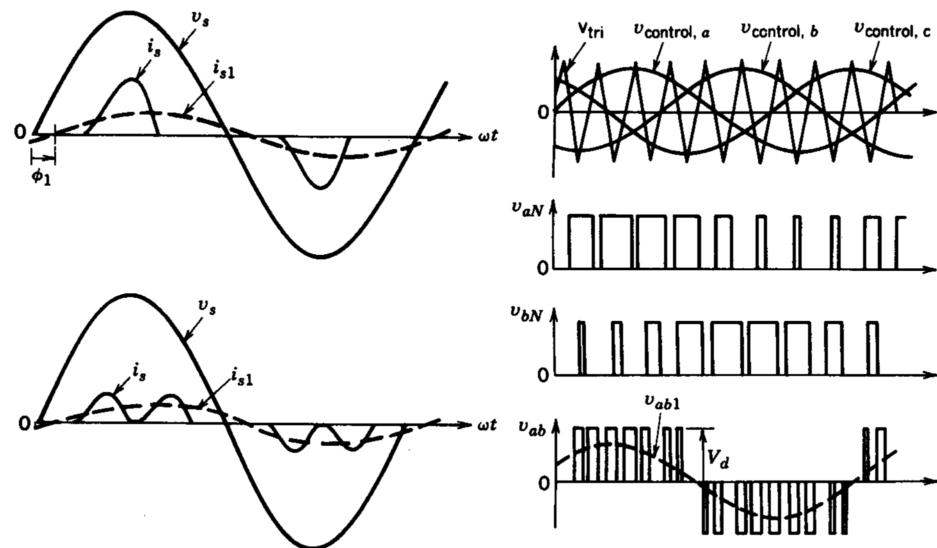
Figure 14-18 Classification of variable-frequency converters: (*a*) PWM-VSI with a diode rectifier; (*b*) square-wave VSI with a controlled rectifier; (*c*) CSI with a controlled rectifier.

- PWM-VSI is now most commonly use

PWM-VSI System



(a)



(b)

Figure 14-19 PWM-VSI: (*a*) schematic; (*b*) waveforms.

- Diode rectifier for unidirectional power flow

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PWM-VSI System

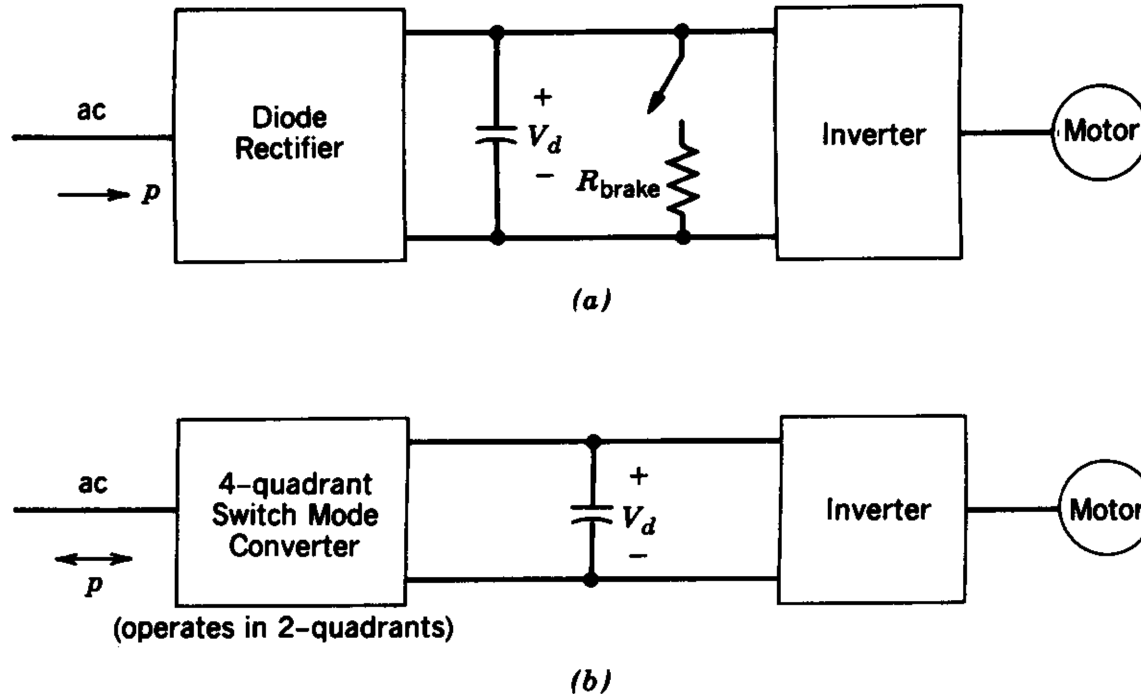

Figure 14-20 Electromagnetic braking in PWM-VSI: (*a*) dissipative braking; (*b*) regenerative braking.

- Options for recovered energy during regenerative braking

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General-Purpose Speed Controller

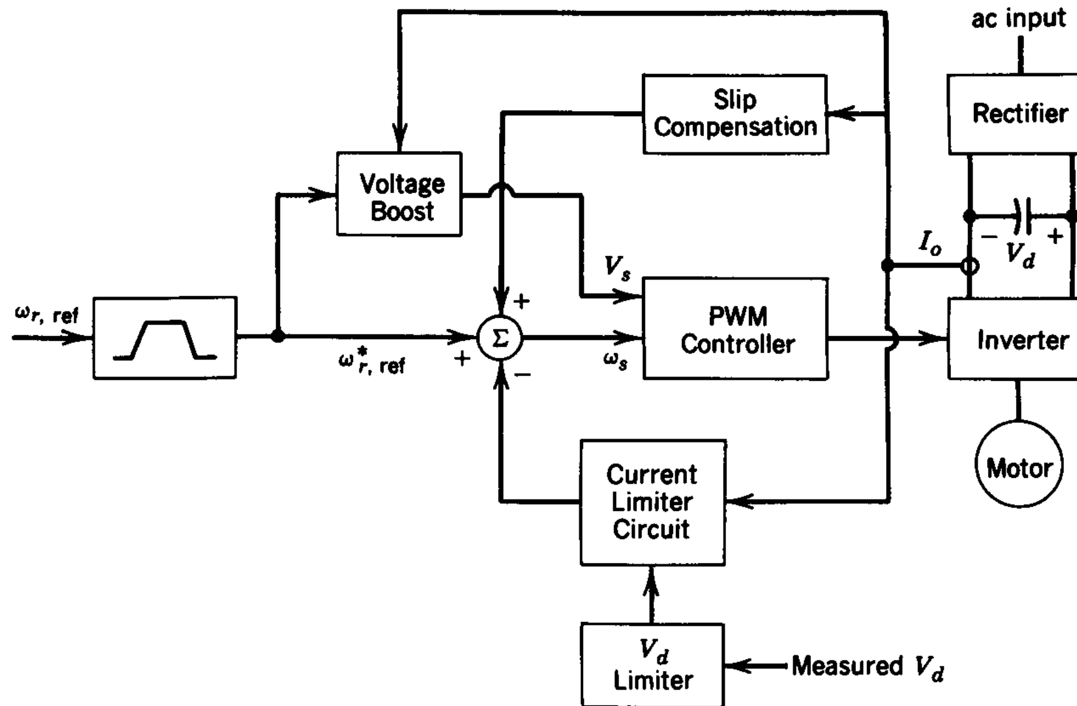

Figure 14-21 Speed control circuit. Motor speed is not measured.

- High dynamic performance is not the objective here

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Change in Switching Frequency based on the required Fundamental Frequency

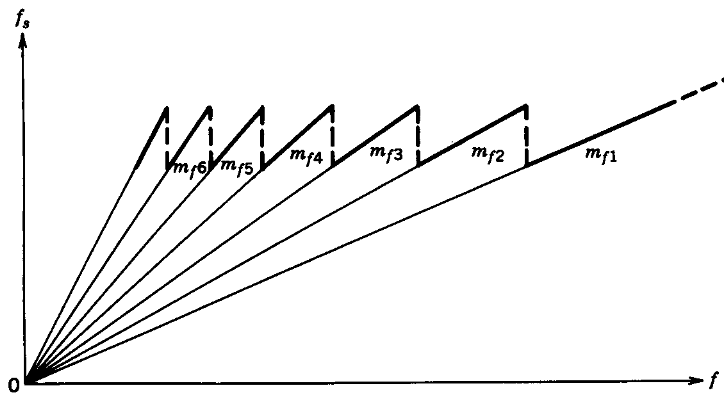

Figure 14-22 Switching frequency versus the fundamental frequency.

- Can be significant in large power ratings

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Field-Oriented Control

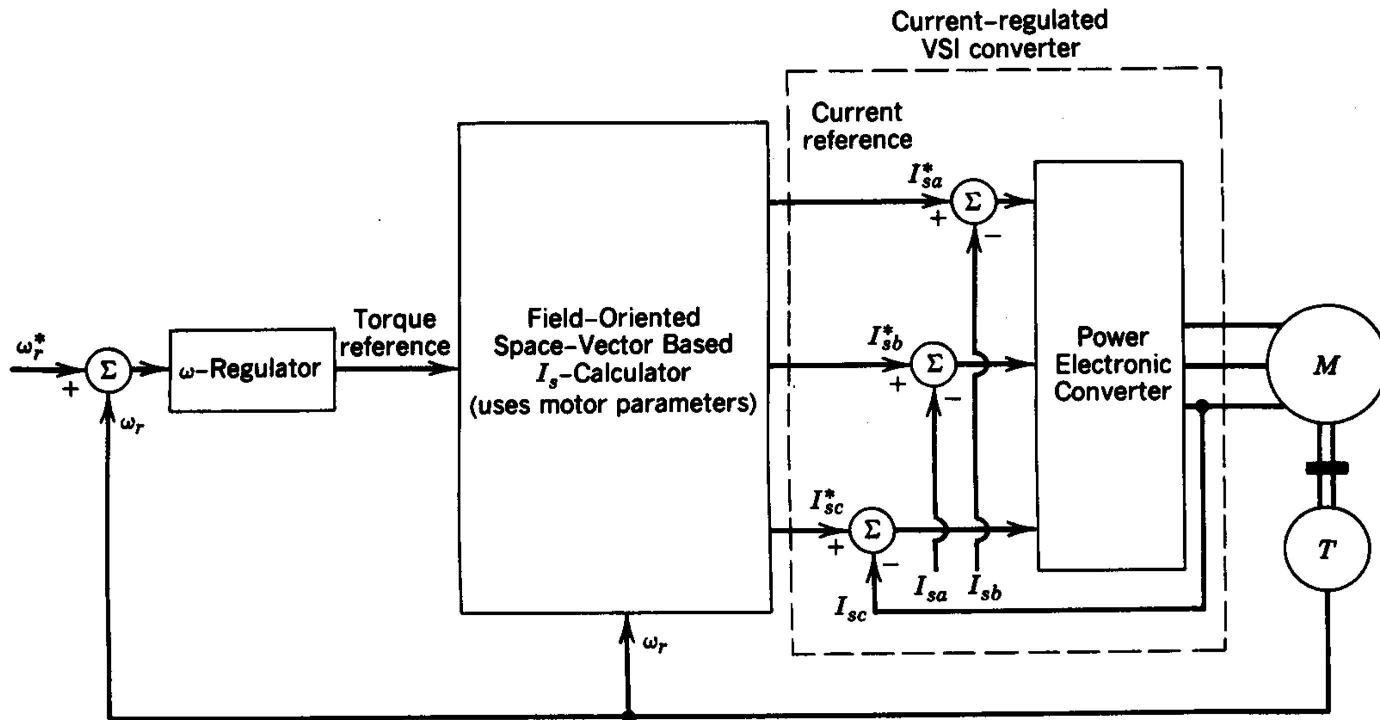

Figure 14-23 Field-oriented control for induction motor servo drive.

- A concise coverage is presented in "Advanced Electric Drives: Analysis, Control and Modeling using Simulink" by N. Mohan (www.MNPERE.com)

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Square-Wave VSI Waveforms

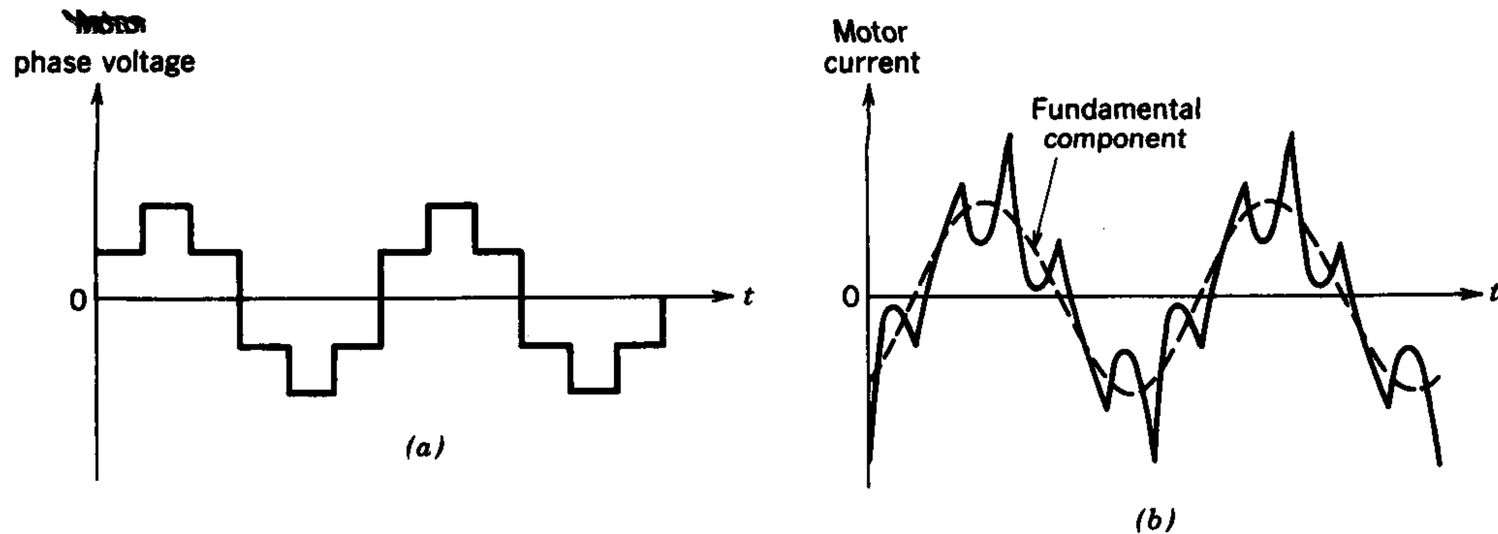

Figure 14-24 Square-wave VSI waveforms.

- Large peak-peak ripple in currents

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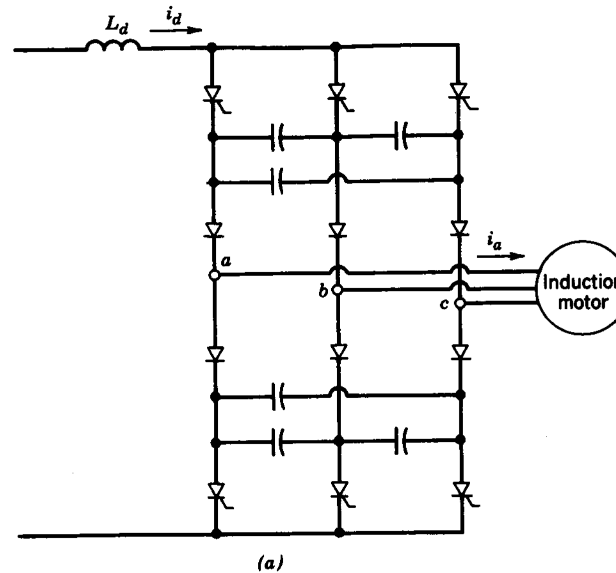
CSI Drives



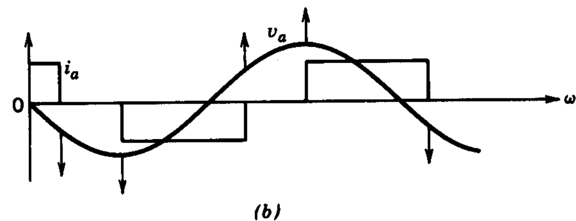


Figure 14-25 CSI drive: (*a*) inverter; (*b*) idealized phase waveforms.

- Mostly PWM-VSI drives are used

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Comparison of Three Types of Inverter Systems

Table 14-2 Comparison of Adjustable Frequency Drives

Parameter	*PWM*	*Square Wave*	*CSI*
Input power factor	+	−	−−
Torque pulsations	++	−	−
Multimotor capability	+	+	−
Regeneration	−	−	++
Short-circuit protection	−	−	++
Open-circuit protection	+	+	−
Ability to handle undersized motor	+	+	−
Ability to handle oversized motor	−	−	−
Efficiency at low speeds	−	+	+
Size and weight	+	+	−−
Ride-through capability	+	−	−

- PWM-VSI is by far the most commonly selected system now

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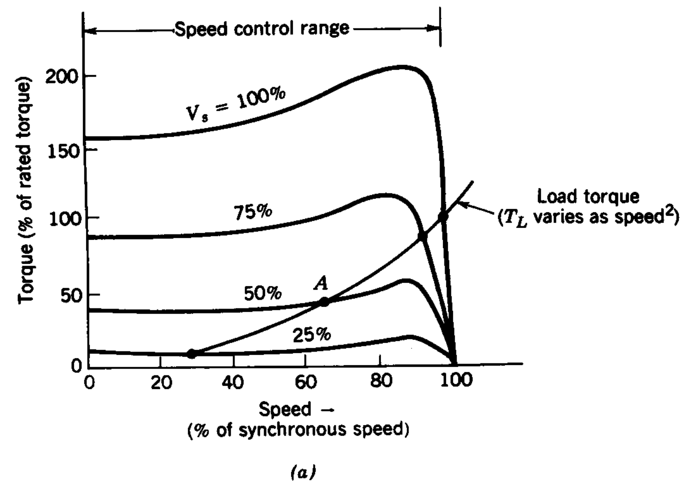
Speed Control by Adjusting the Stator Voltage



- Highly inefficient in most cases

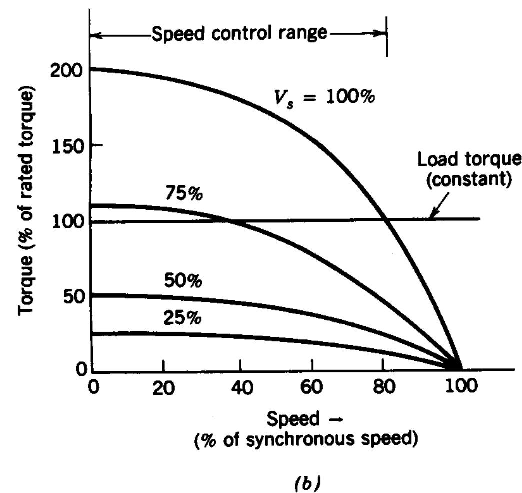


Figure 14-26 Speed control by stator voltage control: (*a*) motor with a low value of s_{rated}, fan-type load; (*b*) motor with a large s_{rated}, constant-torque load.

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Controlling the Stator Voltage Magnitude

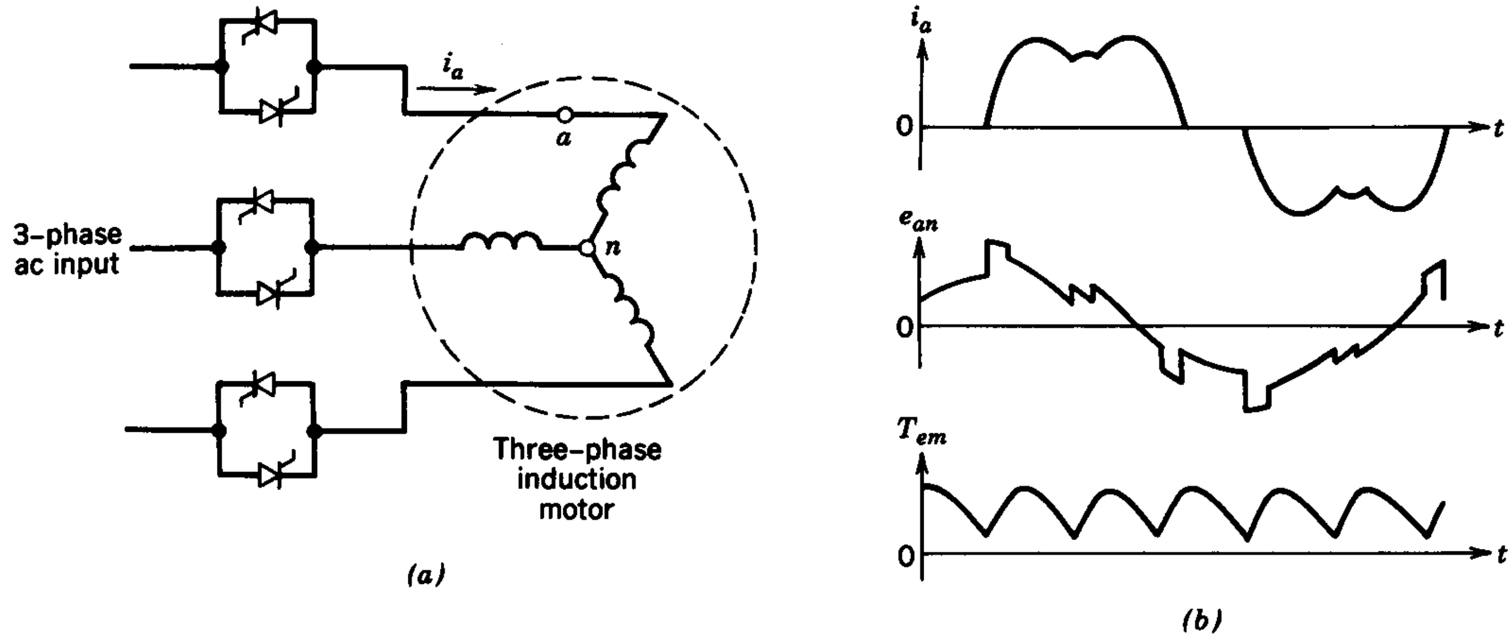

Figure 14-27 Stator voltage control: (*a*) circuit; (*b*) waveforms.

- Results in distorted current and torque pulsations

Torque-Speed Curves for Wound-Rotor Machines

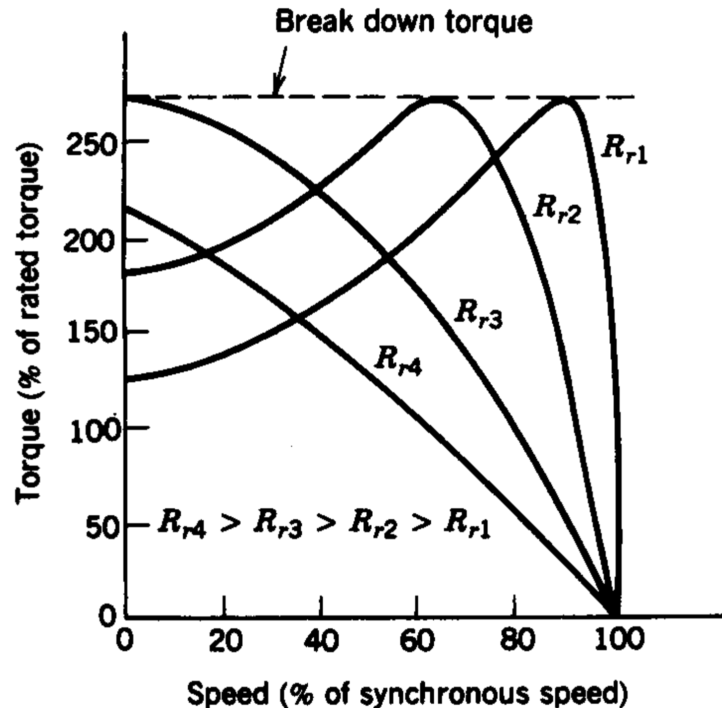

Figure 14-28 Torque–speed curves for a wound-rotor induction motor.

- Highly energy-inefficient unless using energy recovery schemes

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Static Slip Recovery

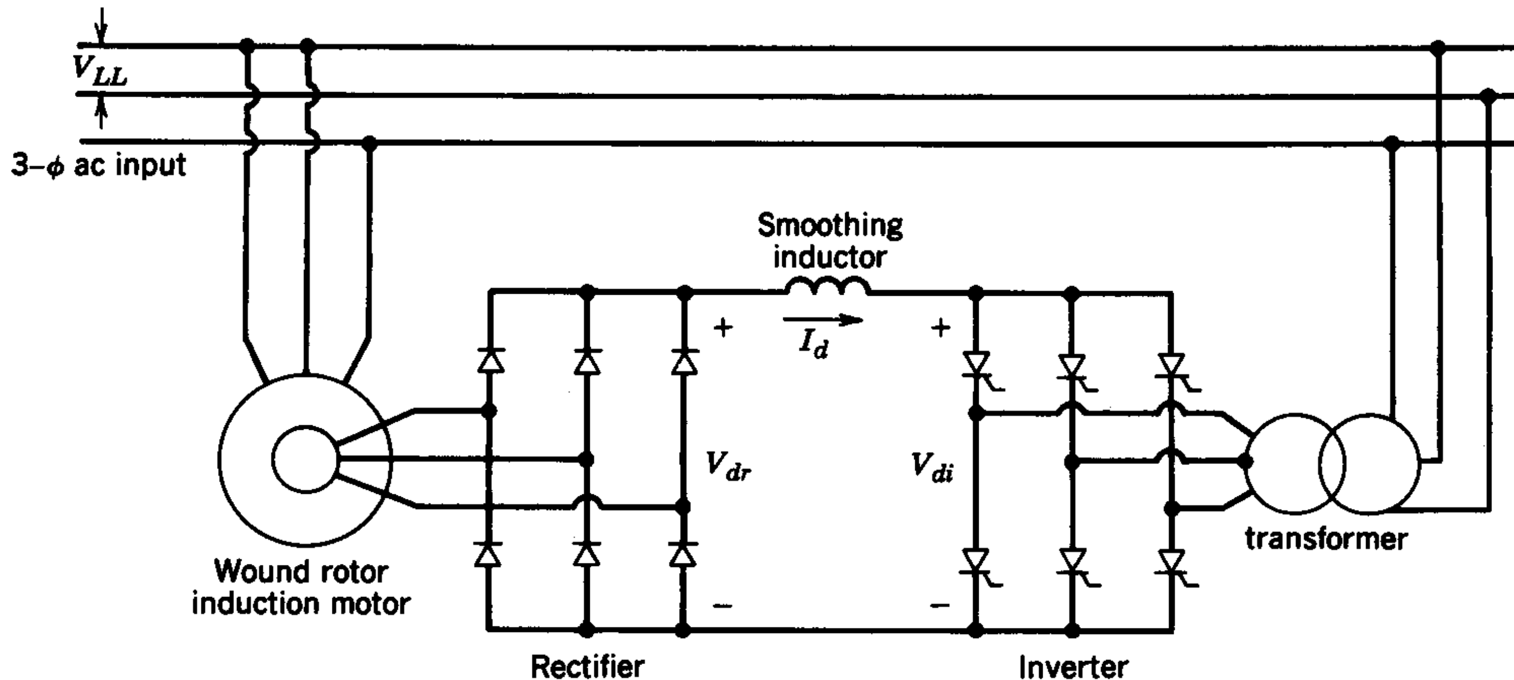

Figure 14-29 Static slip recovery.

- Applications in very large power ratings where the speed is to be adjusted over a very limited range

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Chapter 15

Synchronous Motor Drives

Chapter 15 Synchronous Motor Drives **435**

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15-3 Synchronous Servomotor Drives with Sinusoidal Waveforms 439
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- A large variety of applications – higher efficiency

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Rotor Structure

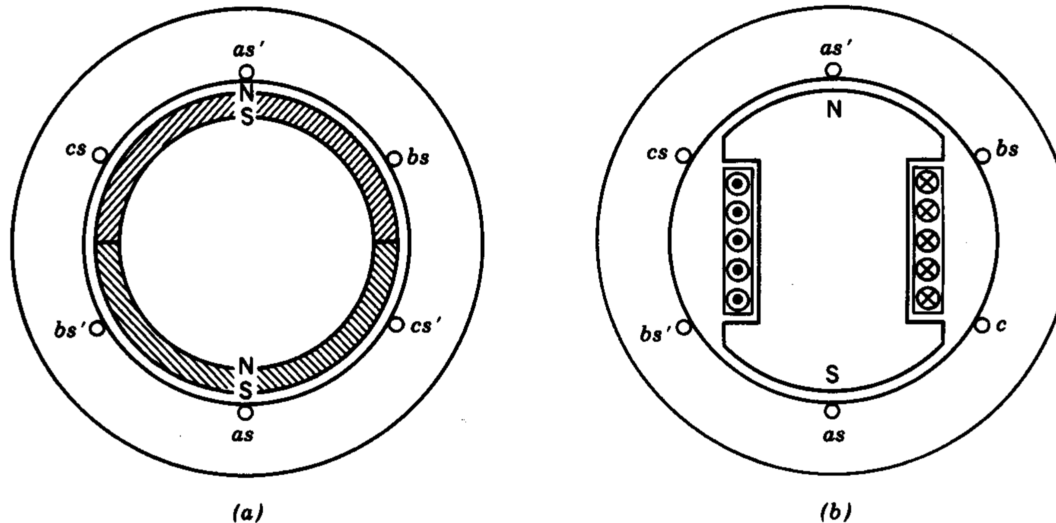

Figure 15-1 Structure of synchronous motors: (*a*) permanent-magnet rotor (two-pole); (*b*) salient-pole wound rotor (two-pole).

- Permanent-magnet or wound with a field winding

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Per-Phase Representation

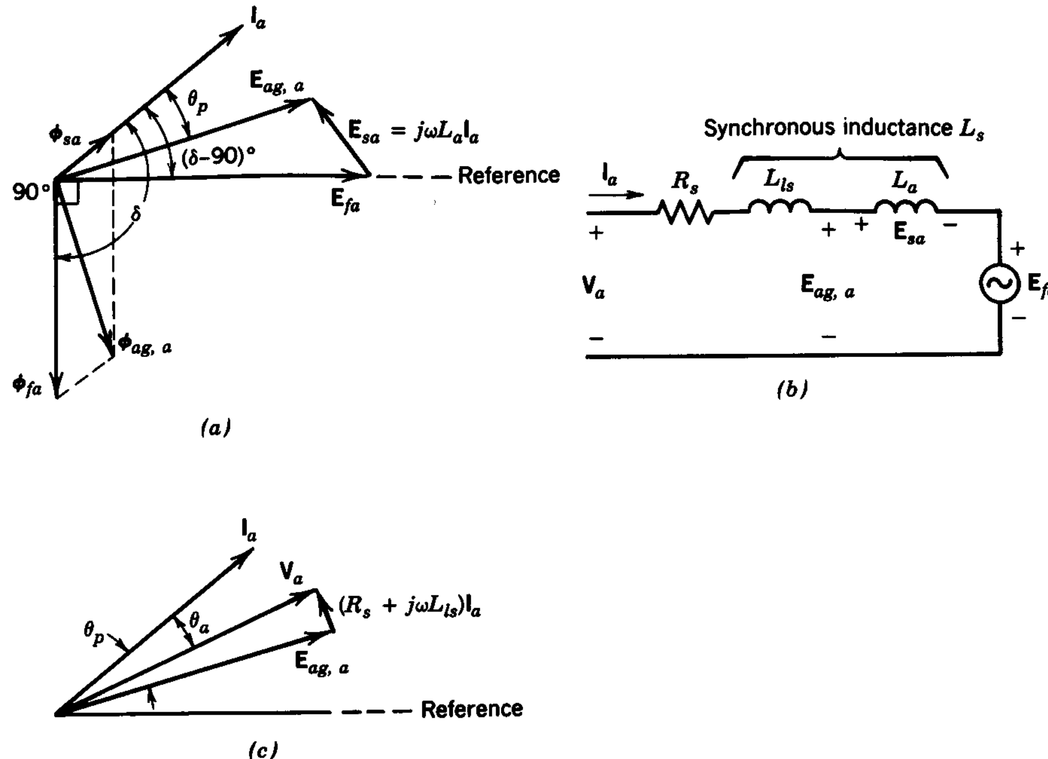

Figure 15-2 Per-phase representation: (*a*) phasor diagram; (*b*) equivalent circuit; (*c*) terminal voltage.

- In sinusoidal steady state

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Phasor Diagram

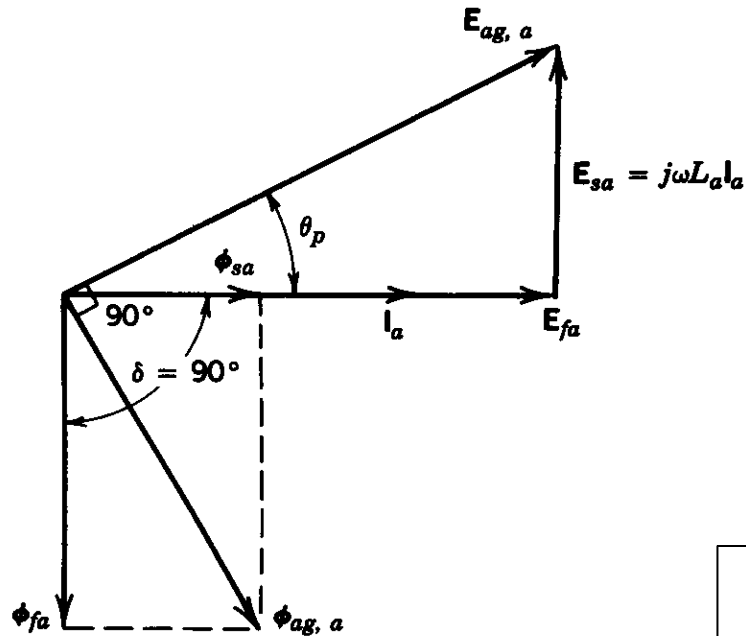

Figure 15-3 Phasor diagram with $\delta = 90°$.

- Optimum operation

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Rotor Position

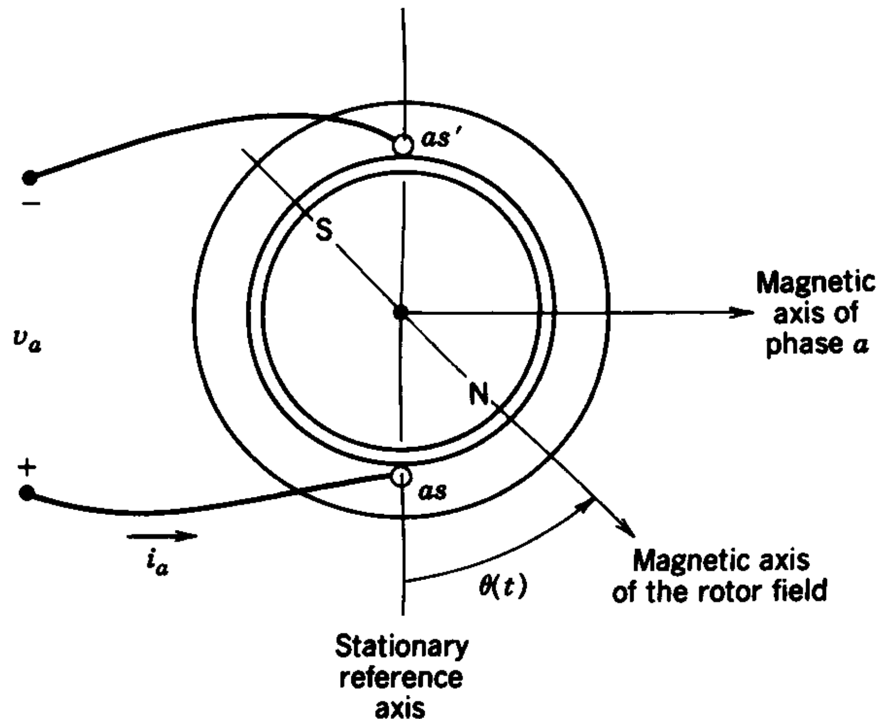

Figure 15-4 Measured rotor position θ at time *t*.

- Needs closed-loop operation knowing the rotor position

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Synchronous Motor Drive

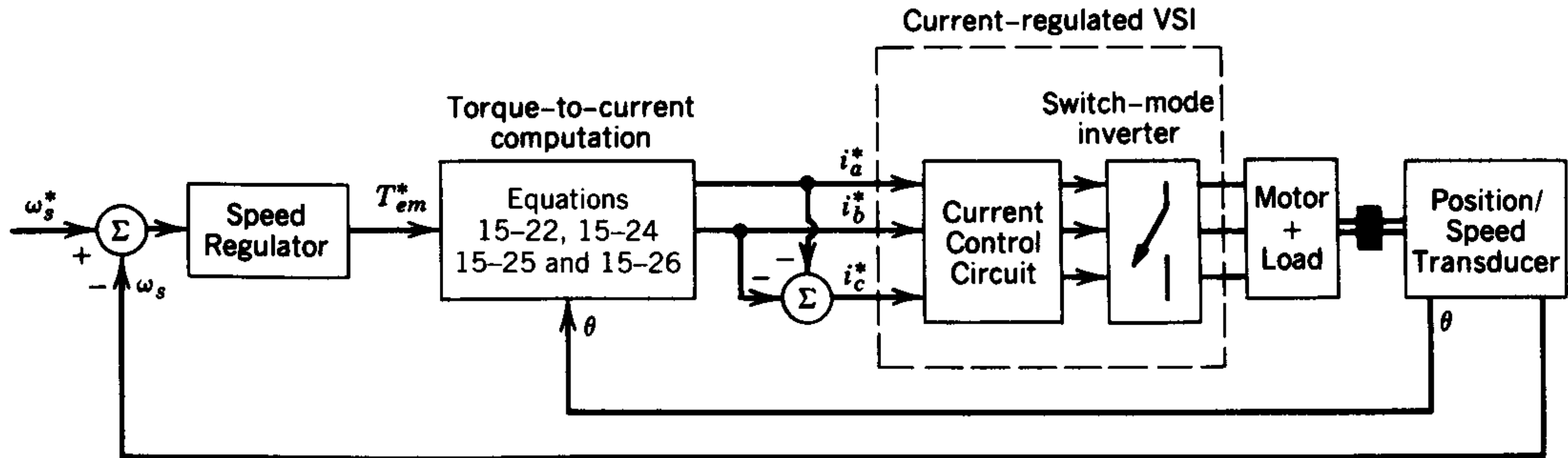

Figure 15-5 Synchronous motor servo drive.

- Controller based on steady state operation

Trapezoidal Waveform Synchronous Motor

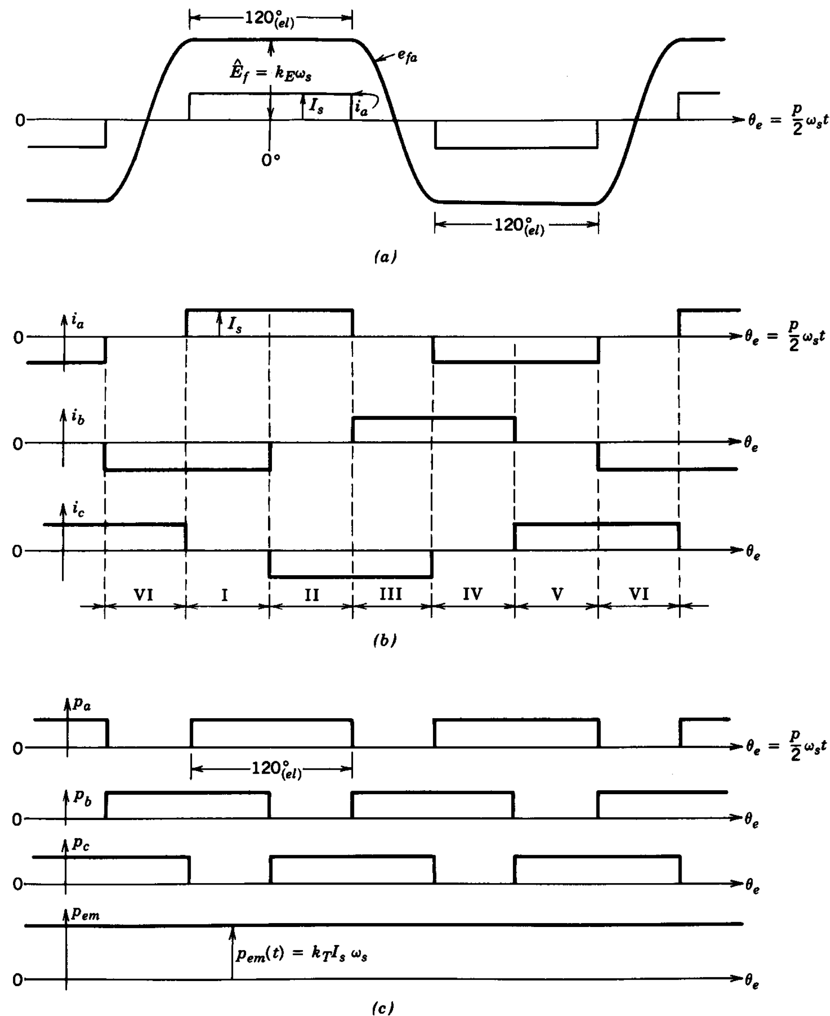

Figure 15-6 Trapezoidal-waveform synchronous motor drive.

- used in applications where speed of response not critical

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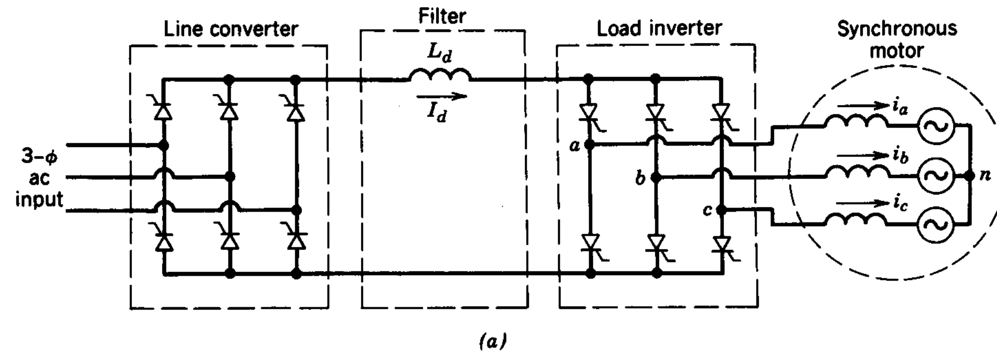
Load-Commutated Inverter (LCI) Drive



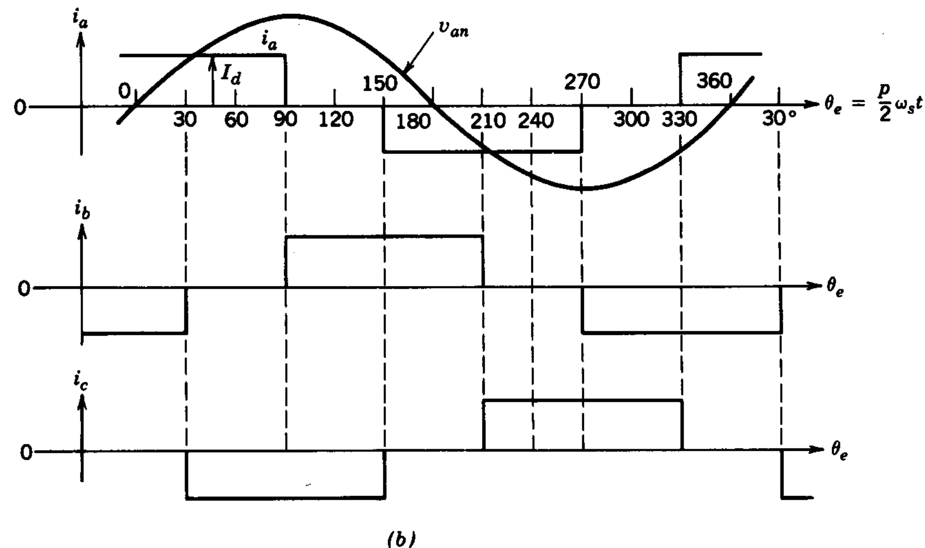


Figure 15-7 An LCI drive: (*a*) circuit; (*b*) idealized waveforms.

- Used in very large power ratings

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LCI Drive Controller

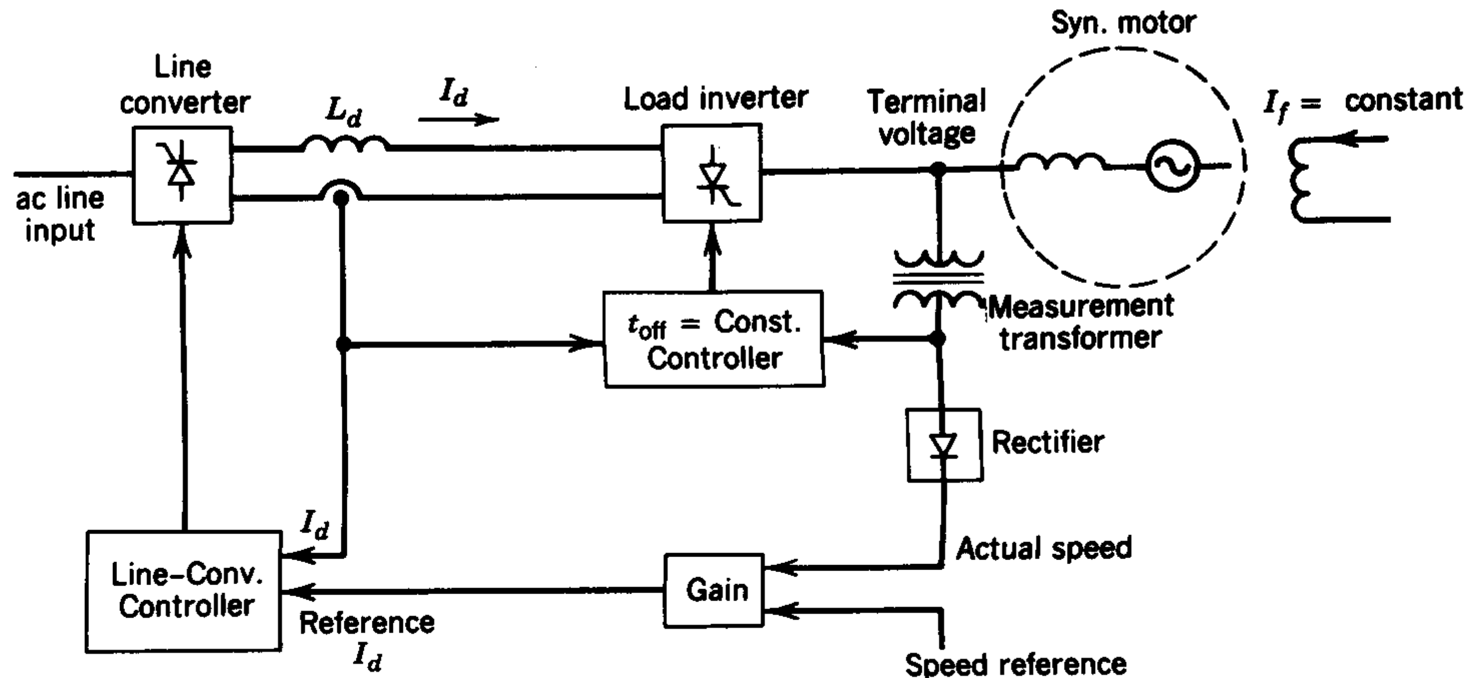

Figure 15-8 An LCI drive controller.

- Line converter controls the dc-link current

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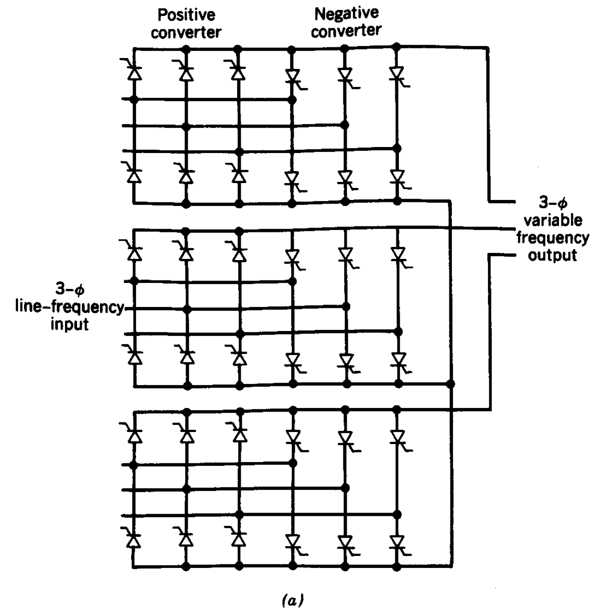
Three-Phase Cycloconverter

• Low-frequency ac output is synthesized



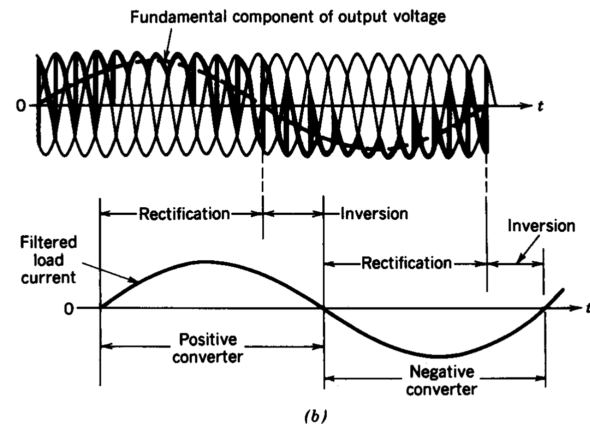


Figure 15-9 Three-phase cycloconverter.

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Chapter 16

Residential and Industrial Applications

Chapter 16 Residential and Industrial Applications **451**

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- Significant in energy conservation; productivity

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Improving Energy Efficiency of Heat Pumps

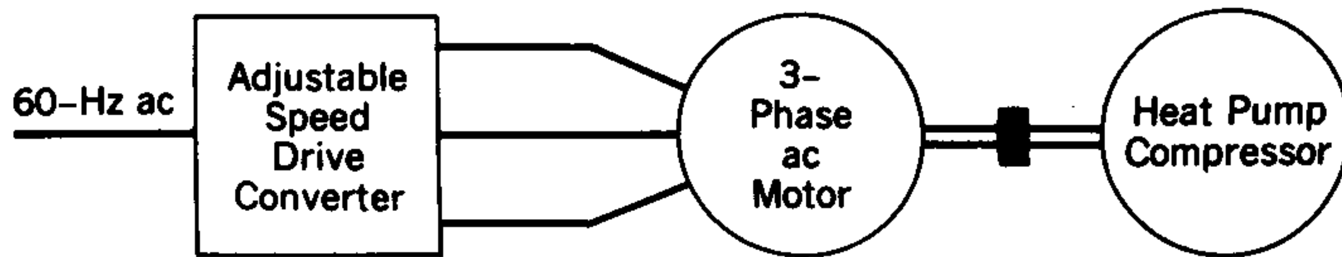

Figure 16-1 Load-proportional capacity-modulated heat pump.

- Used in one out of three new homes in the U.S.

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Loss Associated with ON/OFF Cycling

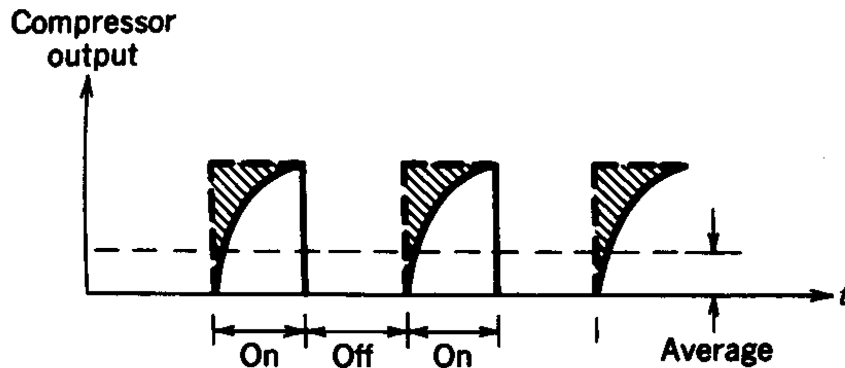

Figure 16-2 Conventional heat pump waveforms.

- The system efficiency is improved by ~30 percent

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Inductive Ballast of Fluorescent Lamps

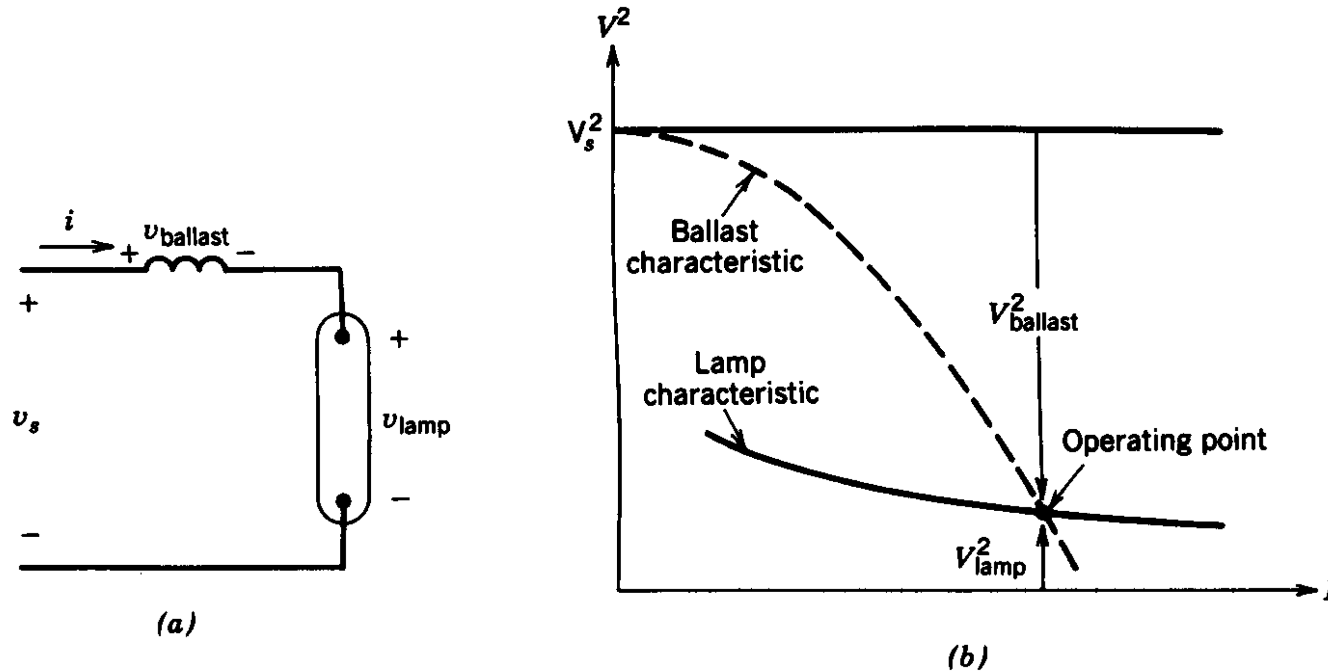

Figure 16-3 Fluorescent lamp with an inductive ballast.

- Inductor is needed to limit current

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Rapid-Start Fluorescent Lamps

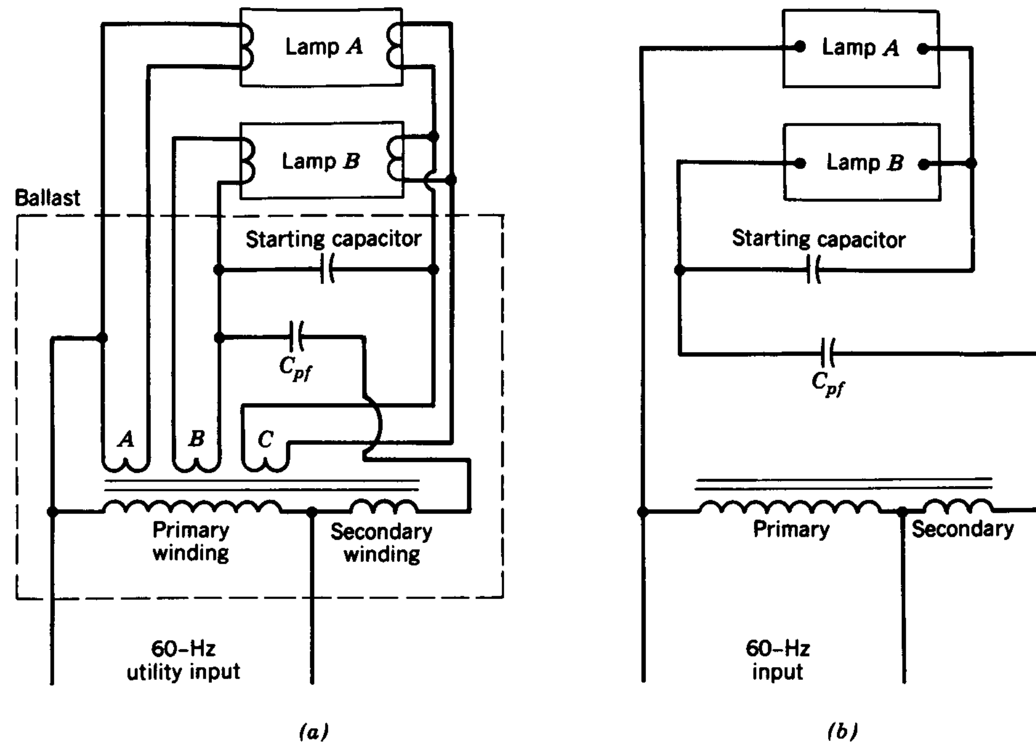

Figure 16-4 Conventional 60-Hz rapid-start fluorescent lamp: (*a*) circuit schematic; (*b*) simplified schematic.

- Starting capacitor is needed

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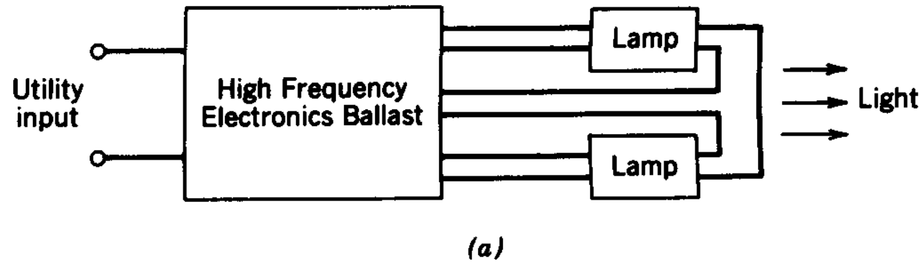
Electronic Ballast for Fluorescent Lamps



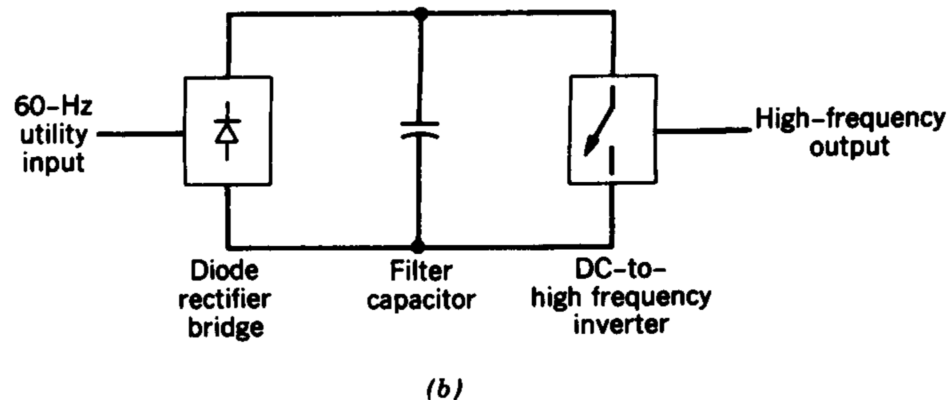


Figure 16-5 High-frequency fluorescent lighting system: (*a*) system block diagram; (*b*) ballast block diagram.

- Lamps operated at ~40 kHz

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Induction Cooking

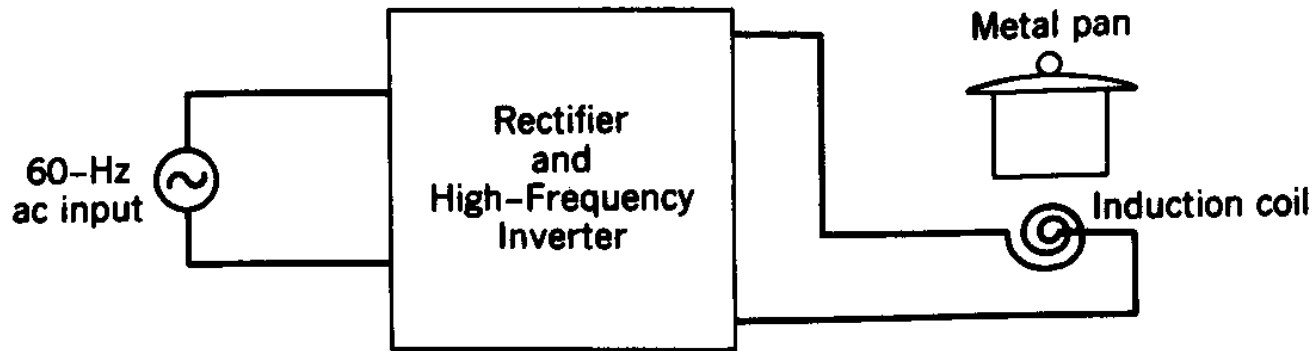

Figure 16-6 Induction cooking

- Pan is heated directly by circulating currents – increases efficiency

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Industrial Induction Heating

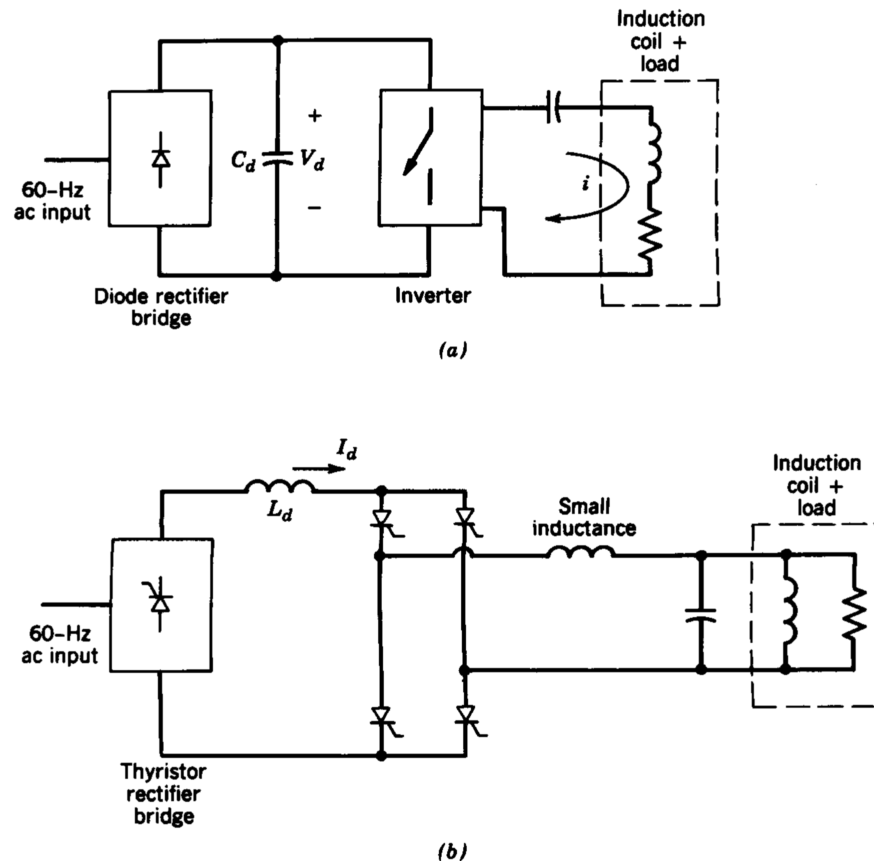

Figure 16-7 Induction heating: (*a*) voltage-source series-resonant induction heating; (*b*) current-source parallel-resonant induction heating.

- Needs sinusoidal current at the desired frequency: two options

Welding Application

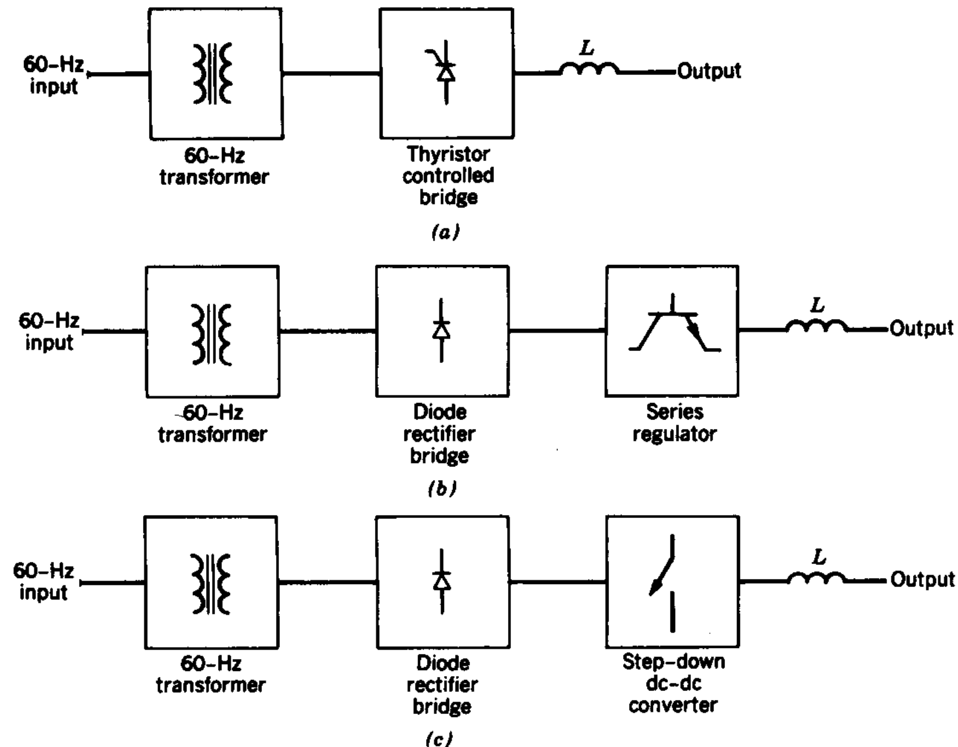

Figure 16-8 Welders with a 60-Hz transformer: (*a*) controlled thyristor bridge; (*b*) series regulator; (*c*) step-down dc–dc converter.

- Three options

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Switch-Mode Welders

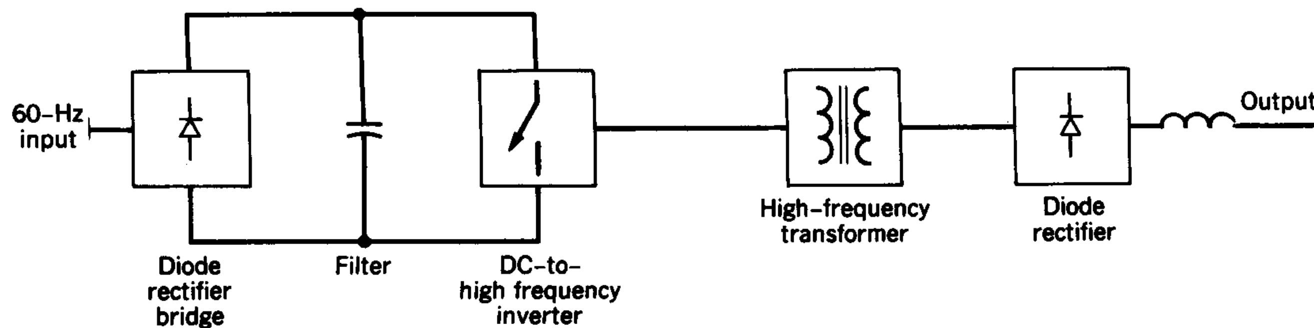

Figure 16-9 Switch-mode welder.

- Can be made much lighter weight

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Integral Half-Cycle Controllers

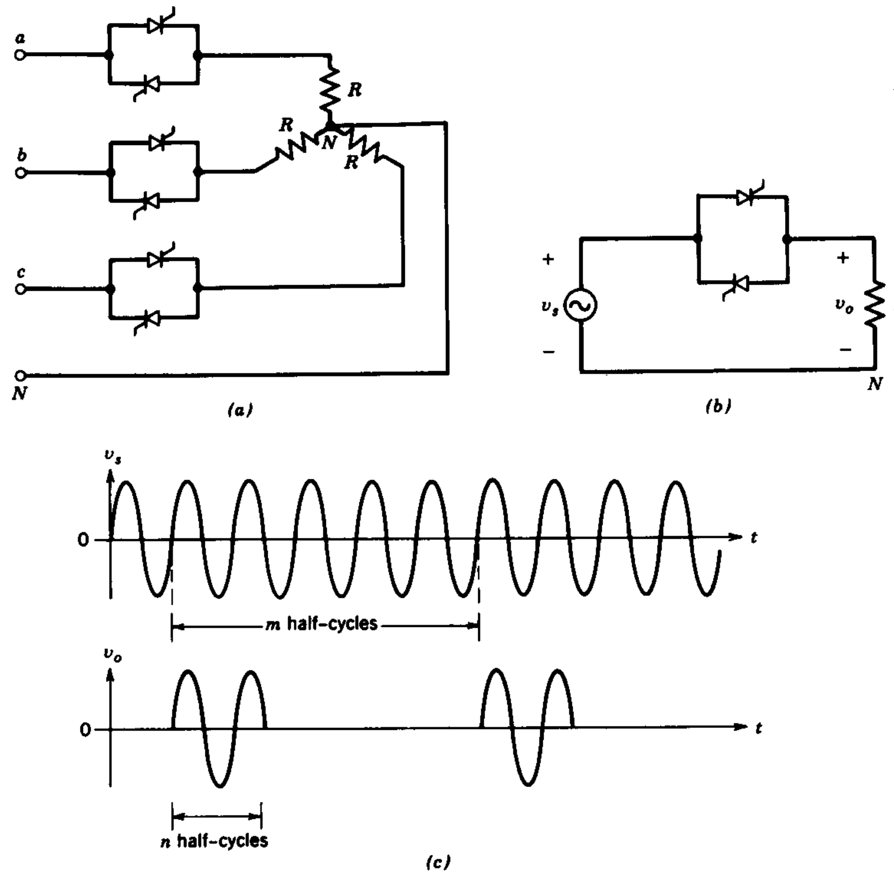

Figure 16-10 Integral half-cycle controllers: (*a*) three-phase circuit; (*b*) per-phase circuit; (*c*) waveforms.

- Used for heating

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Chapter 17

Electric Utility Applications

Chapter 17 Electric Utility Applications **460**

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- These applications are growing rapidly

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HVDC Transmission

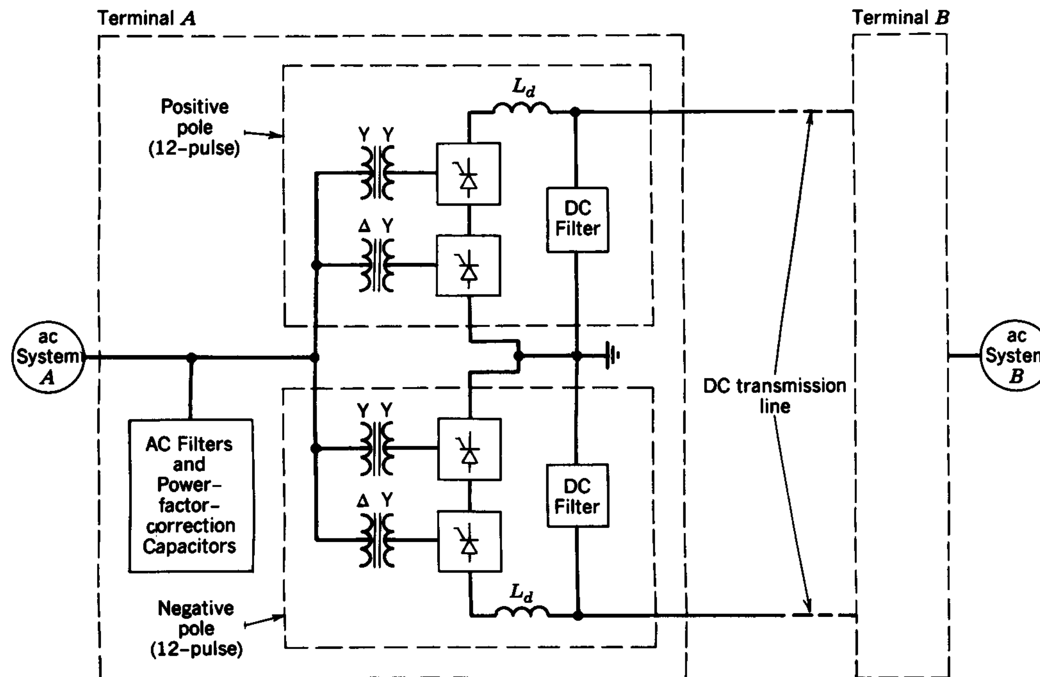

Figure 17-1 A typical HVDC transmission system.

- There are many such systems all over the world

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HVDC Poles

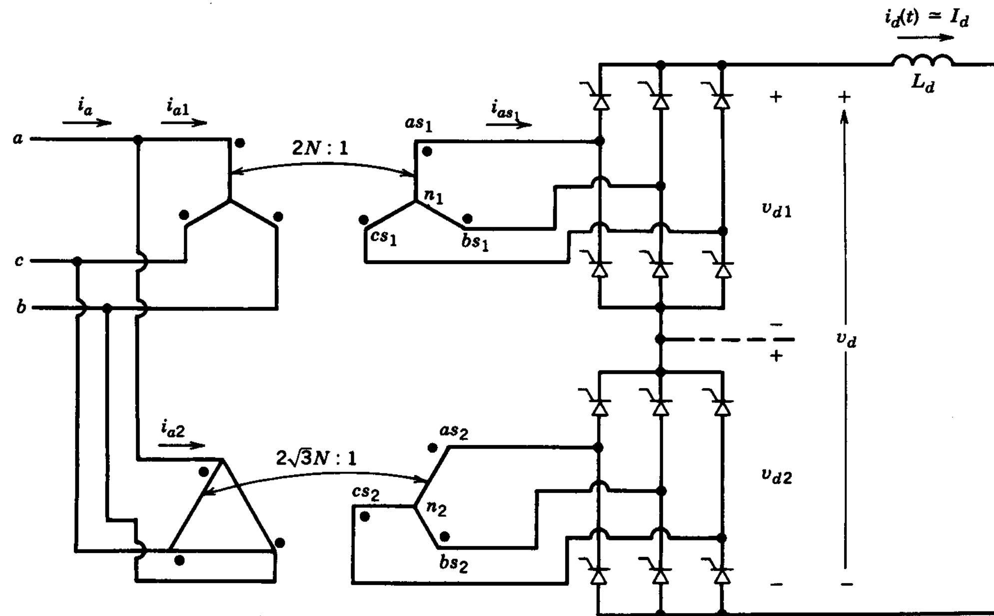

Figure 17-2 Twelve-pulse converter arrangement.

- Each pole consists of 12-pulse converters

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HVDC Transmission: 12-Pulse Waveforms

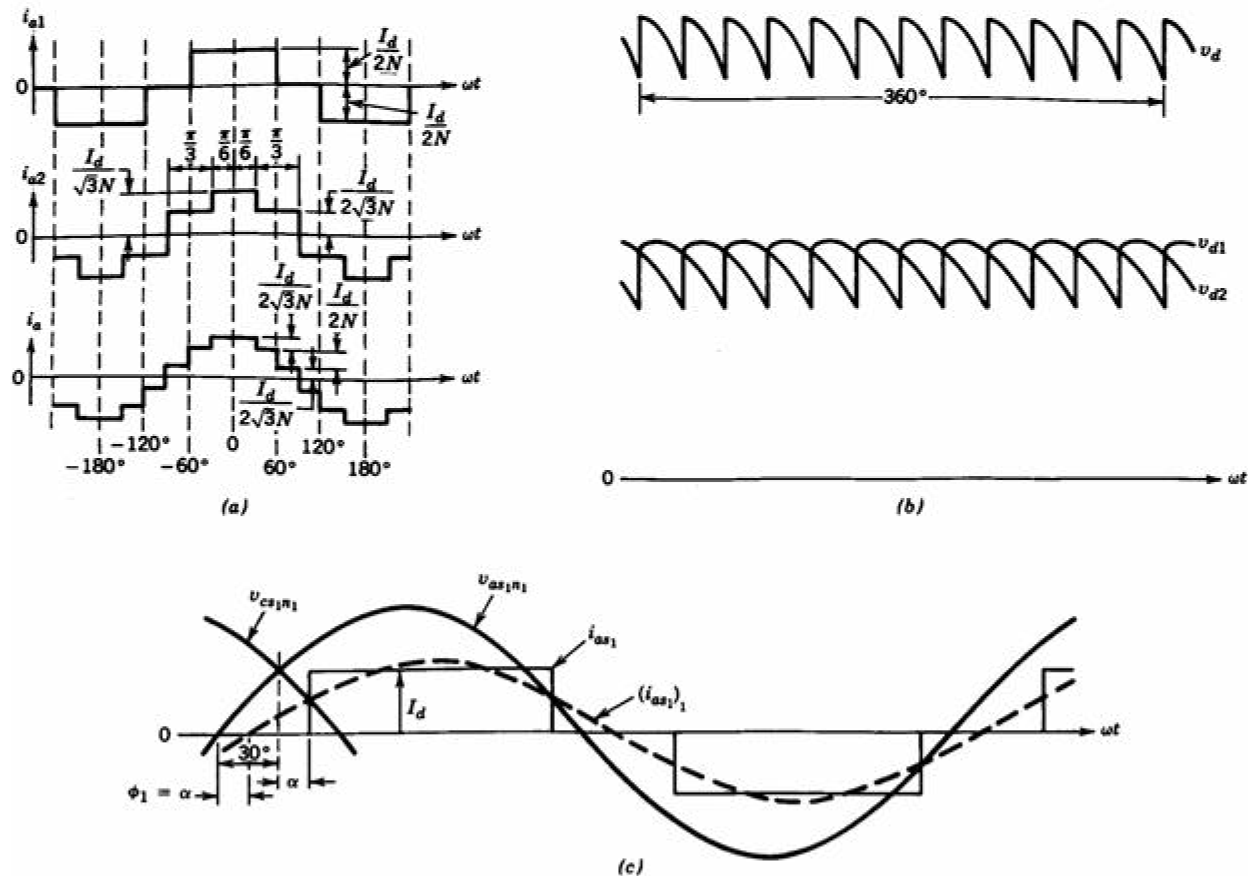
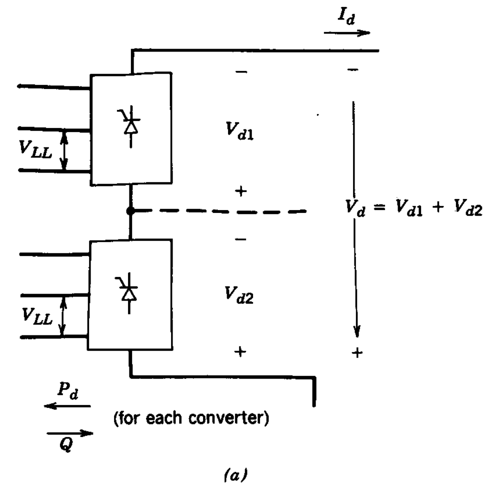
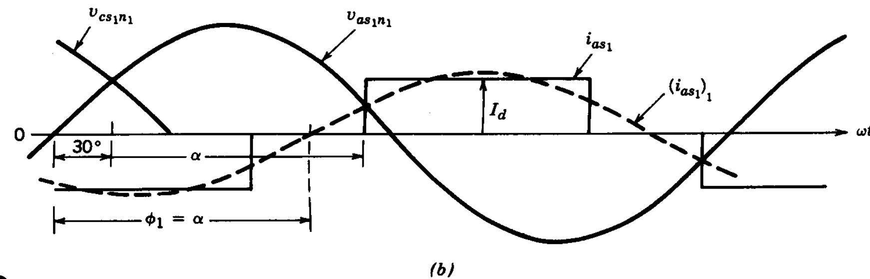


Figure 17-3 Idealized waveforms assuming $L_s = 0$.

- Idealized waveforms

HVDC Transmission: Converters





- Inverter mode of operation

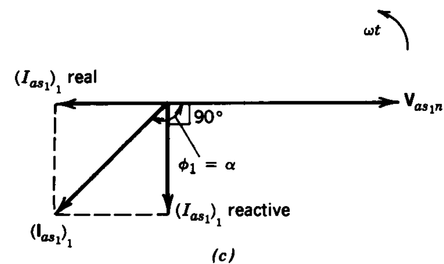


Figure 17-4 Inverter mode of operating (assuming $L_s = 0$).

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Control of HVDC Transmission System

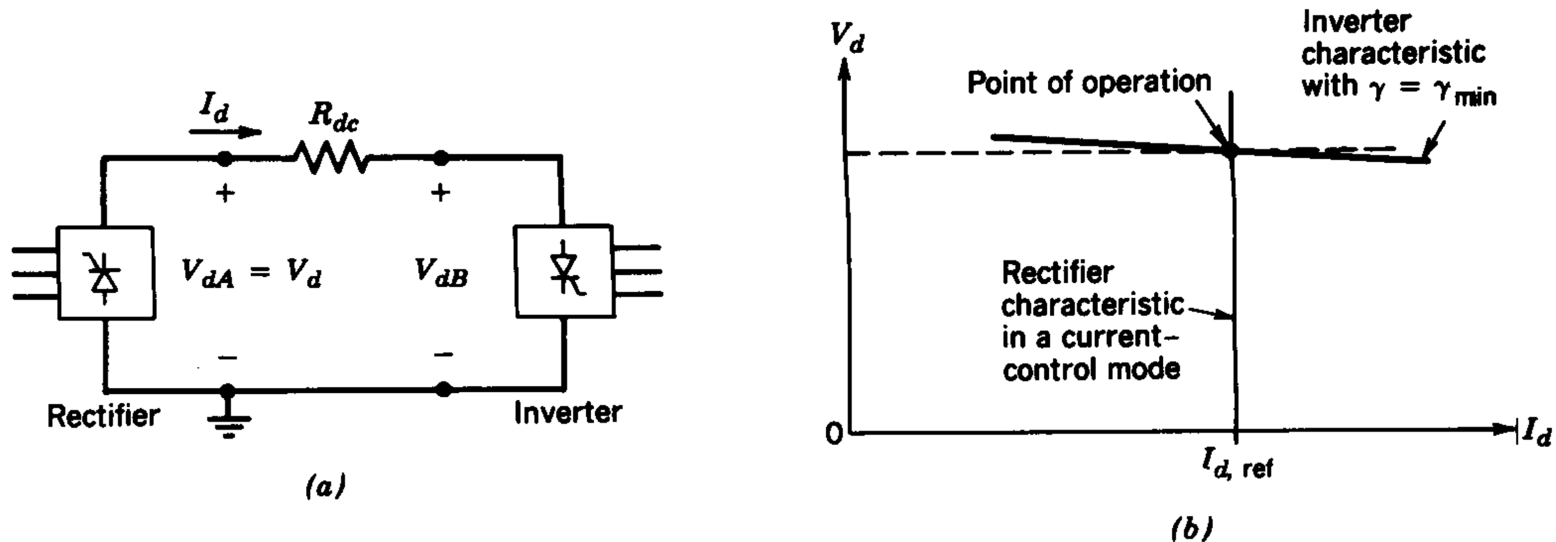

Figure 17-5 Control of HVDC system.

- Inverter is operated at the minimum extinction angle and the rectifier in the current-control mode

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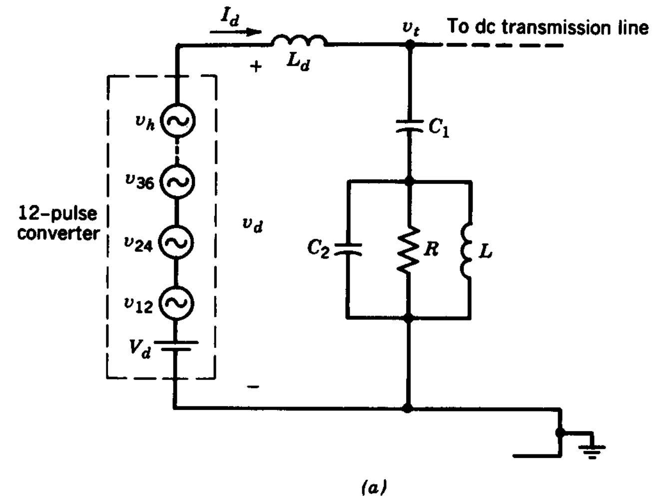
HVDC Transmission: DC-Side Filters



Tuned for the lowest (12th harmonic) frequency

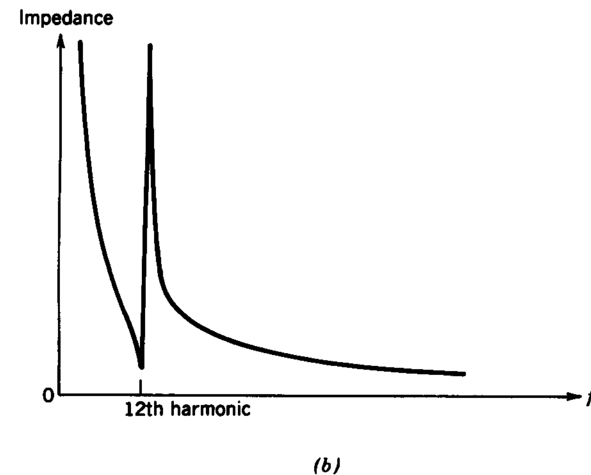


Figure 17-6 Filter for dc-side voltage harmonics: (*a*) dc-side equivalent circuit; (*b*) high-pass filter impedance vs. frequency.

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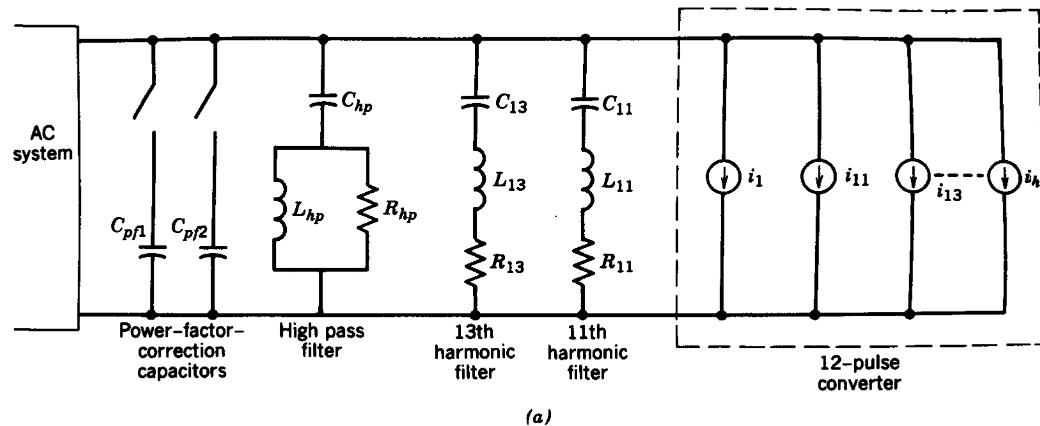
HVDC Transmission: AC-Side Filters



Tuned for the lowest (11th and the 13th harmonic) frequencies

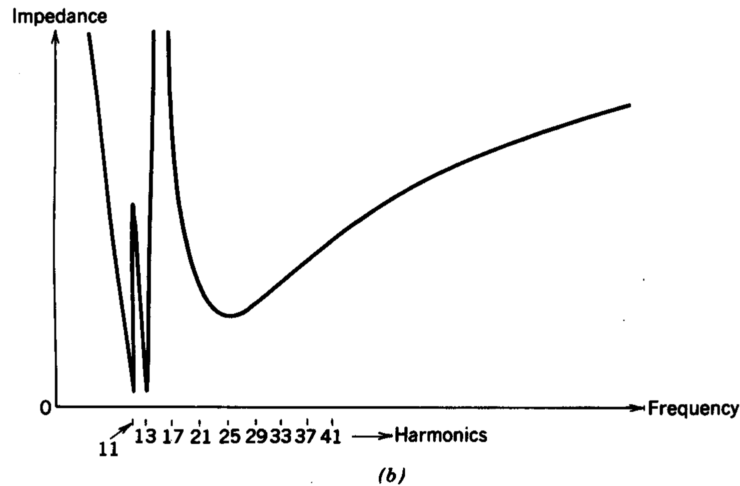


Figure 17-7 The ac side filters and power factor correction capacitors: (*a*) per-phase equivalent circuit; (*b*) combined per-phase filter impedance vs. frequency.

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Effect of Reactive Power on Voltage Magnitude

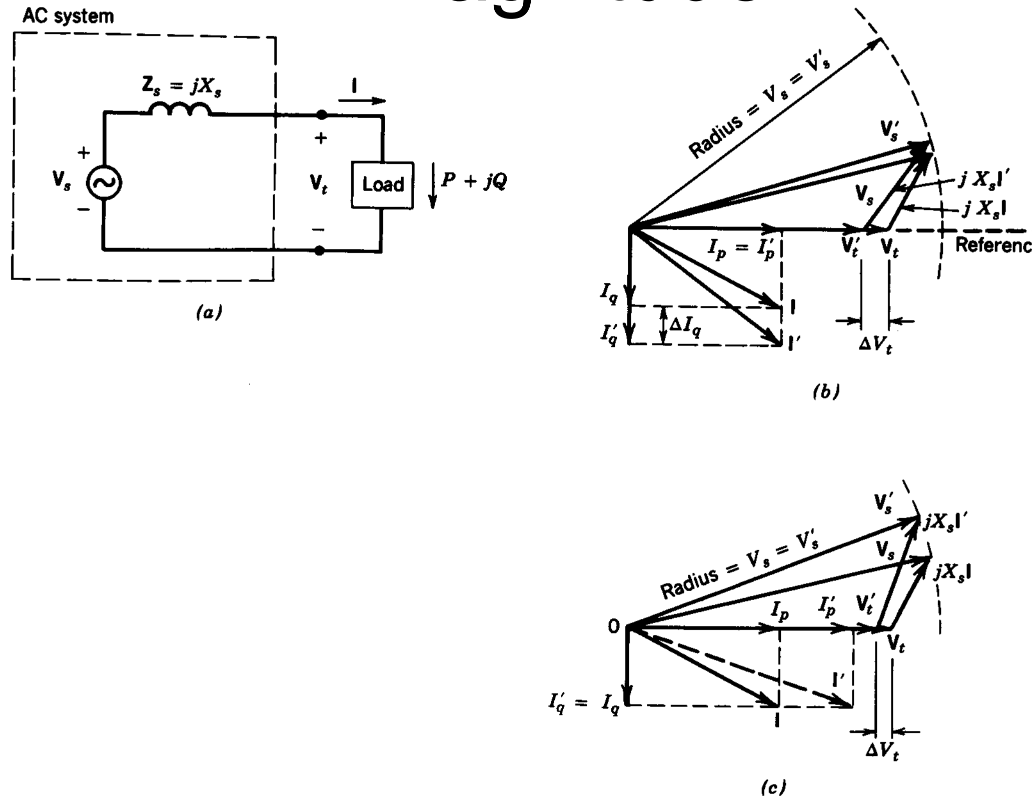

Figure 17-8 Effect of I_p and I_q on V_t: (*a*) equivalent circuit; (*b*) change in I_q; (*c*) change in I_p.

- Illustration of the basic principle

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Thyristor-Controlled Inductor (TCI)

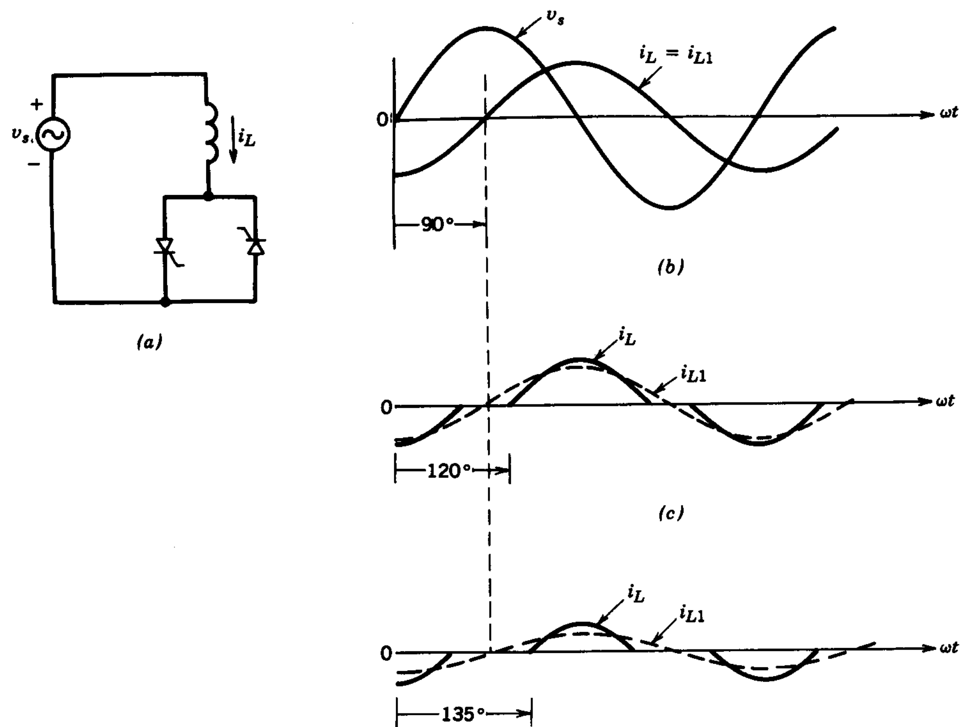

Figure 17-9 A TCI, basic principle: (*a*) per-phase TCI; (*b*) $0 < \alpha < 90°$; (*c*) $\alpha = 120°$; (*d*) $\alpha = 135°$.

- Increasing the delay angle reduces the reactive power drawn by the TCI

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Thyristor-Switched Capacitors (TSCs)

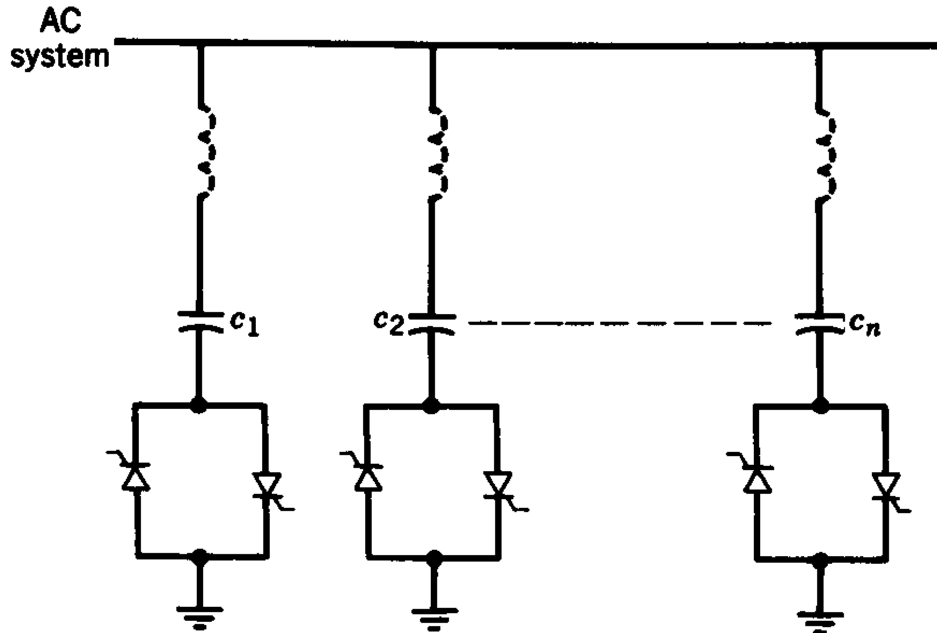

Figure 17-10 A TSC arrangement.

- Transient current at switching must be minimized

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Instantaneous VAR Controller (SATCOM)

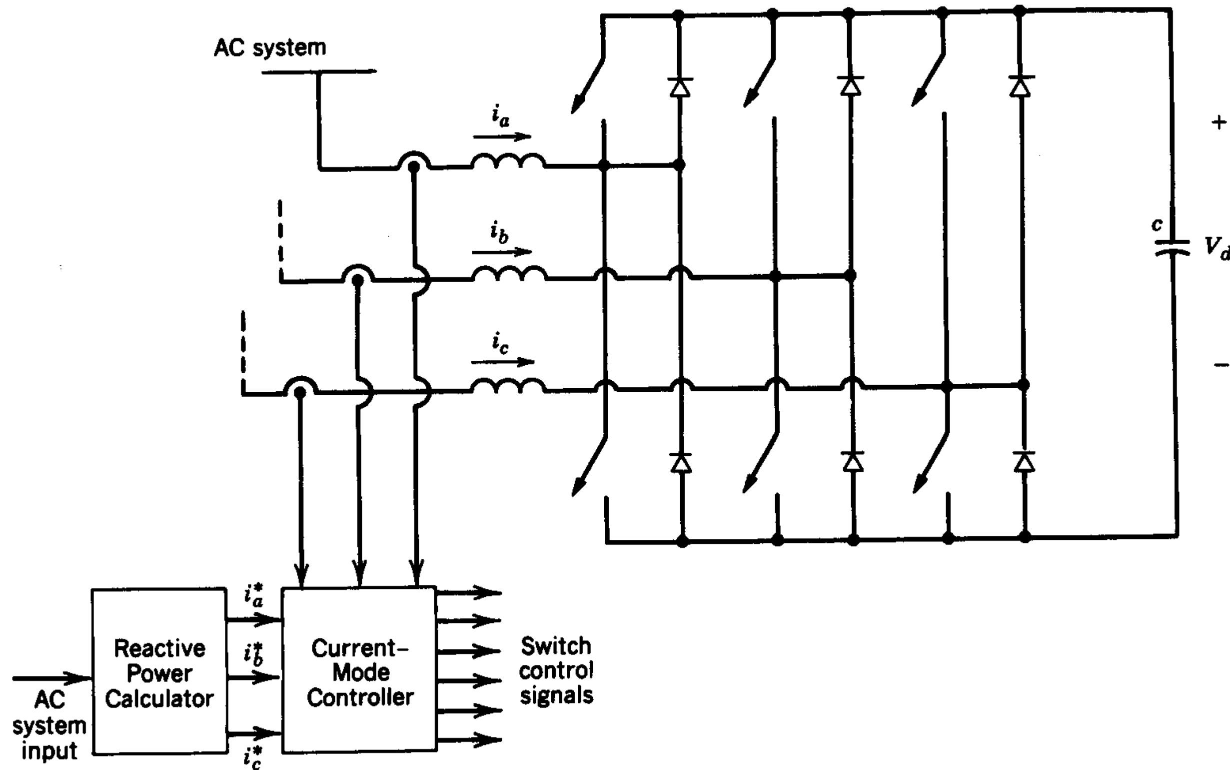

Figure 17-11 Instantaneous var controller.

- Can be considered as a reactive current source

Characteristics of Solar Cells

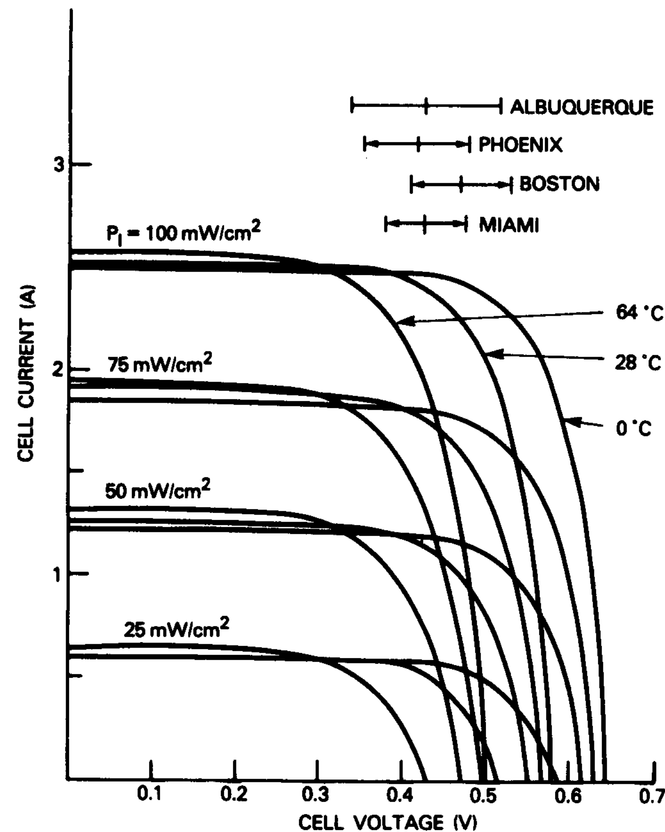

Figure 17-12 The *I–V* characteristics of solar cells. (*Source:* reference 10.)

- The maximum power point is at the knee of the characteristics

Photovoltaic Interface

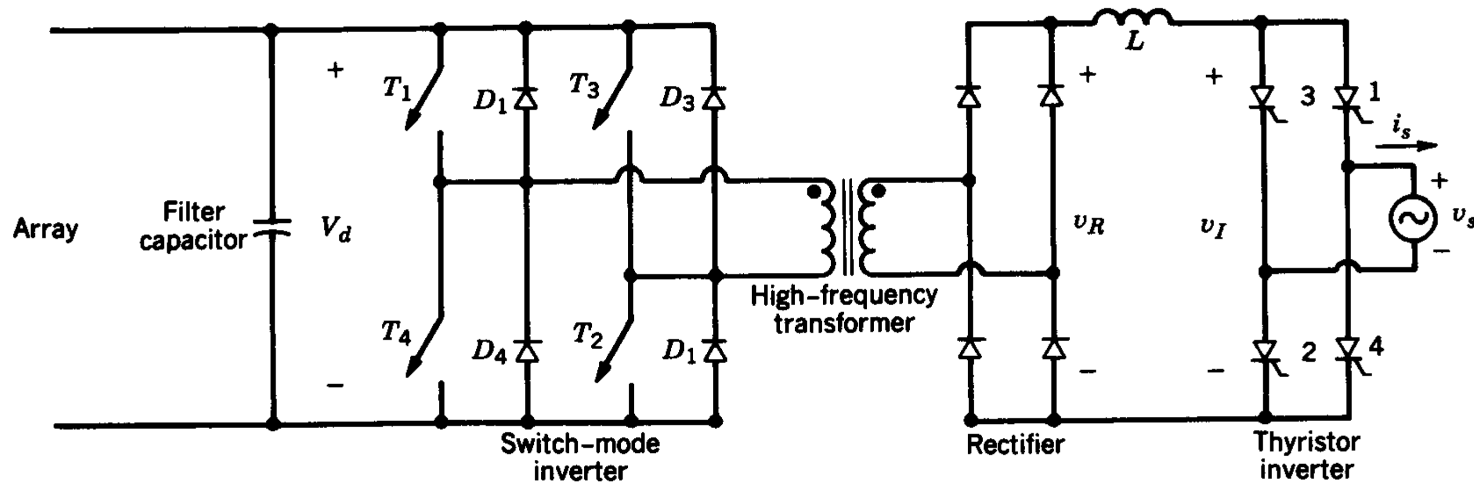

Figure 17-13 High-frequency photovoltaic interface.

- This scheme uses a thyristor inverter

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Harnessing of Wing Energy

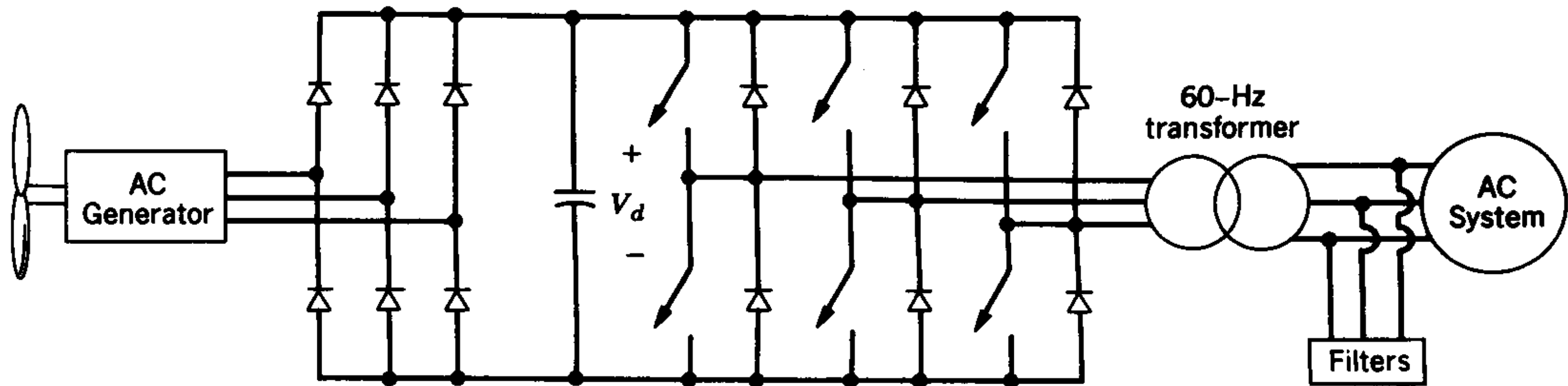

Figure 17-14 Interconnection of wind/hydro generator.

- A switch-mode inverter may be needed on the wind generator side also

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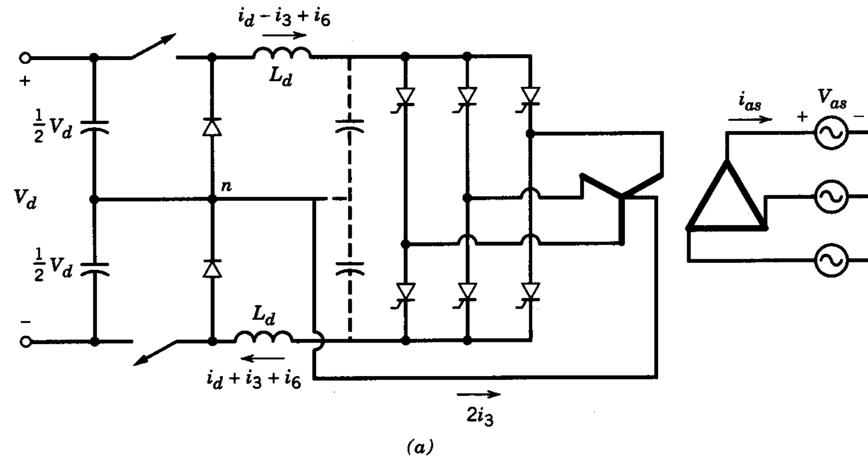
Interface with 3-Phase Utility Grid



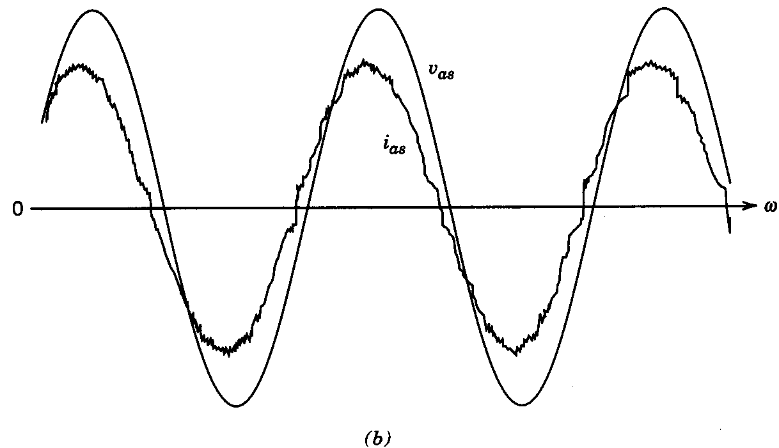


Figure 17-15 New topology, utility interface [12].

- Uses a thyristor inverter

Interface of SMES

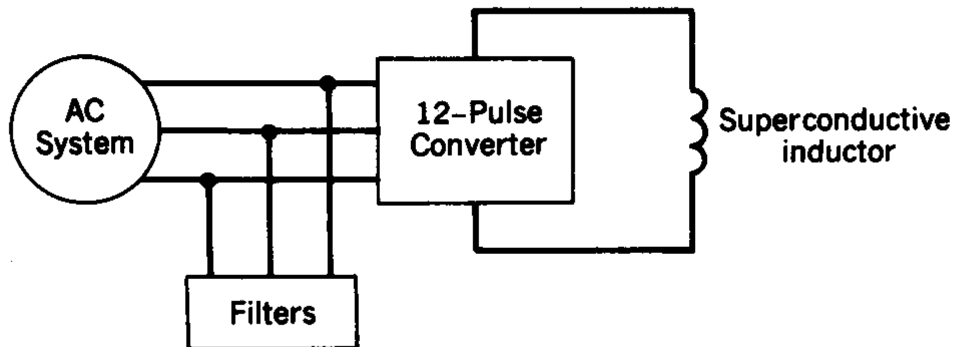


Figure 17-16 Superconductive energy storage inductor interconnection.

- Can be used for utility load leveling

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Active Filters for Harmonic Elimination

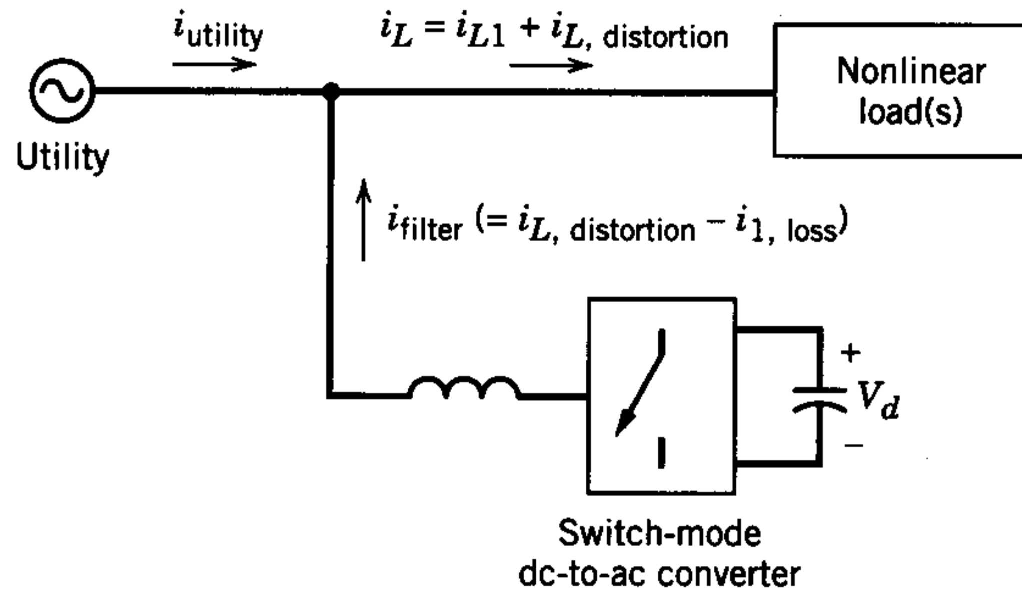

Figure 17-17 One-line diagram of an active filter.

- Active filters inject a nullifying current so that the current drawn from the utility is nearly sinusoidal

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Chapter 18

Utility Interface

Chapter 18 Optimizing the Utility Interface with Power Electronic Systems **483**

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- Power quality has become an important issue

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Various Loads Supplied by the Utility Source

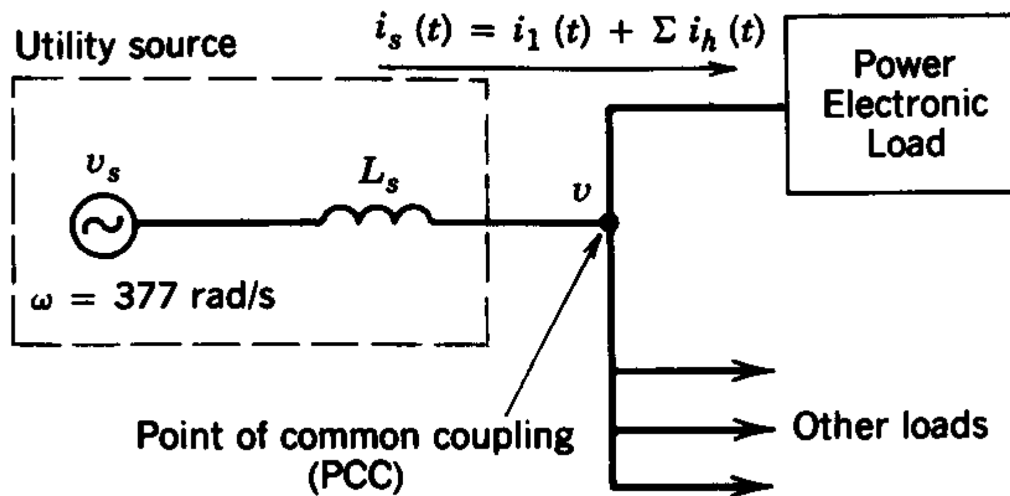

Figure 18-1 Utility interface.

- PCC is the point of common coupling

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Diode-Rectifier Bridge

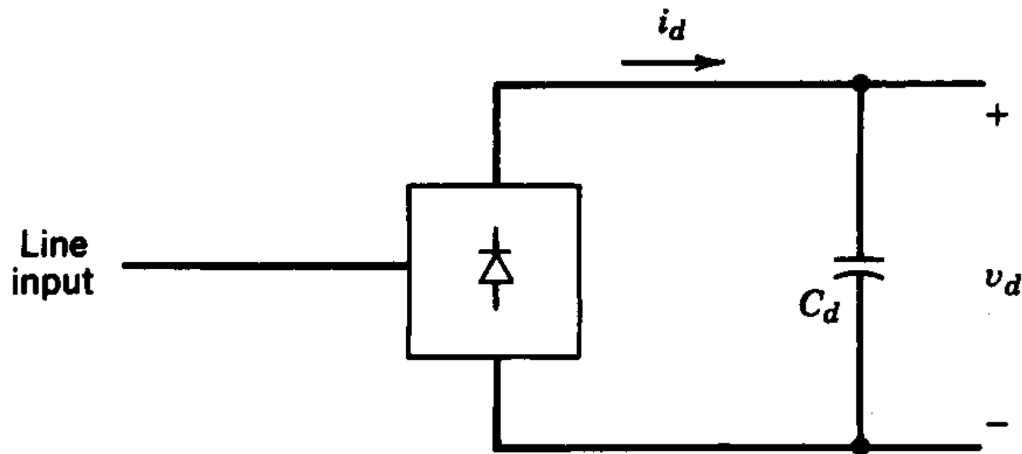

Figure 18-2 Diode rectifier bridge.

- Bock diagram

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Typical Harmonics in the Input Current

Table 18-1 Typical Harmonics in a Single-Phase Input Current Waveform with No Line Filtering

h	3	5	7	9	11	13	15	17
$\left(\frac{I_h}{I_1}\right)\%$	73.2	36.6	8.1	5.7	4.1	2.9	0.8	0.4

- Single-phase diode-rectifier bridge

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Harmonic Guidelines: IEEE 519

Table 18-2 Harmonic Current Distortion (I_h/I_1)

I_{SC}/I_1	*Odd Harmonic Order h (%)*					*Total Harmonic Distortion (%)*
	$h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h$	
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Note: Harmonic current limits for nonlinear load connected to a public utility at the point of common coupling (PCC) with other loads at voltages of 2.4–69 kV. I_{sc} is the maximum short-circuit current at PCC. I_1 is the maximum fundamental-frequency load current at PCC. Even harmonics are limited to 25% of the odd harmonic limits above.

Source: Reference 1.

- commonly used for specifying limits on the input current distortion

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Harmonic Guidelines: IEEE 519

Table 18-3 Harmonic Voltage Limits (V_h/V_1) (%) for Power Producers (Public Utilities or Cogenerators)

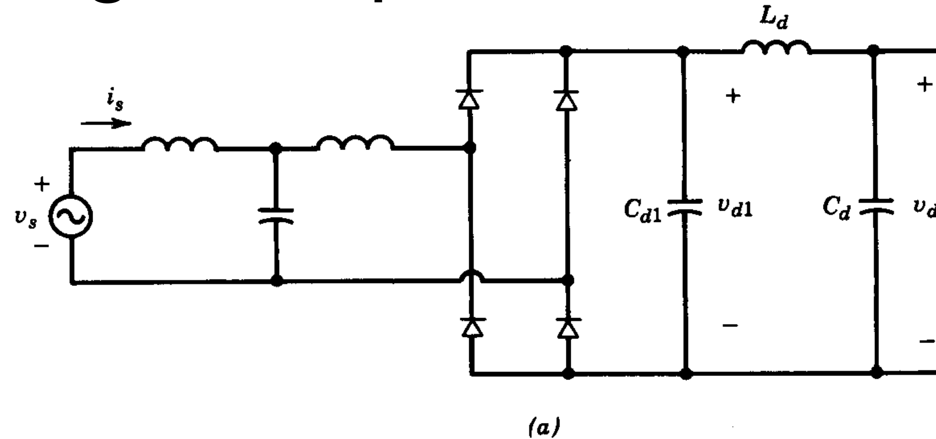
	2.3–69 kV	*69–138 kV*	*> 138 KV*
Maximum for individual harmonic	3.0	1.5	1.0
Total harmonic distortion	5.0	2.5	1.5

Note: This table lists the quality of the voltage that the power producer is required to furnish a user. It is based on the voltage level at which the user is supplied.

Source: Reference 1.

- Limits on distortion in the input voltage supplied by the utility

Reducing the Input Current Distortion



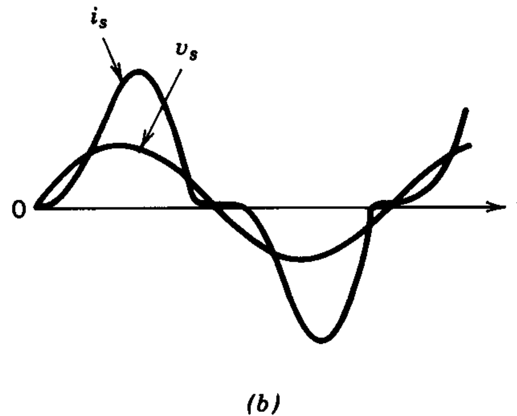


Figure 18-3 Passive filters to improve i_s waveform: (*a*) passive filter arrangement; (*b*) current waveform.

- use of passive filters

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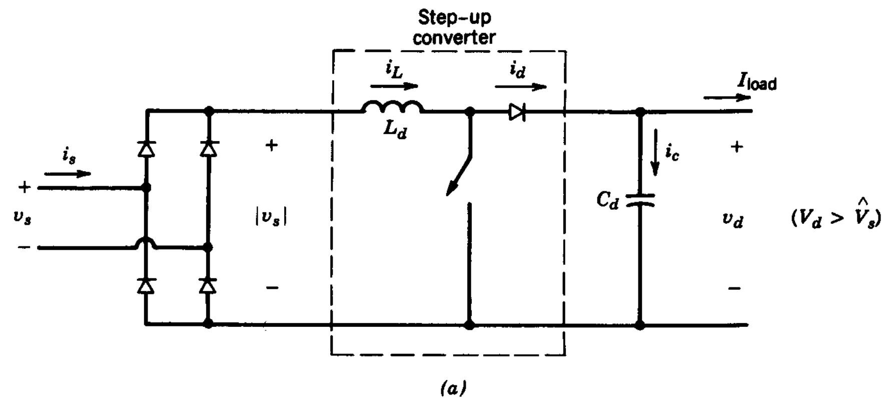
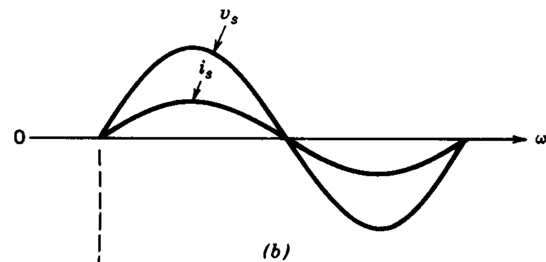
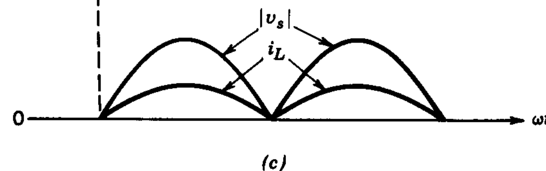
Power-Factor-Correction (PFC) Circuit



(a)



(b)



(c)

Figure 18-4 Active harmonic filtering: (a) step-up converter for current shaping; (b) line waveforms; (c) v_s and i_L.

- For meeting the harmonic guidelines

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Power-Factor-Correction (PFC) Circuit Control

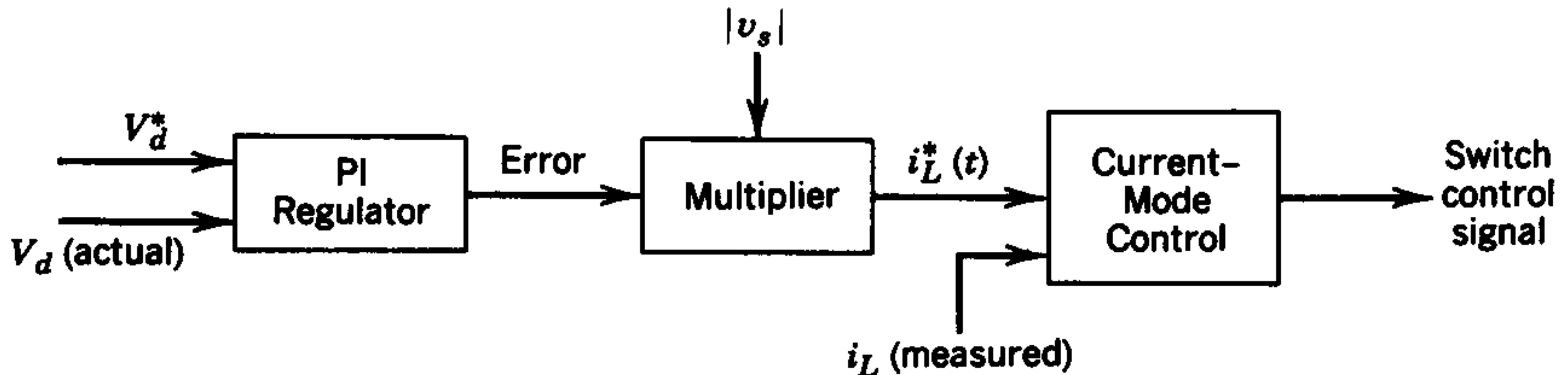

Figure 18-5 Control block diagram.

- generating the switch on/off signals

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Power-Factor-Correction (PFC) Circuit

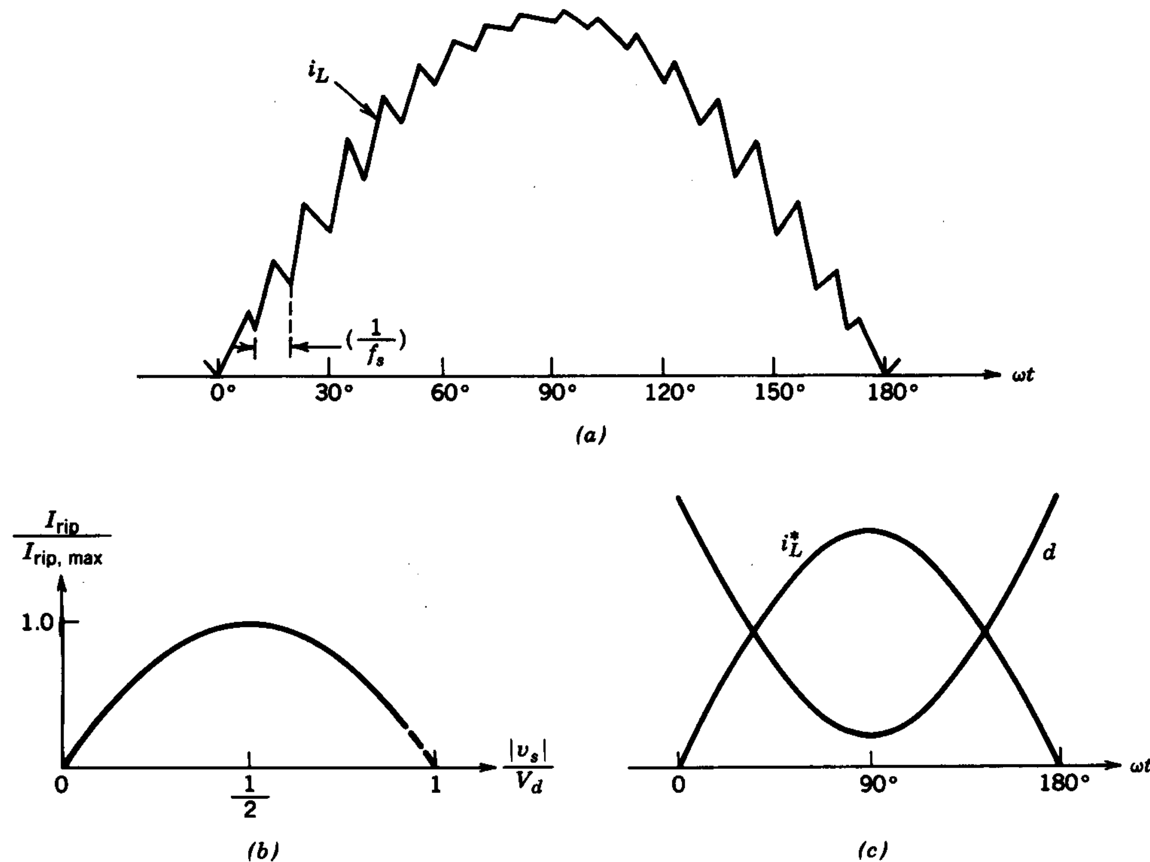

Figure 18-6 Constant-frequency control.

- Operation during each half-cycle

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Thyristor Converters for 4-Quadrant Operation

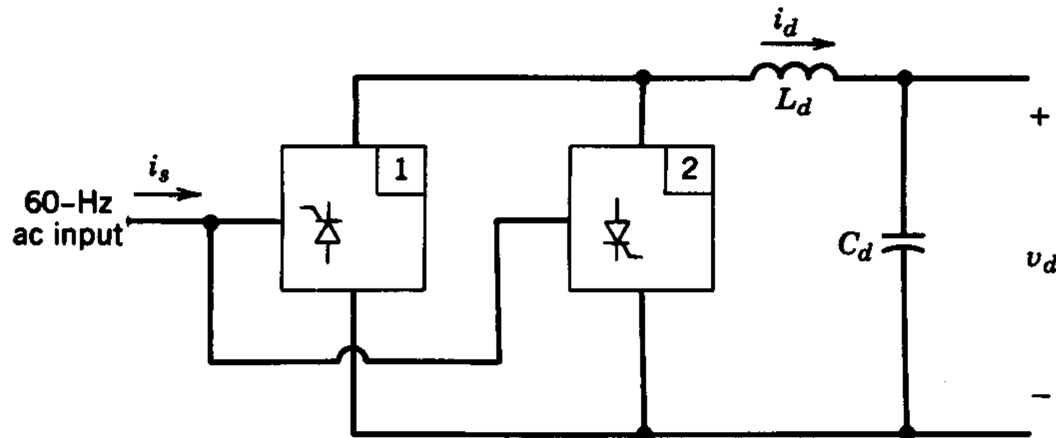

Figure 18-7 Back-to-back connected converters for bidirectional power flow.

- Two back-to-back connected 2-quadrant converters

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Switch-Mode Converter Interface

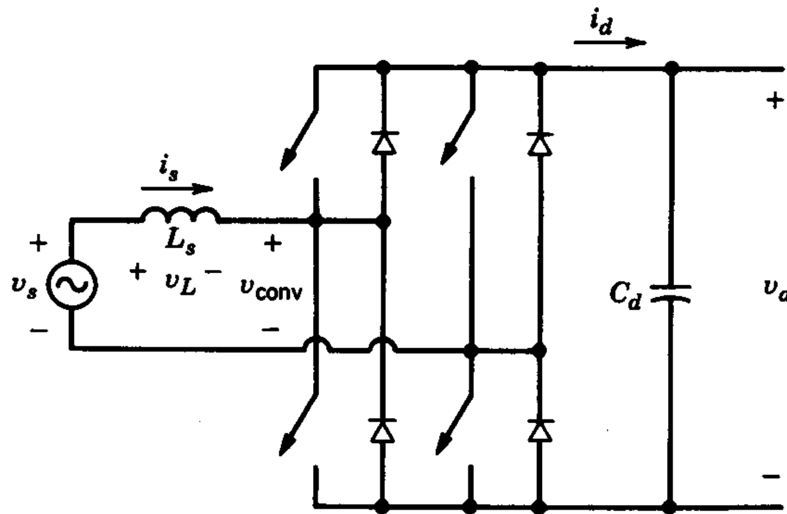

Figure 18-8 Switch-mode converter for the utility interface.

- Bi-directional power flow; unity PF is possible

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Switch-Mode Converter Interface

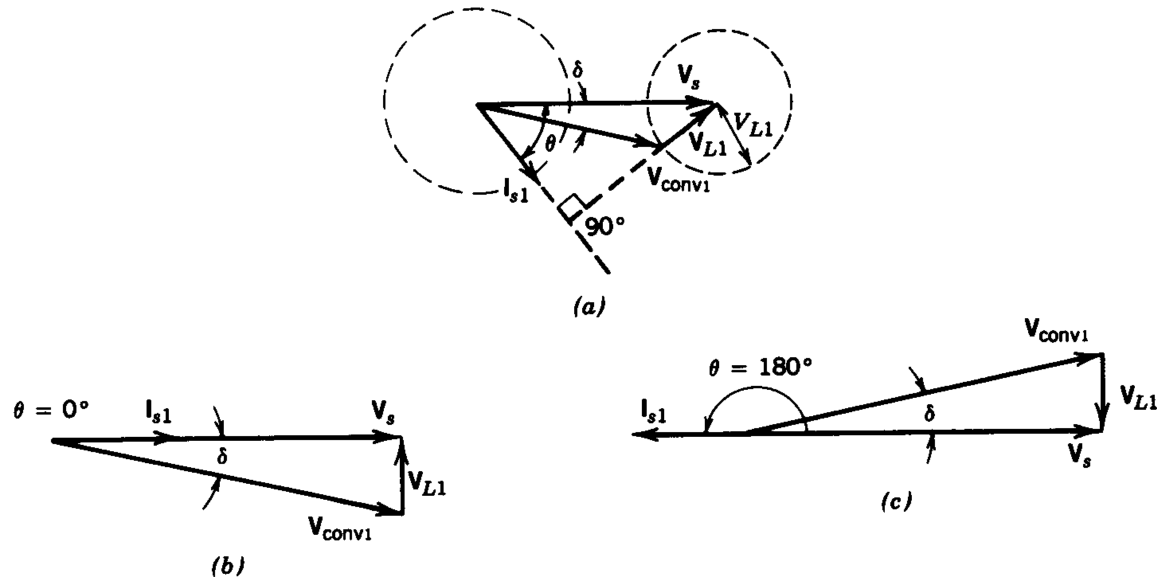

Figure 18-9 Rectification and inversion: (*a*) general phasor diagram; (*b*) rectification at unity power factor; (*c*) inversion at unity power factor.

- Rectifier and Inverter modes based on the direction of power flow

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Switch-Mode Converter Control

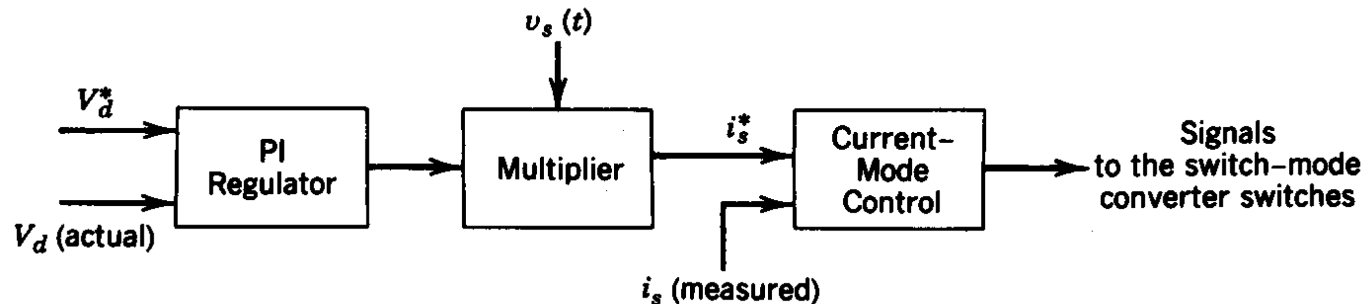

Figure 18-10 Control of the switch-mode interface.

- DC bus voltage is maintained at the reference value

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Switch-Mode Converter Interface

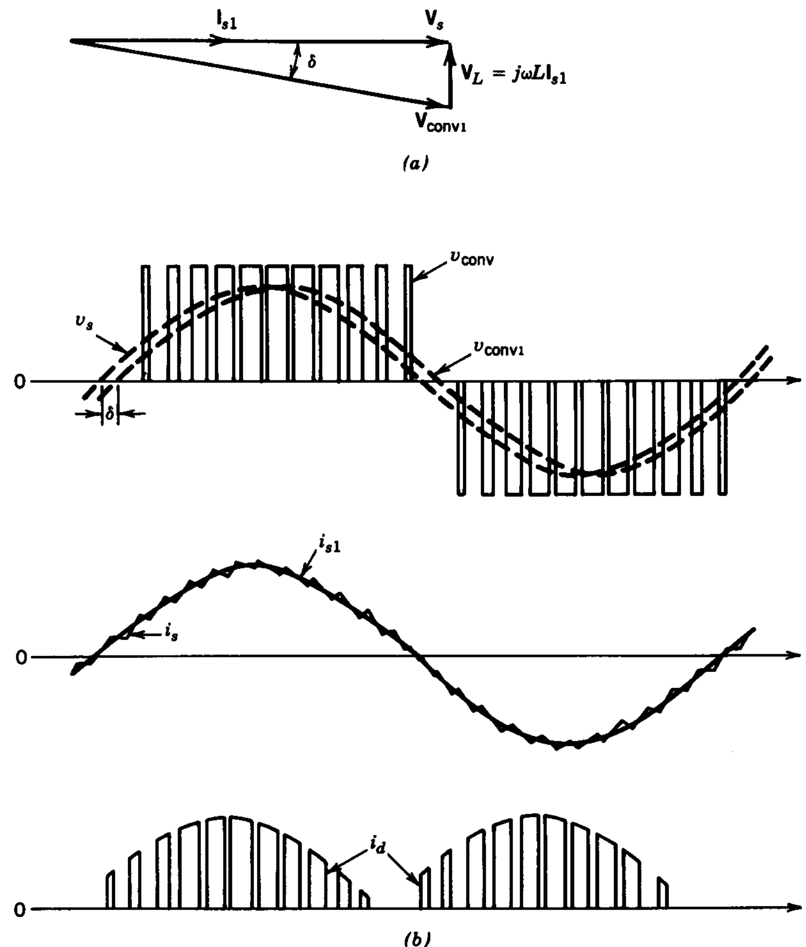

Figure 18-11 Waveforms in the circuit of Fig. 18-8 at unity power factor of operation: (*a*) phasor diagram; (*b*) circuit waveforms.

- Waveforms in the rectifier mode

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3-Phase Switch-Mode Converter Interface

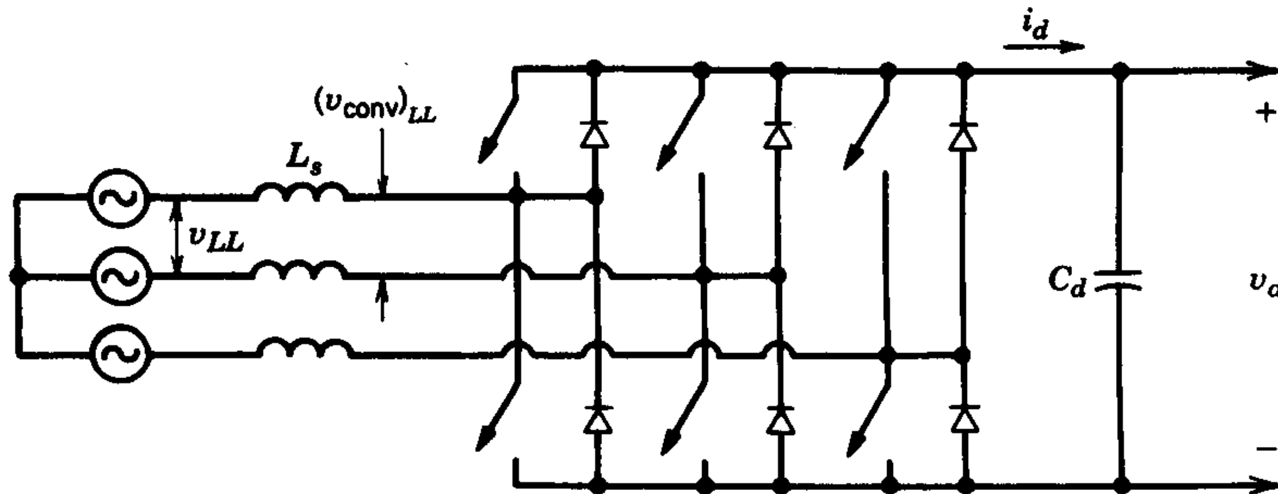

Figure 18-12 Three-phase, switch-mode converter.

- Rectifier and Inverter modes based on the direction of power flow

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EMI: Conducted Interefence

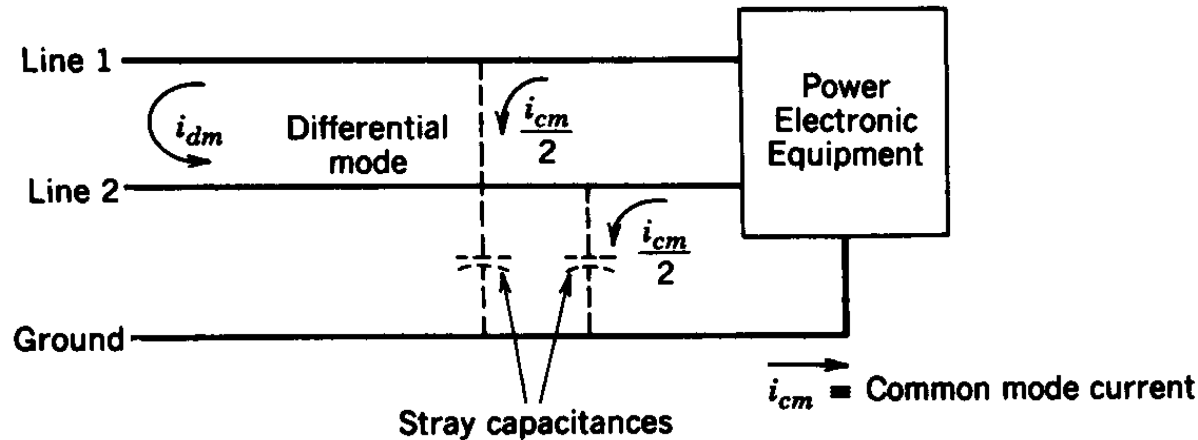

Figure 18-13 Conducted interference.

- Common and differential modes

Switching Waveforms

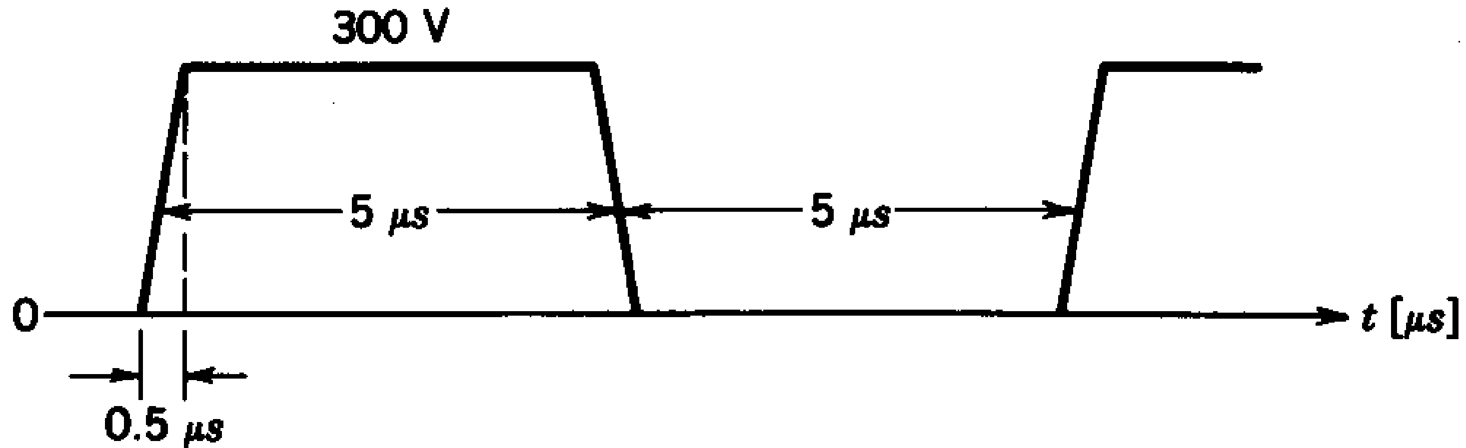

Figure 18-14 Switching waveform.

- Typical rise and fall times

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Conducted EMI

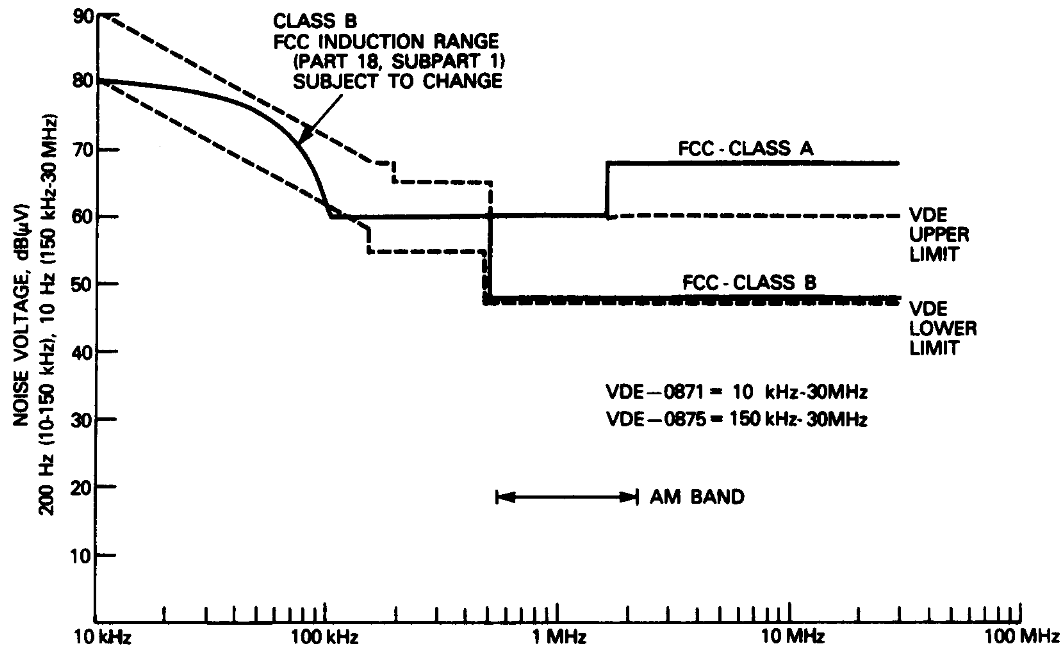

Figure 18-15 The FCC and VDE standards for conducted EMI.

- Various Standards

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Conducted EMI

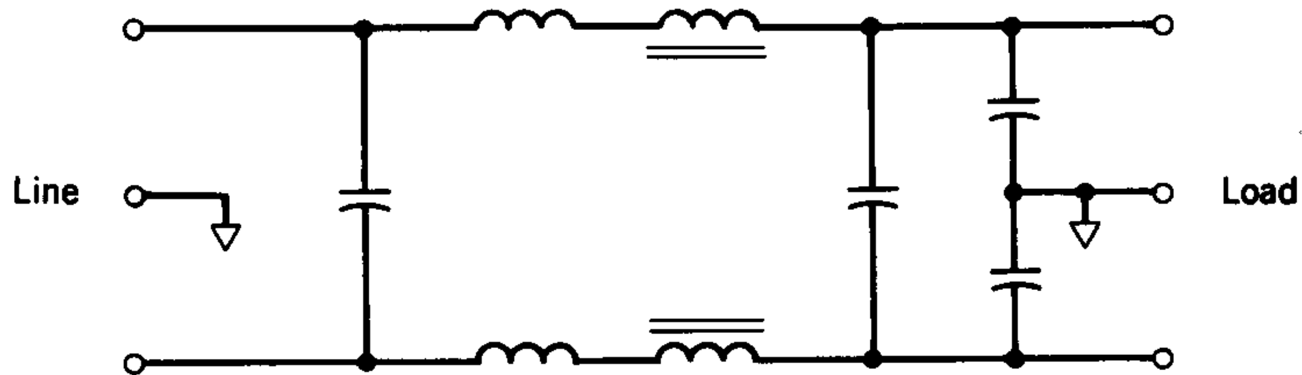

Figure 18-16 Filter for conducted EMI.

- Filter arrangement

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Review of Basic Semiconductor Physics

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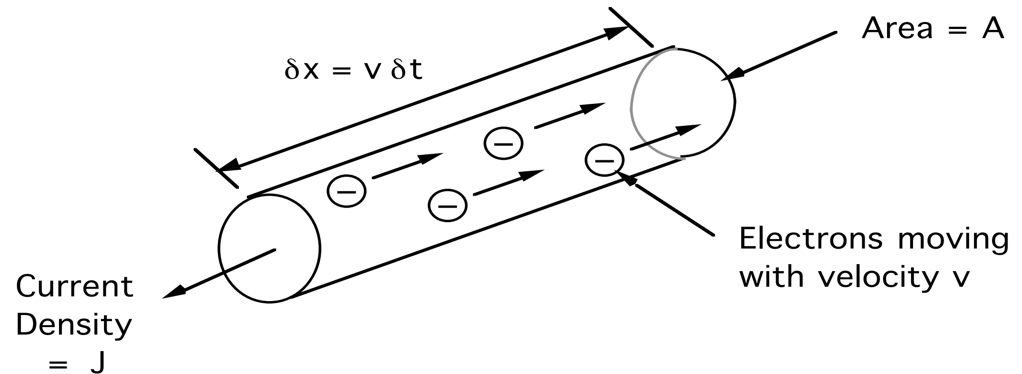
Current Flow and Conductivity

- Charge in volume $A\delta x = \delta Q$

  $= q\, n\, A\, \delta x = q\, n\, A\, v\delta t$

- Current density $J = (\delta Q/\delta t)A^{-1}$
  $= q\, n\, v$



- Metals - gold, platinum, silver, copper, etc.
  - $n = 10^{23}$ cm^{-3} ; $\sigma = 10^{7}$ mhos-cm

- Insulators - silicon dioxide, silicon nitride, aluminum oxide
  - $n < 10^{3}$ cm^{-3} ; $\sigma < 10^{-10}$ mhos-cm

- Semiconductors - silicon, gallium arsenide, diamond, etc.
  - $10^{8} < n < 10^{19}$ cm^{-3} ; $10^{-10} < \sigma < 10^{4}$ mhos-cm

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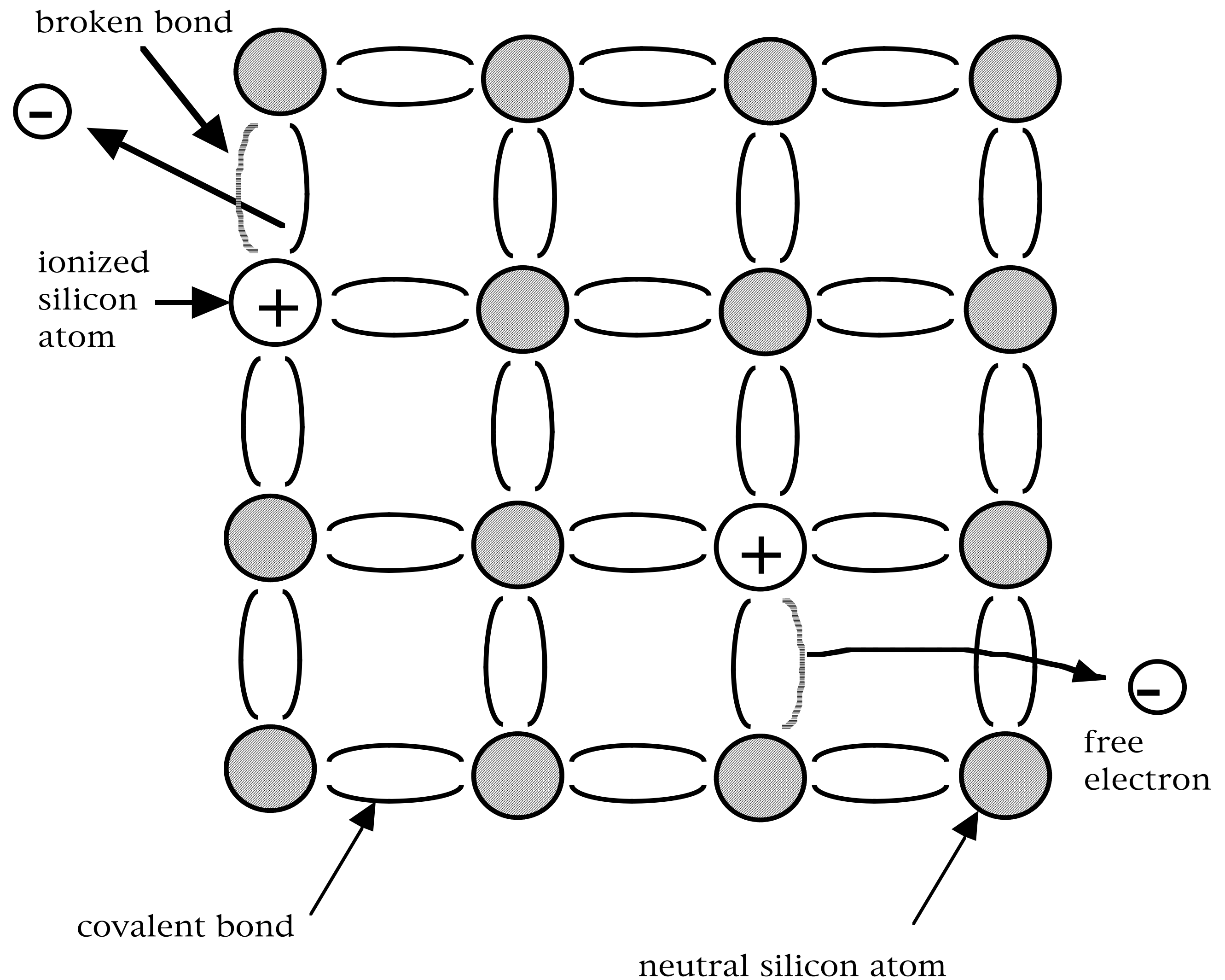
Thermal Ionization

- Si atoms have thermal vibrations about equilibrium point.
- Small percentage of Si atoms have large enough vibrational energy to break covalent bond and liberate an electron.



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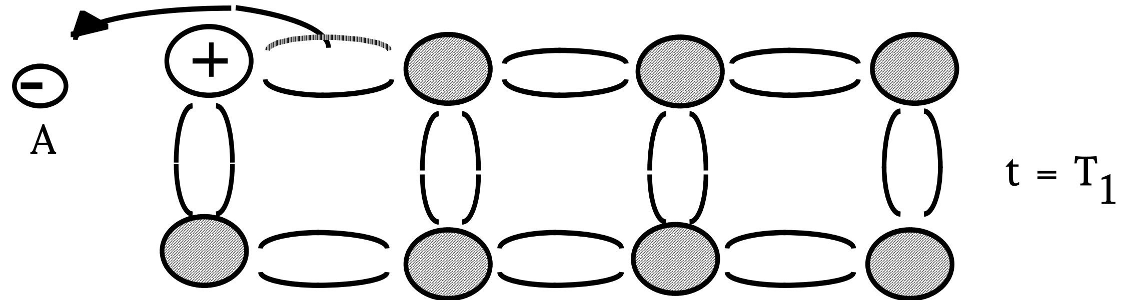
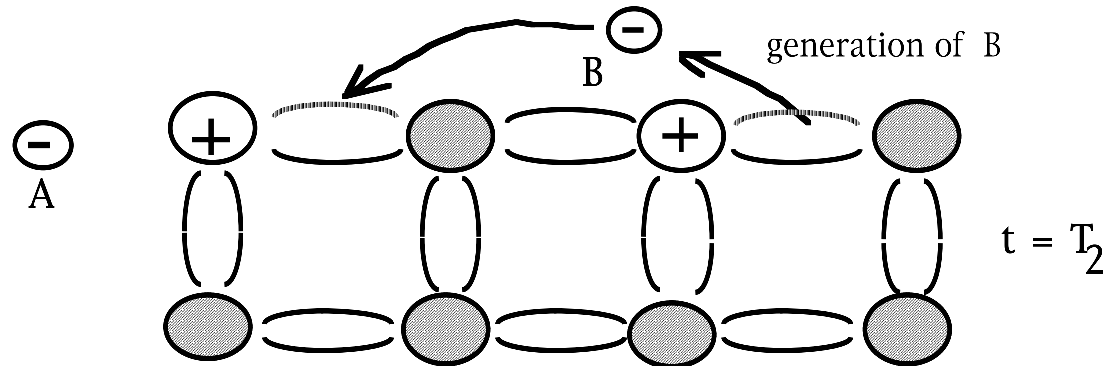
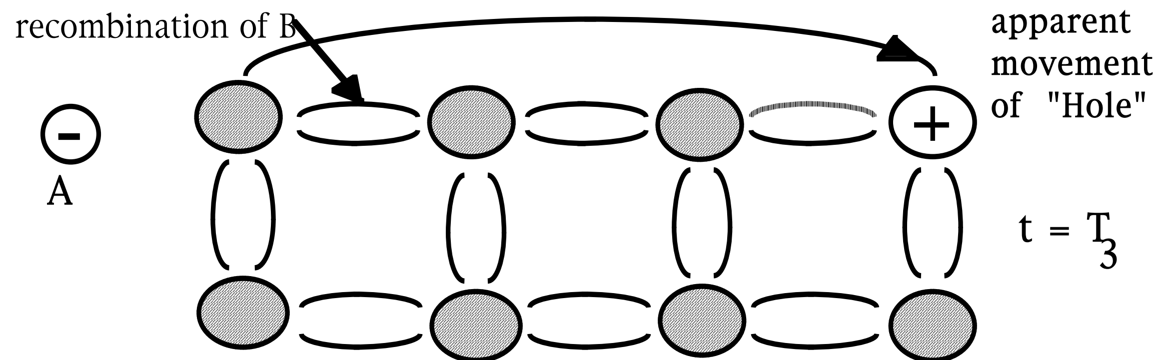
Electrons and Holes

- $T_3 > T_2 > T_1$
- Density of free electrons = n : Density of free holes = p
  - $p = n = n_i(T)$ = intrinsic carrier density.
- $n_i^2(T) = C \exp(-qE_g/(kT))$ = 10^{20} cm^{-6} at 300 K
  - T = temp in K
  - k = 1.4×10^{-23} joules/ K
  - E_g = energy gap = 1.1 eV in silicon
  - q = 1.6×10^{-19} coulombs







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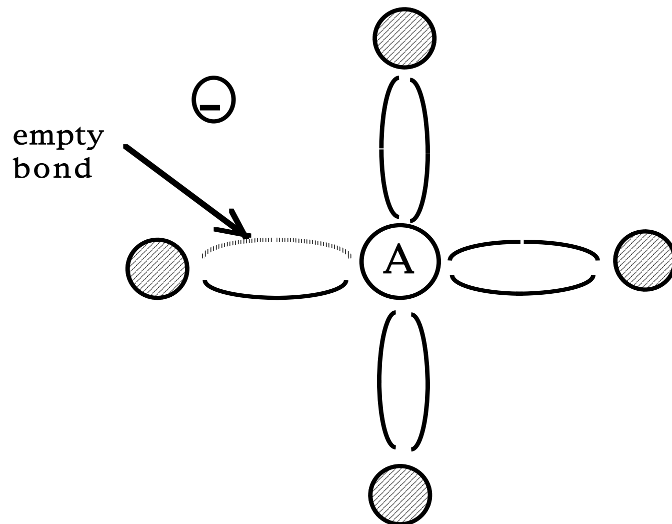
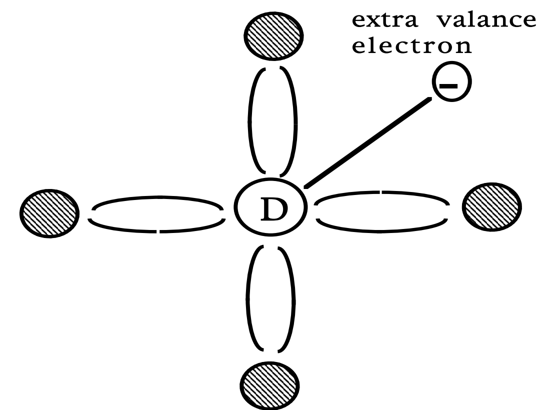
Doped Semiconductors

- Extrinsic (doped) semiconductors: $p = p_o \neq n = n_o \neq n_i$
- Carrier density estimates:
  - Law of mass action $n_o p_o = n_i^2(T)$
  - Charge neutrality $N_a + n_o = N_d + p_o$

- P-type silicon with $N_a >> n_i$:
  $p_o \approx N_a$, $n_o \approx n_i^2 / N_a$



- N-type silicon with $N_d >> n_i$:
  $n_o \approx N_d$, $p_o \approx n_i^2 / N_d$



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Nonequilibrium and Recombination

- Thermal Equilibrium - Carrier generation = Carrier recombination
  - $n = n_o$ and $p = p_o$
- Nonequilibrium - $n > n_o$ and $p > p_o$
  - $n = n_o + \delta n$ and $p = n_o + \delta n$; δn = excess carrier density
  - Excess holes and excess electrons created in equal numbers by breaking of covalent bonds
  - Generation mechanisms -light (photoelectric effect), injection, impact ionization
- Recombination - removal of excess holes and electrons
  - Mechanisms - free electron captured by empty covalent bond (hole) or trapped by impurity or crystal imperfection
  - Rate equation: $d(\delta n)/dt = - \delta n/\tau$
  - Solution $\delta n = \delta n(0)\, e^{-t/\tau}$

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Carrier Lifetimes

- τ = excess carrier lifetime
  - Usually assumed to be constant. Changes in two important situations.
  - τ increases with temperature T
  - τ decreases at large excess carrier densities ; $\tau = \tau_o/[1 + (\delta n/n_b)^2]$

- Control of carrier lifetime values.
  - Switching time-on state loss tradeoff mandates good lifetime control.
  - Control via use of impurities such as gold - lifetime killers.
  - Control via electron irradiation - more uniform and better control.

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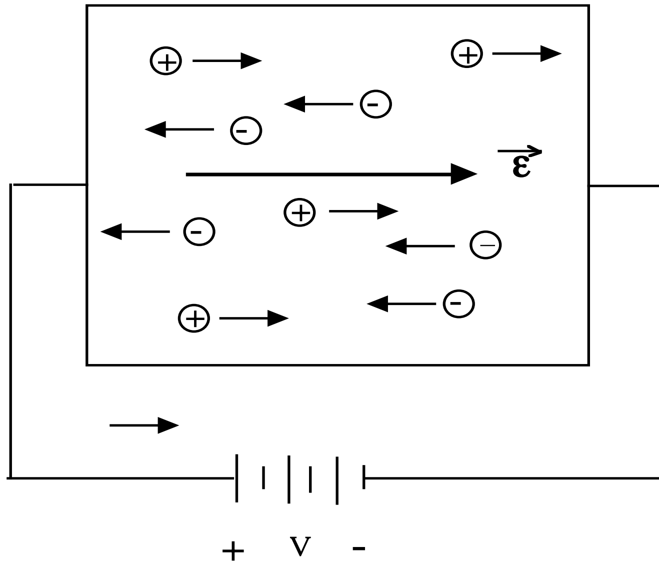
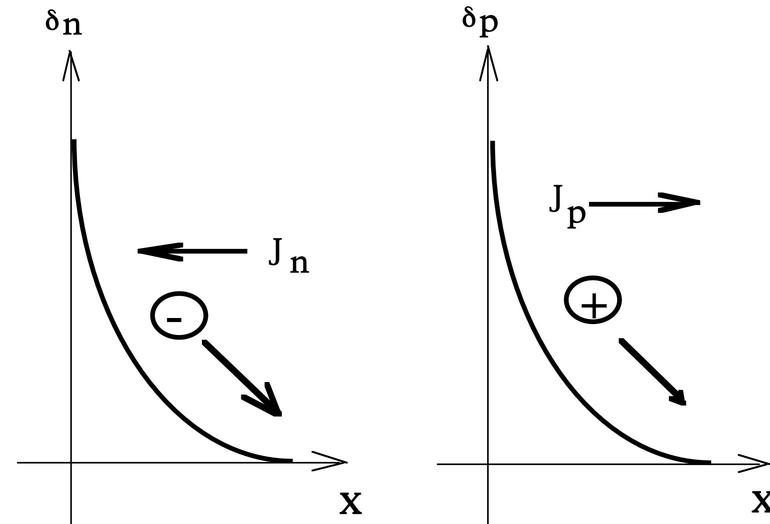
Current Flow

Drift



- $J_{drift} = q\,\mu_n\, n\, E + q\, p\, \mu_p\, E$
- $\mu_n = 1500\ cm^2/V\text{-}sec$ for silicon at room temp. and $N_d < 10^{15}\ cm^{-3}$
- $\mu_p = 500\ cm^2/V\text{-}sec$ for silicon at room temp. and $N_a < 10^{15}\ cm^{-3}$

Diffusion



- $J_{diff} = J_n + J_p = q\, D_n dn/dx - q\, D_p\, dp/dx$
- $D_n/\mu_n = D_p/\mu_p = kT/q$; Einstein relation
- D = diffusion constant, μ = carrier mobility

- Total current density $J = J_{drift} + J_{diff}$

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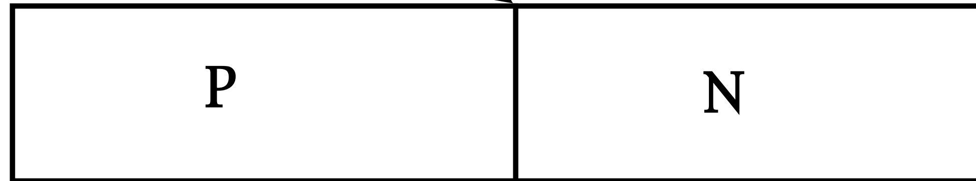
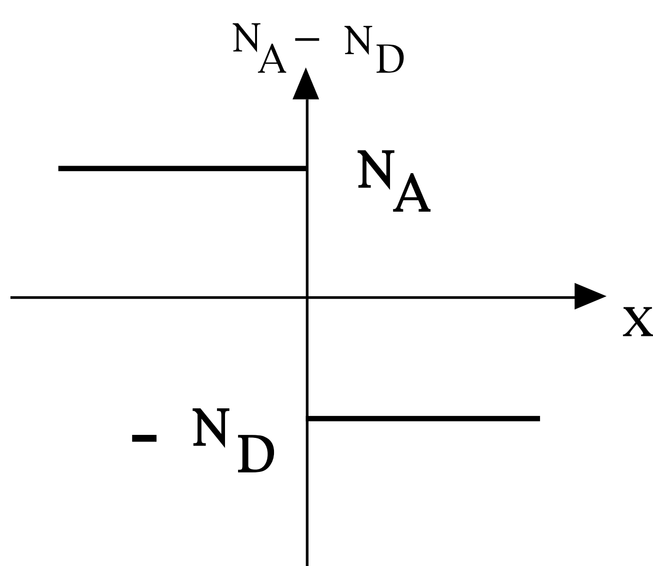
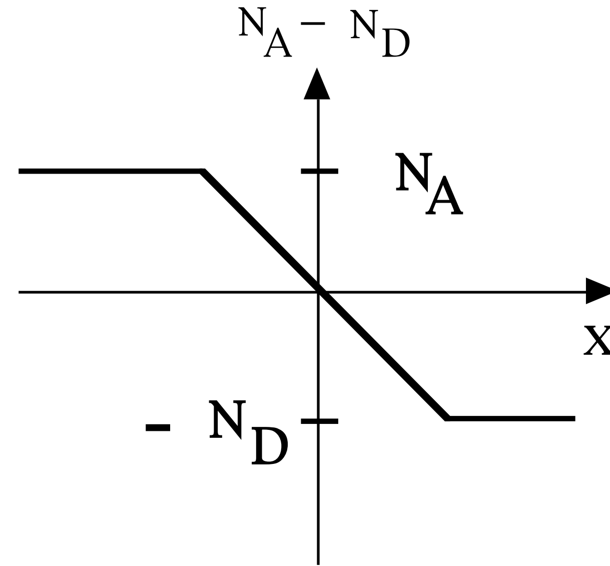
PN Junction





Step (abrupt) junction



Linearly graded junction

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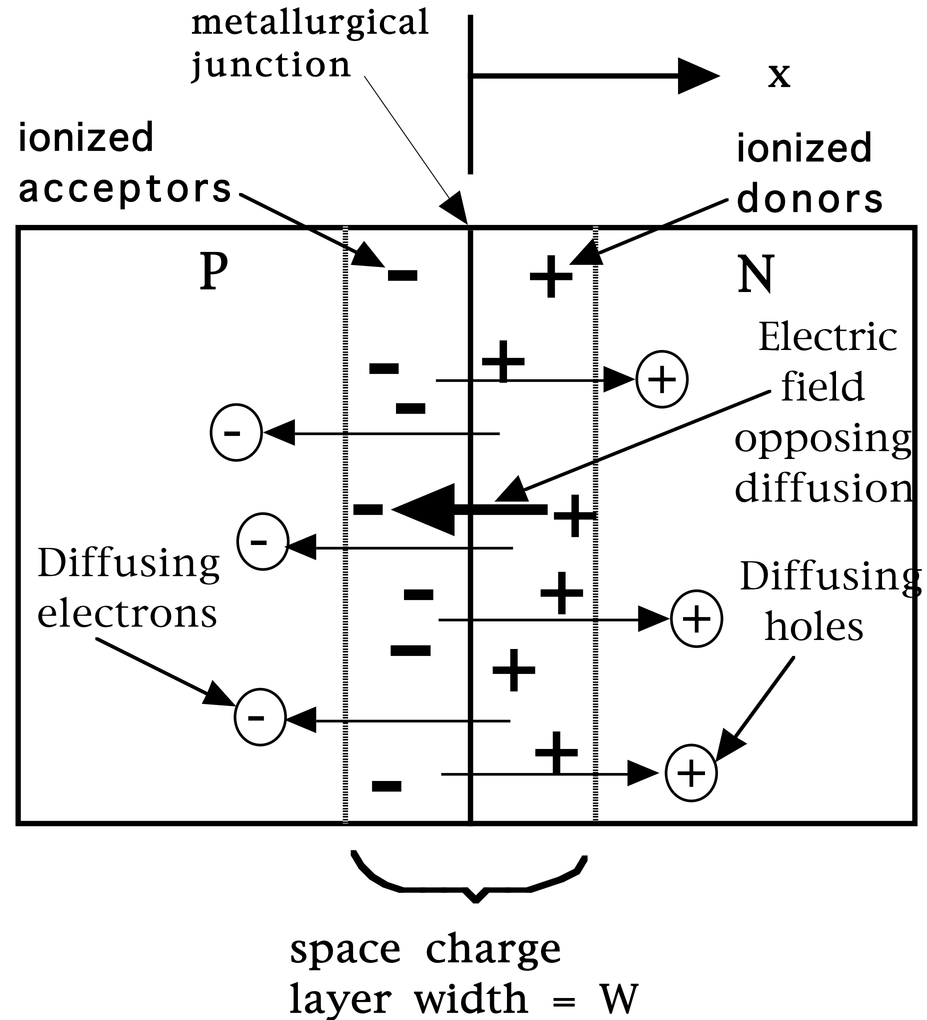
Formation of Space Charge Layer

- Diffusing electrons and holes leave the region near metallurgical junction depleted of free carriers (depletion region).
- Exposed ionized impurities form space charge layer.
- Electric field due to space charge opposes diffusion.



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Quantitative Description of Space Charge Region

- Assume step junction.

$$\frac{d^2\Phi}{dx^2} = -\frac{\rho}{\varepsilon}$$

$$\rho = -qN_a \quad ; \ x < 0$$

$$\rho = qN_d \quad ; \ x > 0$$

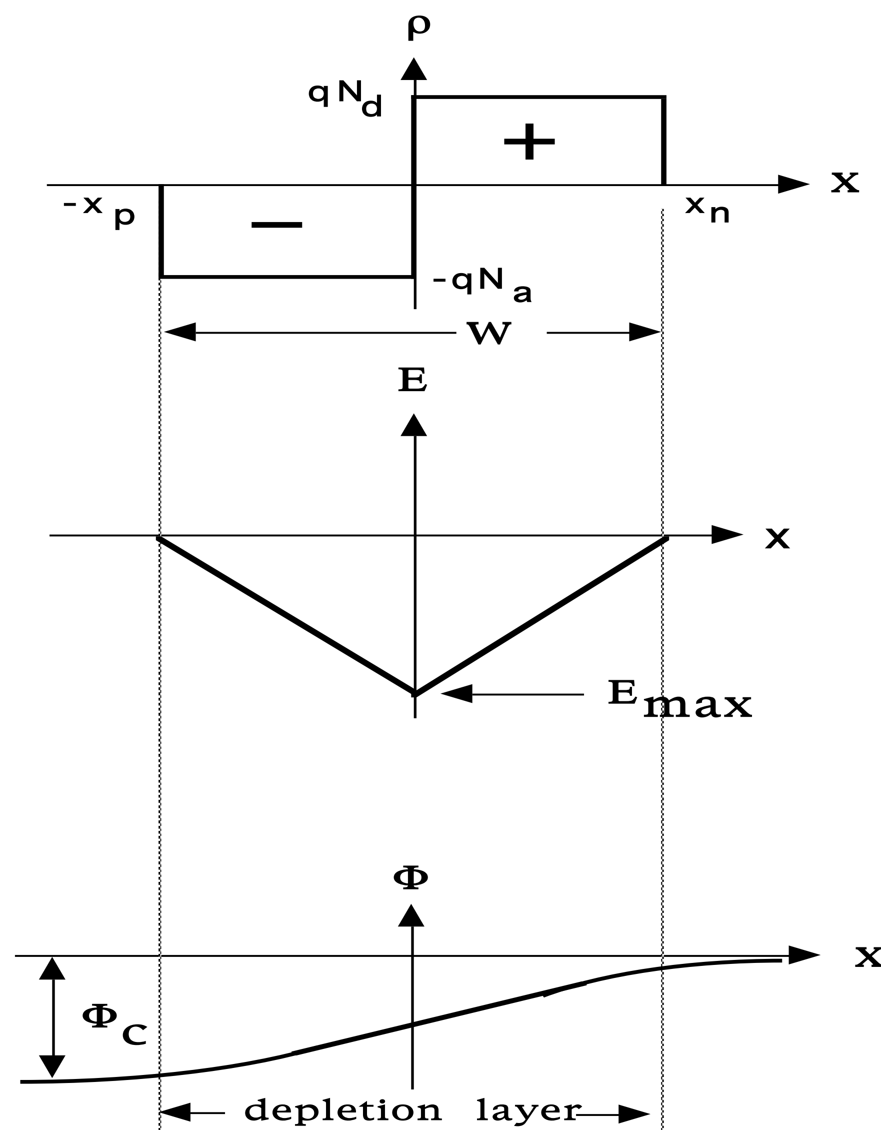
$$\frac{d\Phi}{dx} = -E(x)$$

$$E(x) = \frac{qN_a(x+x_p)}{\varepsilon} ; -x_p < x < 0$$

$$E(x) = \frac{qN_d(x-x_n)}{\varepsilon} ; 0 < x < x_n$$

$$\Phi_c = -\int_{-x_p}^{x_n} E(x)dx$$

$$\Phi_c = -\frac{qN_a x_p^2 + qN_d x_n^2}{2\varepsilon}$$



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Contact (Built-in, Junction) Potential

- In thermal equilibrium $J_n = q\,\mu_n\, n \frac{d\Phi}{dx} + q\, D_n \frac{dn}{dx} = 0$

- Separate variables and integrate ; $\int_{\Phi(x_p)}^{\Phi(x_n)} d\Phi = -\frac{D_n}{\mu_n} \int_{n(x_p)}^{n(x_n)} \frac{dn}{n}$

- $\Phi(x_n) - \Phi(x_p) = \Phi_c = \frac{kT}{q} \ln\left[\frac{N_a N_d}{n_i^2}\right]$; Φ_c = contact potential

- Example

  - Room temperature kT/q = 0.025 eV
  - $N_a = N_d = 10^{16}\ cm^{-3}$; $n_i^2 = 10^{20}\ cm^{-6}$
  - F_c = 0.72 eV

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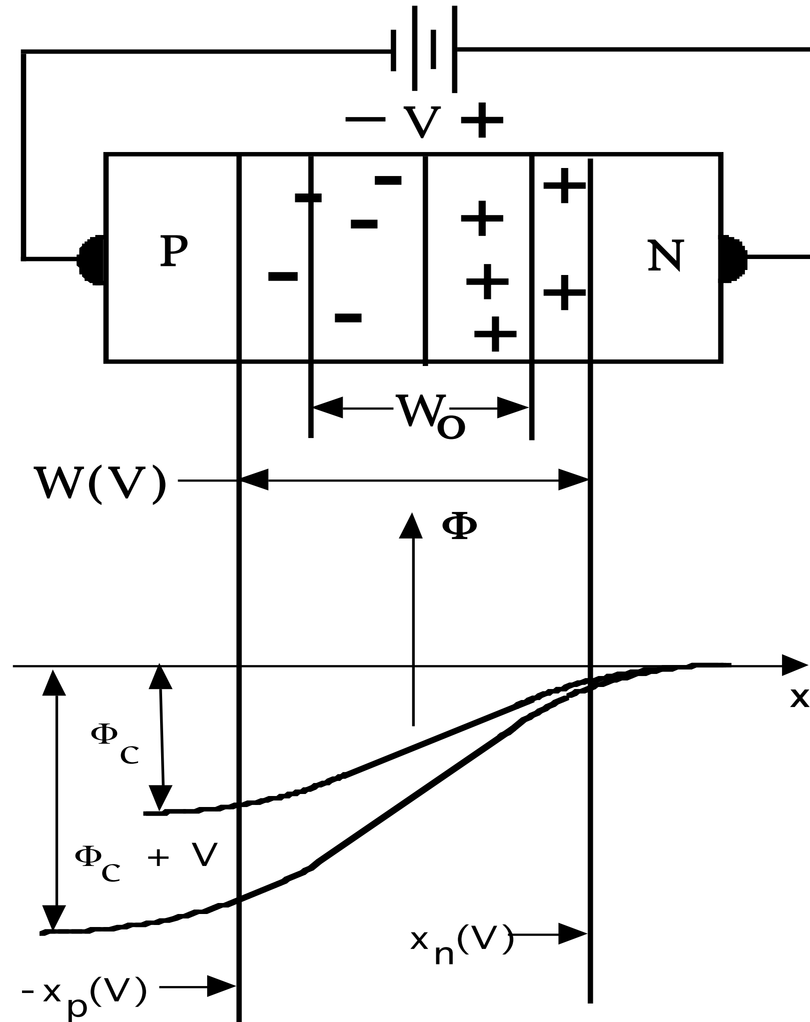
Reverse-Biased Step Junction

- Starting equations
  - $W(V) = x_n(V) + x_p(V)$
  - $V + \Phi_c = -\dfrac{qN_a x_p^2 + qN_d x_n^2}{2\varepsilon}$
  - Charge neutrality $qN_a x_p = qN_d x_n$
- Solve equations simultaneously
  - $W(V) = W_o\sqrt{1+V/\Phi_c}$
  - $W_o = \sqrt{\dfrac{2\varepsilon\Phi_c(N_a+N_d)}{qN_aN_d}}$
  - $E_{max} = \dfrac{2\Phi_c}{W_o}\sqrt{1 + V/\Phi_c}$



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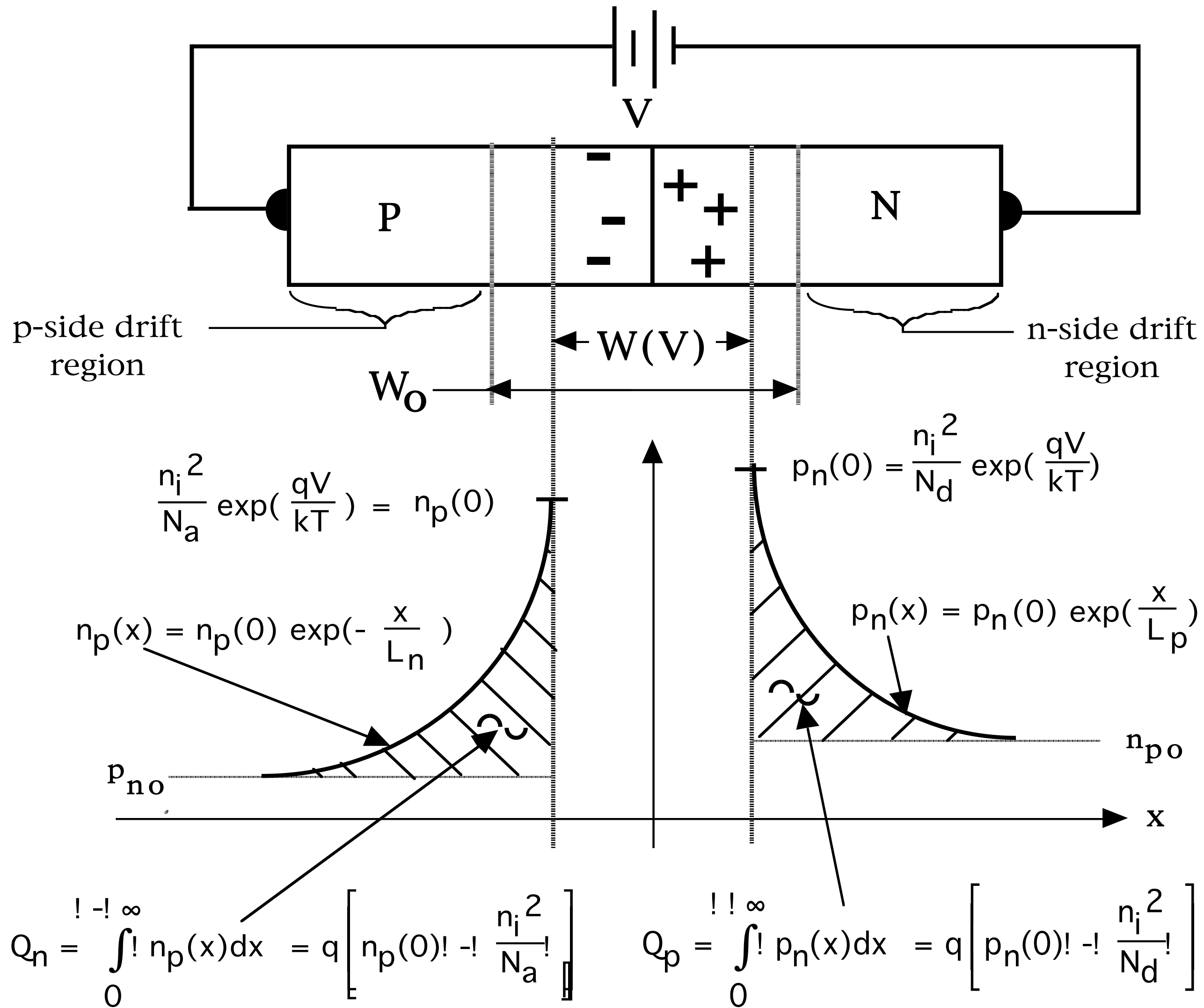
Forward-Biased PN Junction



- Forward bias favors diffusion over drift.
- Excess minority carrier injection into both p and n drift regions.
- Minority carrier diffusion lengths.
  - $L_n = [D_n \tau_n]^{0.5}$
  - $L_p = [D_p \tau_p]^{0.5}$

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Ideal PN Junction I-V Characteristics

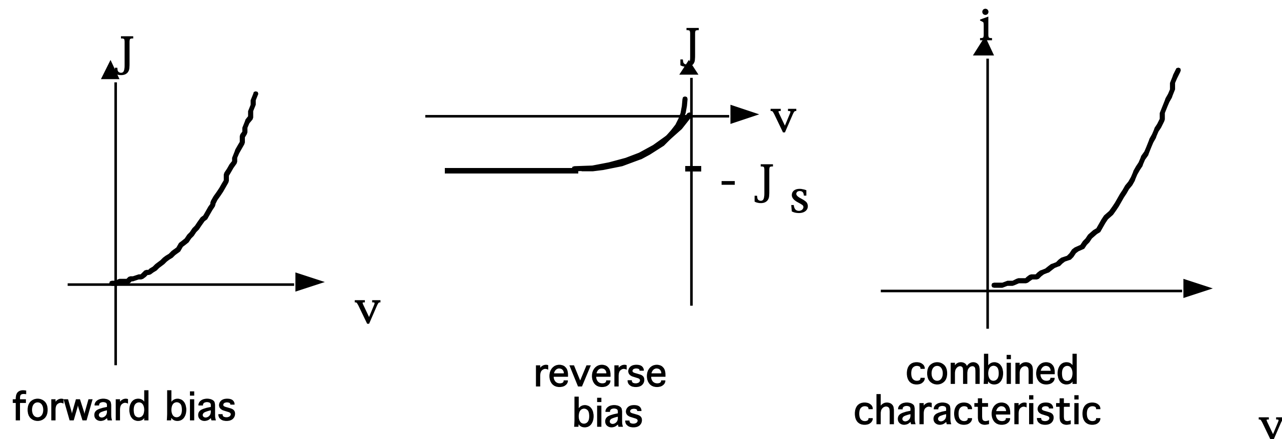
- Excess carriers in drift regions recombined and thus more must be constantly injected if the distributions np(x) and pn(x) are to be maintained.

`

- Constant injection of electrons and holes results in a current density J given by

$$J = \frac{Q_n}{\tau_n} + \frac{Q_p}{\tau_p} = q\, n_i^2 \left[\frac{L_n}{N_a \tau_n} + \frac{L_p}{N_d \tau_p}\right] \left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$J = J_s \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \;;\; J_s = q\, n_i^2 \left[\frac{L_n}{N_a \tau_n} + \frac{L_p}{N_d \tau_p}\right]$$



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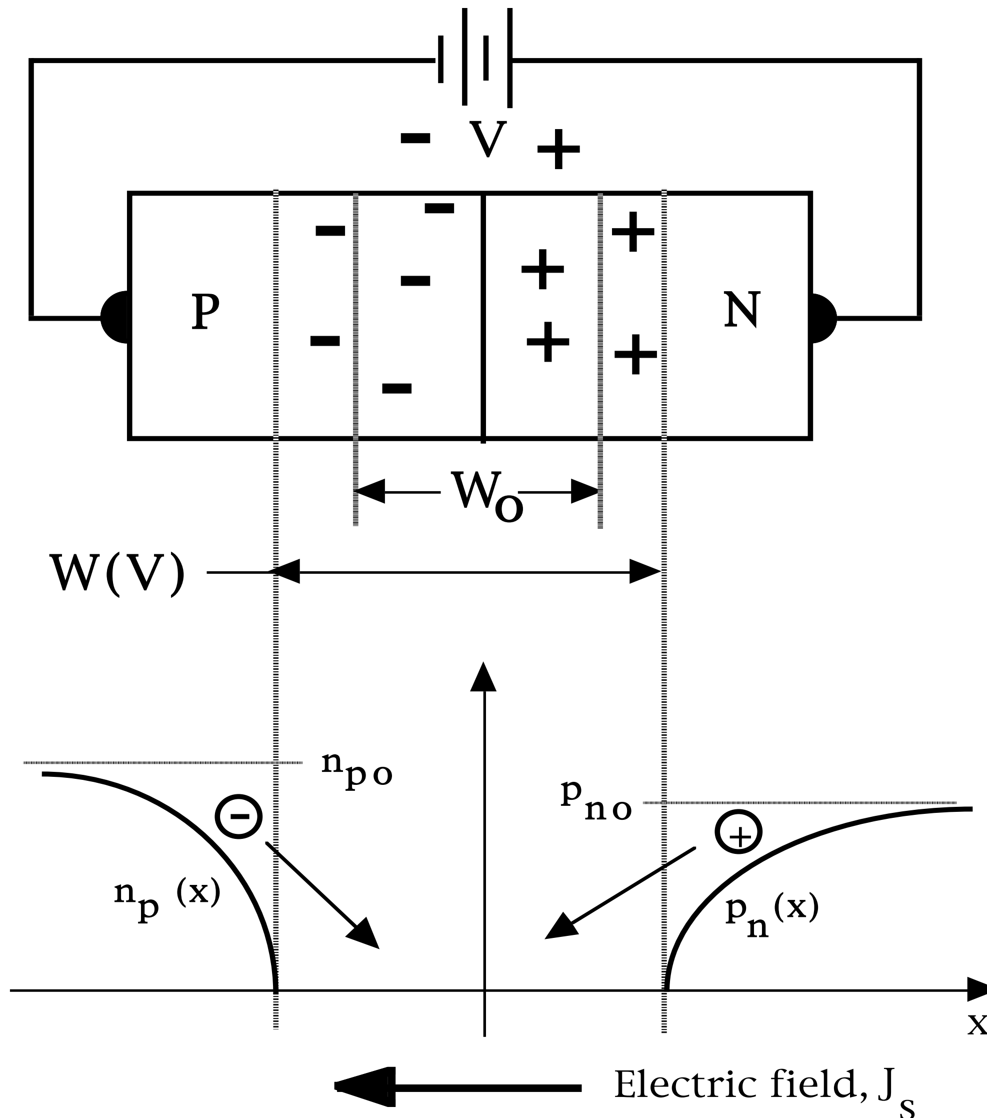
Reverse Saturation Current



- Carrier density gradient immediately adjacent to depletion region causes reverse saturation current to flow via diffusion.
- J_s independent of reverse voltage V because carrier density gradient unaffected by applied voltage.
- J_s extremely temperature sensitivity because of dependence on n_i^2(T.)

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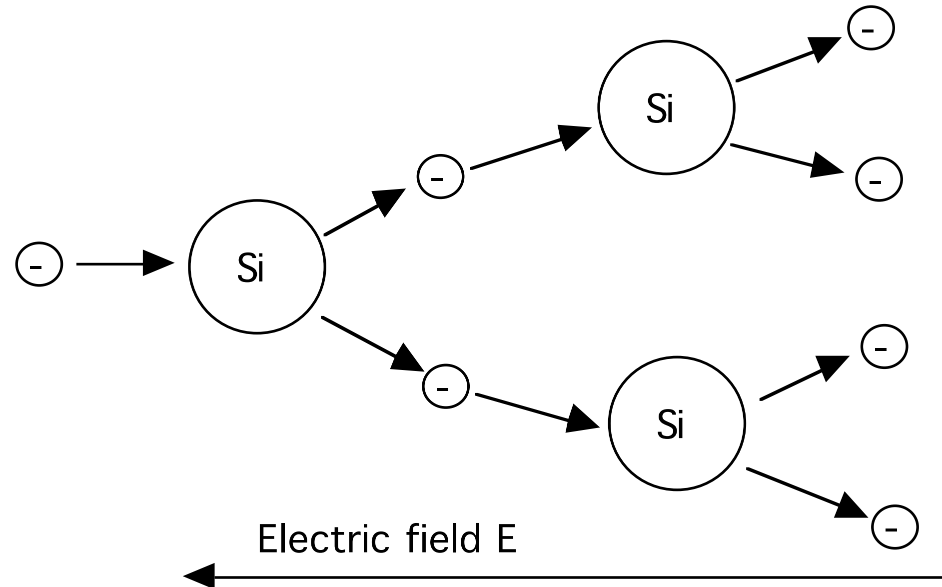
Impact Ionization

- $E \geq E_{BD}$; free electron can acquire sufficient from the field between lattice collisions ($t_c \approx 10^{-12}$ sec) to break covalent bond.
- Energy = $0.5mv^2 = q\,E_g$; $v = q\,E_{BD}t_c$



- Solving for E_{BD} gives

$$E_{BD} = \sqrt{\frac{2!\,E_g!\,m}{q!\,t_c{}^2}}$$

- Numerical evaluation
  - $m = 10^{-27}$ grams, $E_g = 1.1$ eV, $t_c = 10^{-12}$ sec.
  - $E_{BD} = \sqrt{\frac{(2)!\,(1.1)!\,(10^{27})}{(1.6\text{x}10^{-19})!\,(10^{-24})}} = 3\text{x}10^5$ V/cm
    - Experimental estimates are 2-3.5x10^5 V/cm

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Lecture Notes

Diodes for Power Electronic Applications

OUTLINE

- PN junction power diode construction
- Breakdown voltage considerations
- On-state losses
- Switching characteristics
- Schottky diodes
- Modeling diode behavior with PSPICE

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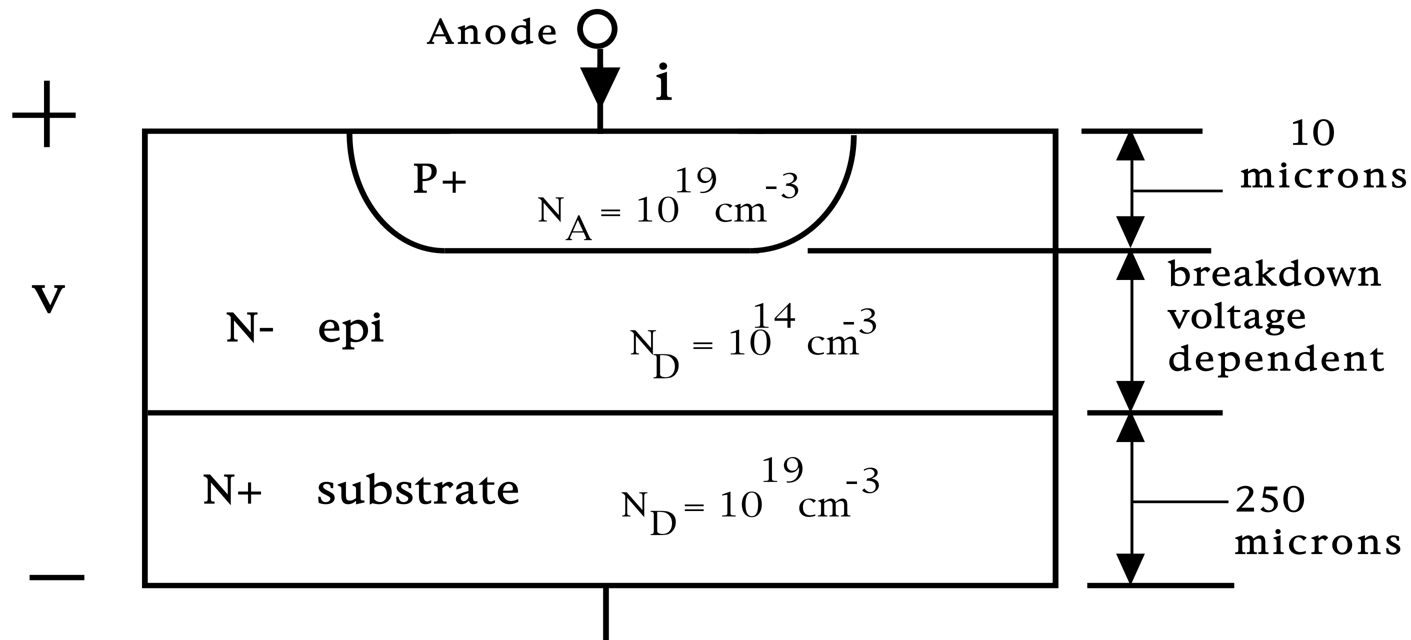
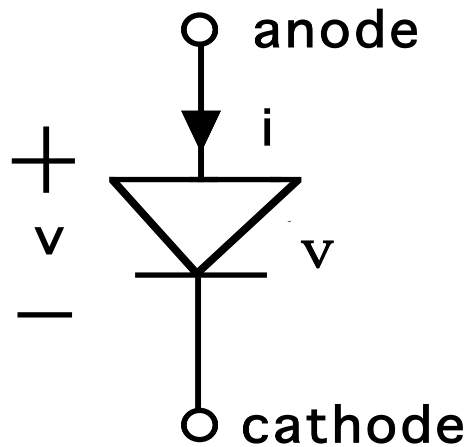
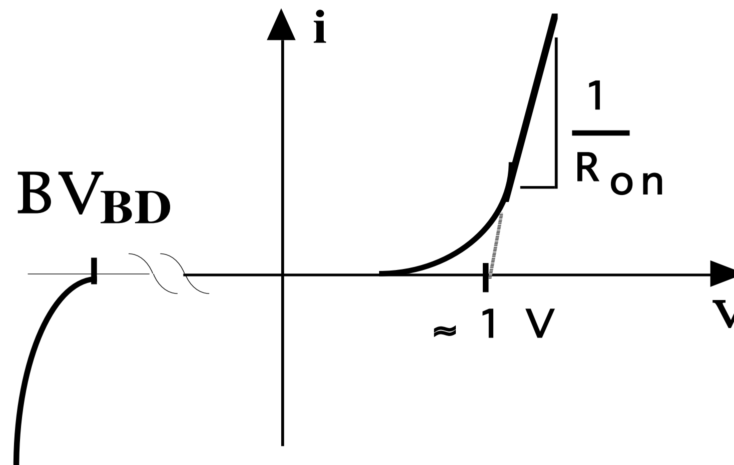
Basic Structure of Power Semiconductor Diodes







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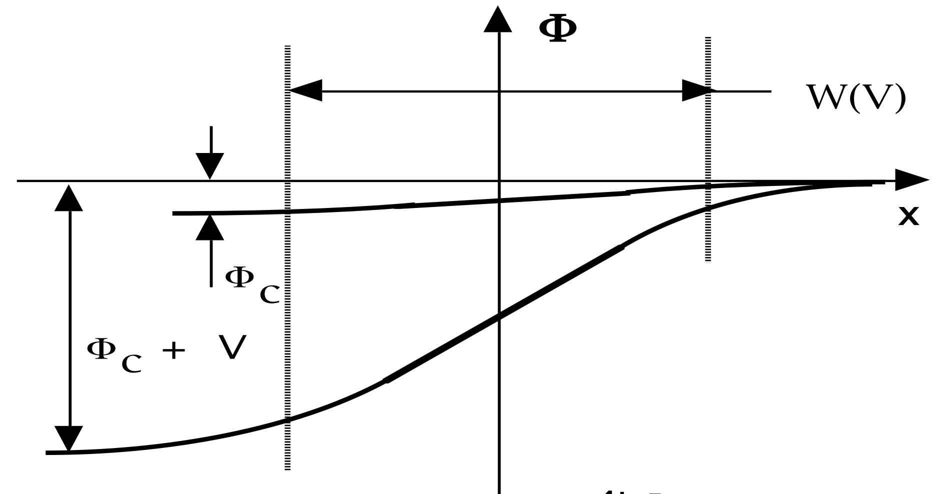
Breakdown Voltage Estimate - Step Junction



- Non-punch-through diode. Drift region length $W_d > W(BV_{BD})$ = length of space charge region at breakdown.

- $W(V) = W_o\sqrt{1+V/\Phi_c}$

- $W_o = \sqrt{\dfrac{2\varepsilon\Phi_c(N_a+N_d)}{qN_aN_d}}$

- $E_{max} = \dfrac{2\Phi_c}{W_o}\sqrt{1! +! V/\Phi_c}$

- Power diode at reverse breakdown: $N_a >> N_d$; $E = E_{BD}$; $V = BV_{BD} >> \Phi_c$

- $W^2(BV_{BD}) = \dfrac{W_o{}^2! BV_{BD}}{\Phi_c}$; $W_o{}^2 = \dfrac{2\varepsilon\Phi_c}{q! N_d}$

- $(E_{max})^2 = (E_{BD})^2 = \dfrac{4! \Phi_c}{W_o{}^2} BV_{BD}$

- Solve for $W(BV_{BD})$ and BV_{BD} to obtain (put in Si values)

  $BV_{BD} = \dfrac{\varepsilon! E_{BD}{}^2}{2! q! N_d} = \dfrac{1.3x10^{17}}{N_d}$; [V]

  $W(BV_{BD}) = \dfrac{2! BV_{BD}}{E_{BD}} = 10^{-5} BV_{BD}$; [μm]

- Conclusions

  1. Large BV_{BD} (10^3 V) requires $N_d < 10^{15}$ cm^{-3}

  2. Large BV_{BD} (10^3 V) requires N^- drift region > 100 μm

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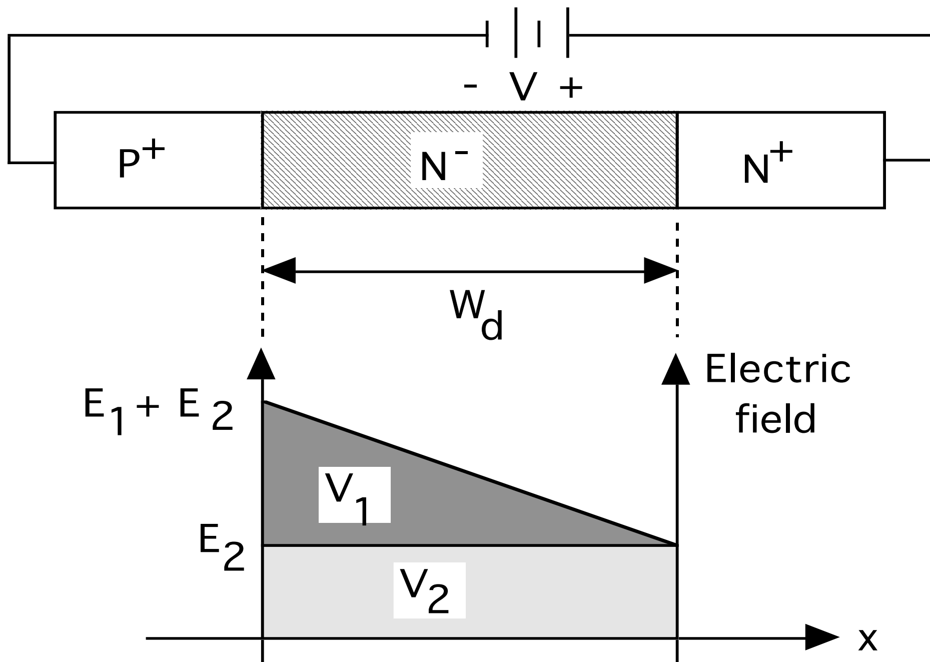
Breakdown Voltage - Punch-Through Step Junction

- Punch-through step junction - $W(BV_{BD}) > W_d$



- $E_1 = \frac{qN_dW_d}{\varepsilon}$; $V_1 = \frac{qN_dW_d^2}{2\varepsilon}$
- $V_2 = E_2 W_d$

- At breakdown:
  - $V_1 + V_2 = BV_{BD}$
  - $E_1 + E_2 = E_{BD}$
- $BV_{BD} = E_{BD} W_d - \frac{qN_dW_d^2}{2\varepsilon}$
- If $N_d << \frac{\varepsilon(EBD)^2}{2q(BV_{BD})}$ (required value of N_d for non-punch-thru diode), then
  - $BV_{BD} \approx E_{BD} W_d$ and
  - W_d(Punch-thru) $\approx 0.5\ W_d$(non-punch-thru)

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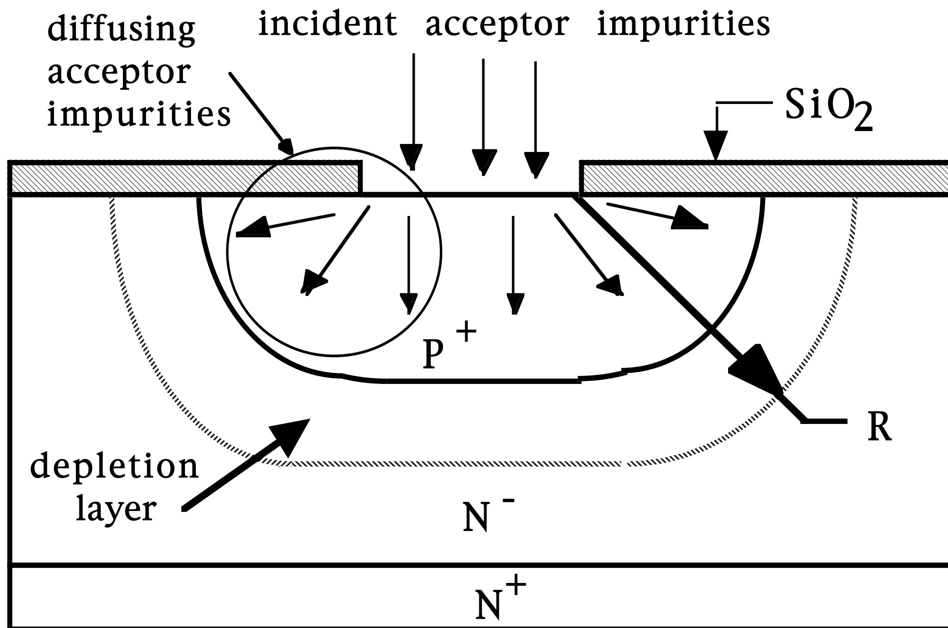
Effect of Space Charge Layer Curvature



- Impurities diffuse as fast laterally as vertically
- Curvature develops in junction boundary and in depletion layer.

- If radius of curvature is comparable to depletion layer thickness, electric field becomes spatially nonuniform.
- Spatially nonuniform electric field reduces breakdown voltage.
- R > 6 W(BV_{BD}) in order to limit breakdown voltage reduction to 10% or less.
- Not feasible to keep R large if BV_{BD} is to be large (> 1000 V).

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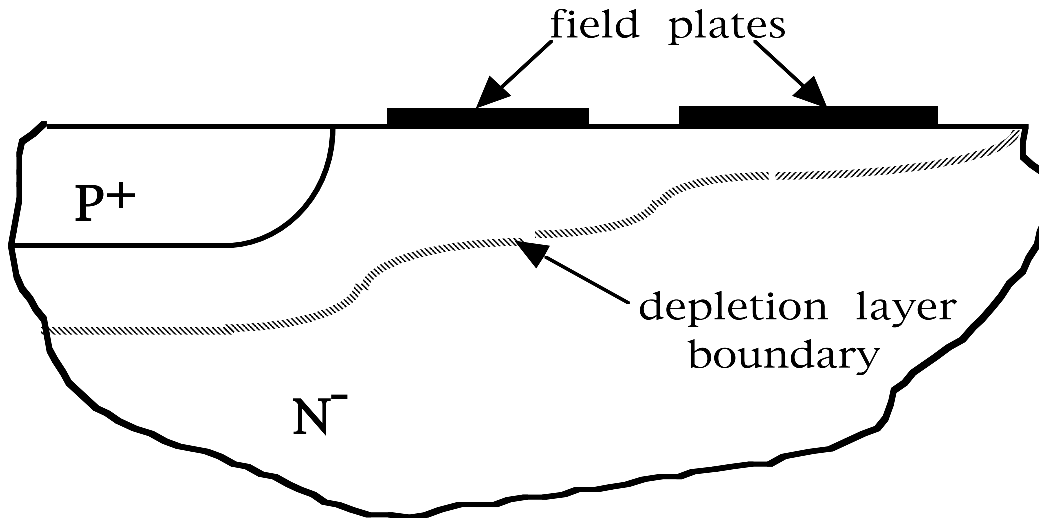
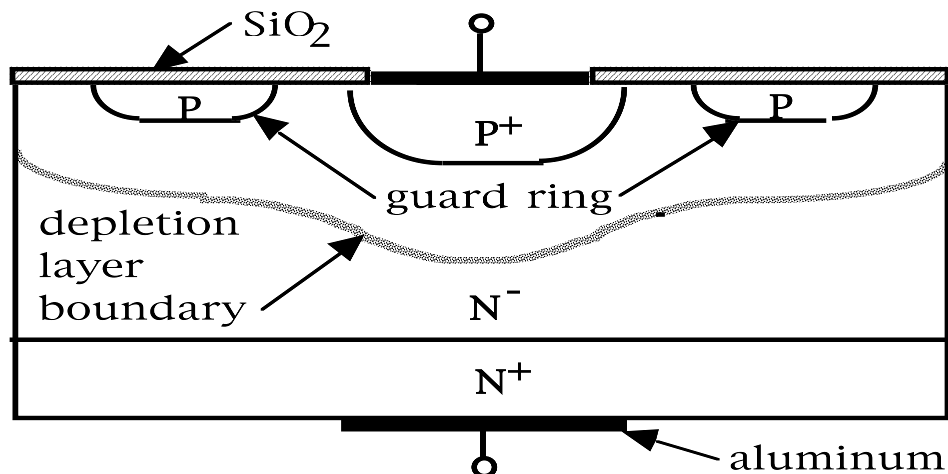
Control of Space Charge Layer Boundary Contour



- Electrically isolated conductors (field plates) act as equipotential surfaces.
- Correct placement can force depletion layer boundary to have larger radius of curvature and t;hus minimize field crowding.



- Electrically isolated p-regions (guard rings)has depletion regions which interact with depletion region of main pn junction.
- Correct placement of guard rings can result in composite depletion region boundary having large radius of curvature and thus minimize field crowding.

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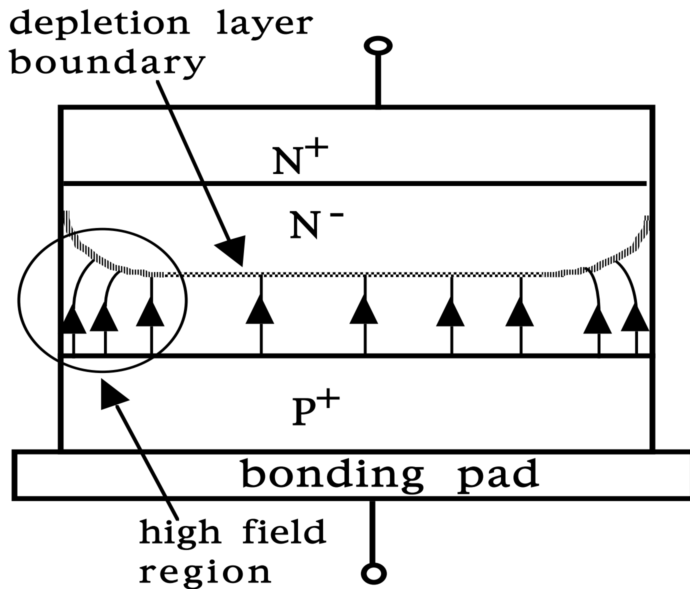
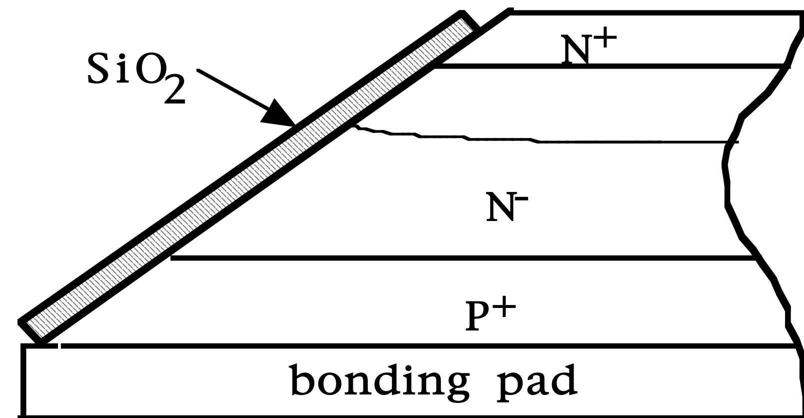
Surface Contouring to Minimize Field Crowding





- Large area diodes have depletion layers that contact Si surface.
- Difference in dielectric constant of Si and air causes field crowding at surface.
- Electric fields fringing out into air attract impurities to surface that can lower breakdown voltage.

- Proper contouring of surface can mimimize depletion layer curvature and thus field crowding.
- Use of a passivation layer like SiO_2 can also help minimize field crowding and also contain fringing fields and thus prevent attraction of impurities to surface.

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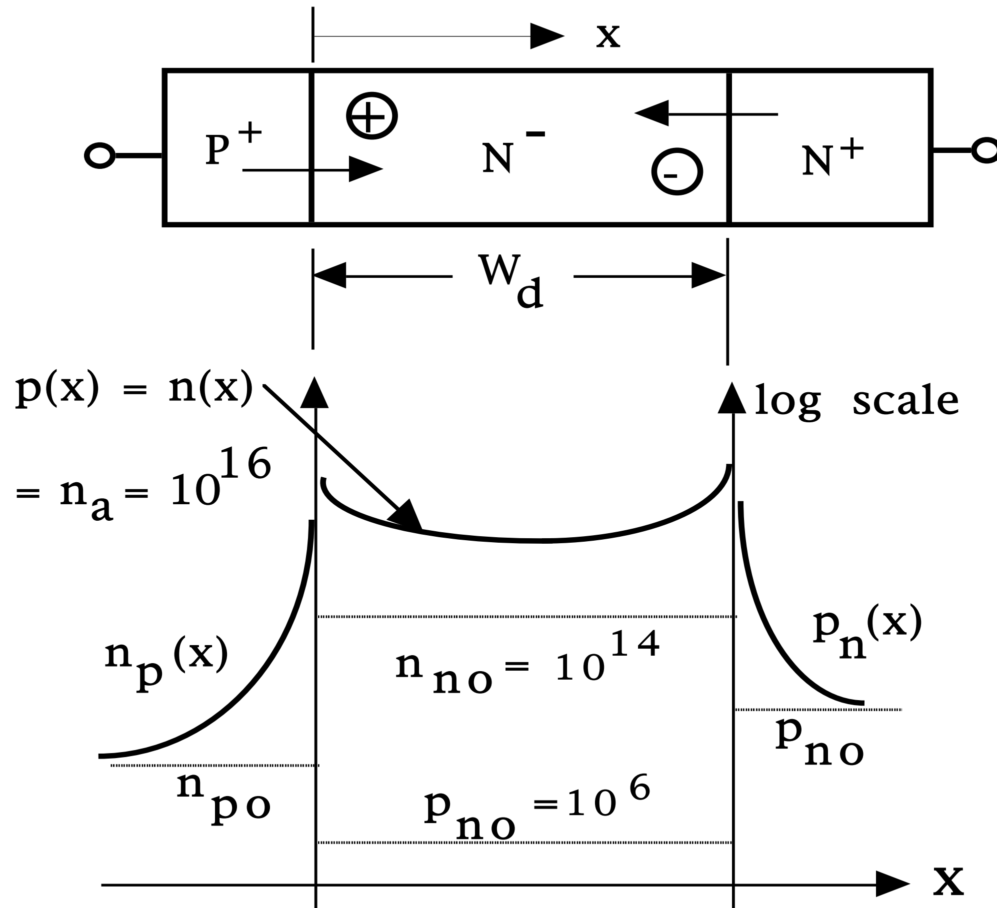
Conductivity Modulation of Drift Region



- Forward bias injects holes into drift region from P^+ layer. Electrons attracted into drift region from N^+ layer. So-called double injection.

- If $W_d \leq$ high level diffusion length L_a, carrier distributions quite flat with $p(x) \approx n(x) \approx n_a$.

- For n_a >> drift region doping N_d, the resistance of the drift region will be quite small. So-called conductivity modulation.

- On-state losses greatly reduced below those estimated on basis of drift region low-level (N_d) ohmic conductivity.

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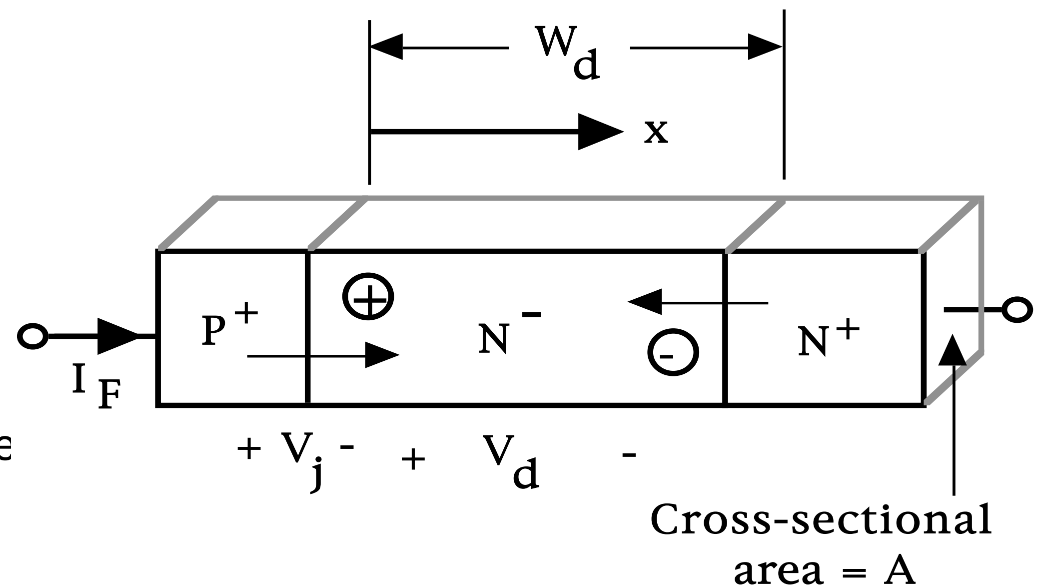
Drift Region On-State Voltage Estimate

- $I_F = \frac{Q_F}{\tau} = \frac{q\! A\! W_d\! n_a}{\tau}$; Current needed to maintain stored charge Q_F.

- $I_F = \frac{q\! [\mu_{n\!} +\! \mu_p]\! n_a\! A\! V_d}{W_d}$;
  Ohm's Law ($J = \sigma E$)

- $V_d = \frac{{W_d}^2}{\! [\mu_{n\!} +\! \mu_p]\! \tau}$; Equate above two equations and solve for V_d

- Conclusion: long lifetime τ minimizes V_d.



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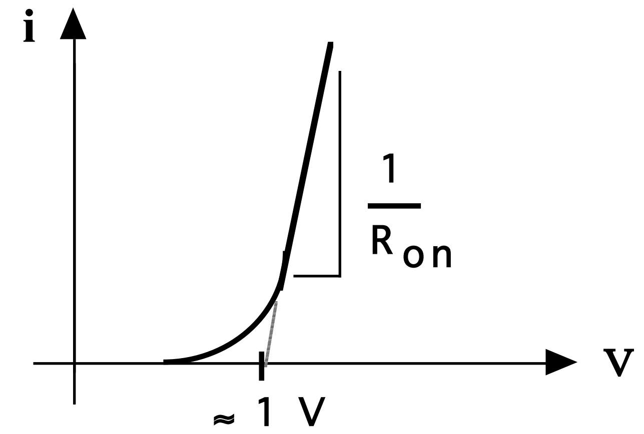
Diode On-State Voltage at Large Forward Currents

- $\mu_n + \mu_p = \dfrac{\mu_o}{1! +! \dfrac{n_a}{n_b}}$; $n_b \approx 10^{17}$ cm^{-3} .
  - Mobility reduction due to increased carrier-carrier scattering at large n_a.

- $I_F = \dfrac{q!\, n_a!\, A!\, V_d}{W_d} \dfrac{\mu_o}{1! +! \dfrac{n_a}{n_b}}$; Ohms Law

  with density-dependent mobility.

- Invert Ohm's Law equation to find V_d as function I_F assuming $n_a >> n_b$.



- $V_d = \dfrac{I_f!\, W_d}{q!\, \mu_o!\, n_b!\, A}$

- $V_d = I_F R_{on}$

- $V = V_j + V_d$

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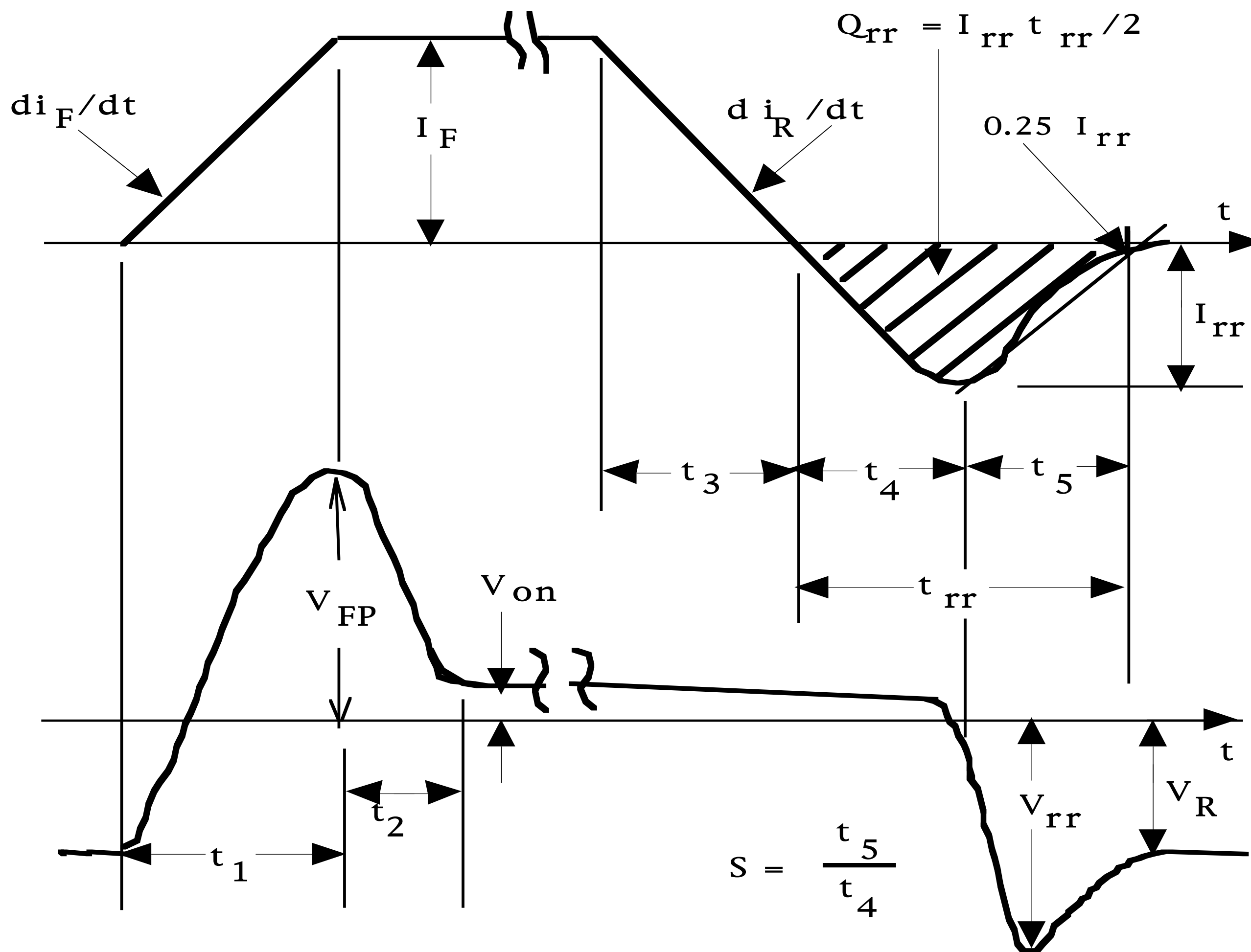
Diode Switching Waveforms in Power Circuits



- $\frac{di_F}{dt}$ and $\frac{di_R}{dt}$ determined by external circuit.
- Inductances or power semiconductor devices.

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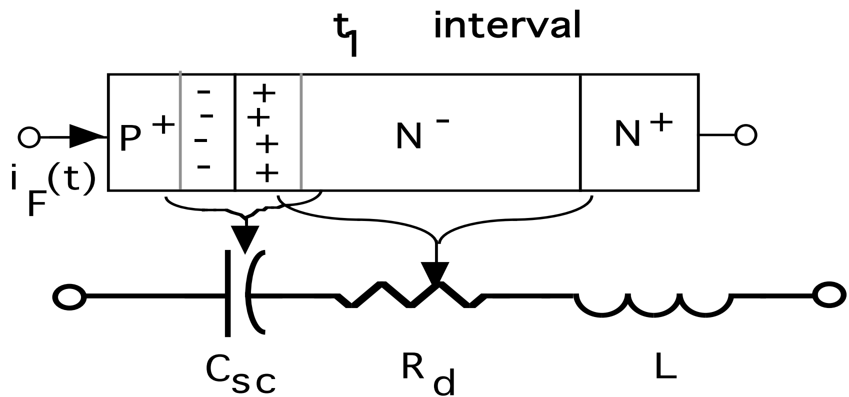
Diode Internal Behavior During Turn-on

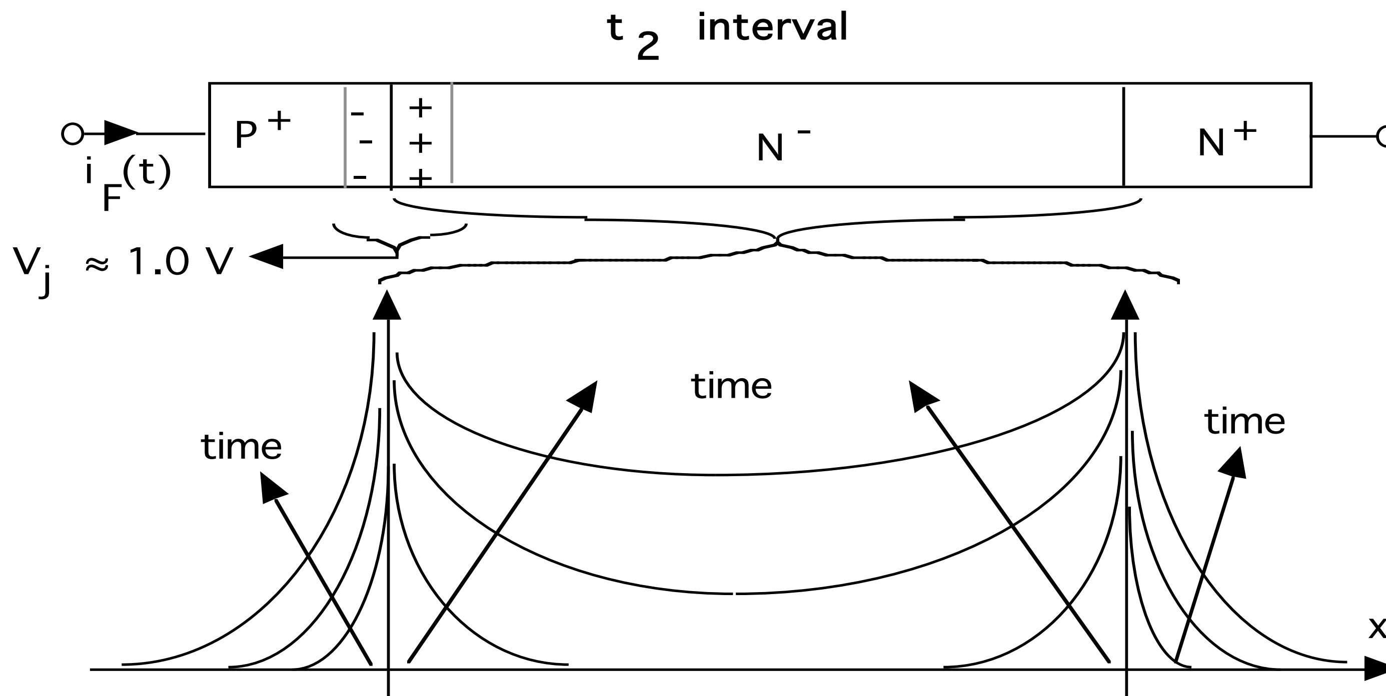


$$C_{sc}(V) = \frac{\varepsilon ! A}{! W(V)}$$

$$R_d = \frac{W_d}{q! \mu_n! N_d! A}$$

$$V_{FP} \approx I_F R_d + L\frac{di_F}{dt}$$

L = stray or wiring inductance



- Injection of excess carriers into drift region greatly reduces R_d.

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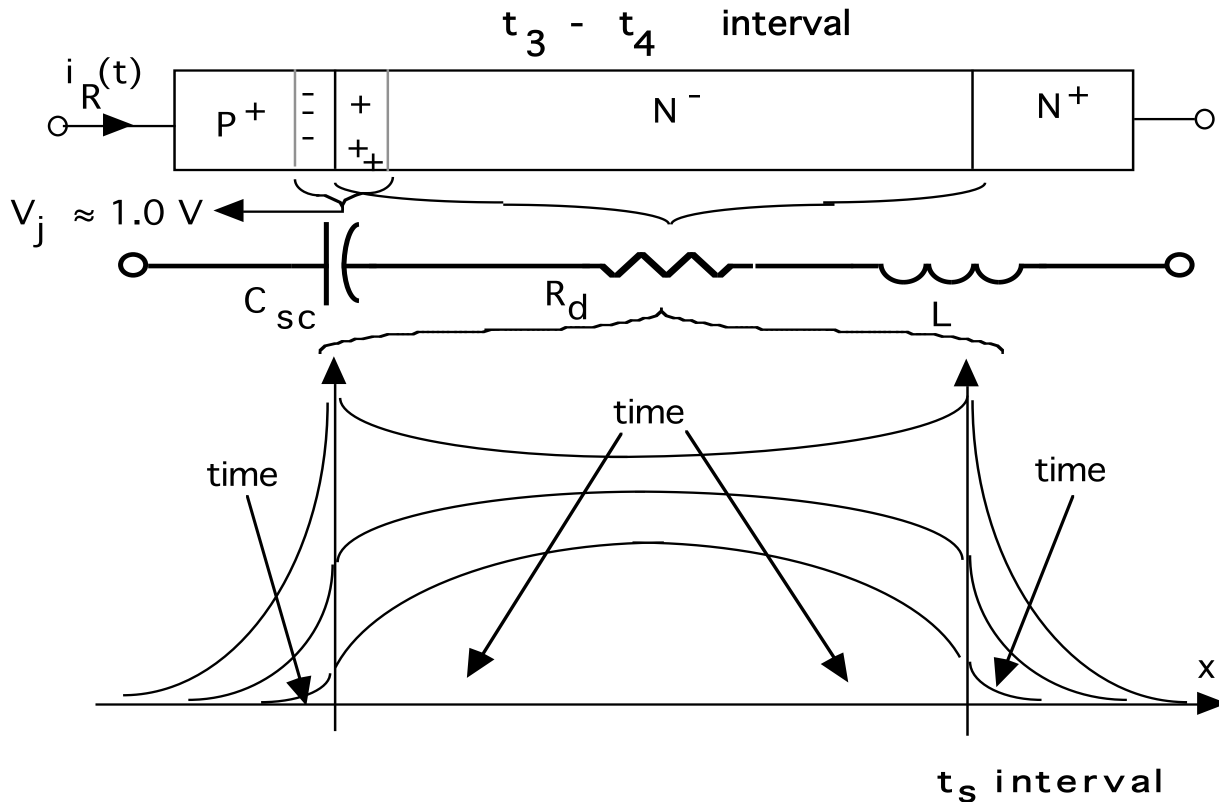
Diode Internal Behavior During Turn-off



- R_d increases as excess carriers are removed via recombination and carrier sweep-out (negative current).

- $V_r = I_{rr}R_d + L\frac{di_R}{dt}$

t_s interval

- Insufficient excess carriers remain to support I_{rr}, so P^+N^- junction becomes reverse-biased and current decreases to zero.

- Voltage drops from V_{rr} to V_R as current decreases to zero. Negative current integrated over its time duration removes a total charge Q_{rr}.

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Factors Effecting Reverse Recovery Time

- $I_{rr} = \frac{di_R}{dt} t_4 = \frac{di_R}{dt} \frac{t_{rr}}{(S!\ +!\ 1)}$; Defined on switching waveform diagram

- $Q_{rr} = \frac{I_{rr!}\ t_{rr}}{2} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(S!\ +!\ 1)}$; Defined on waveform diagram

- Inverting Q_{rr} equation to solve for t_{rr} yields

$$t_{rr} = \sqrt{\frac{2Q_{rr}(S+1)}{\frac{di_R}{dt}}} \text{ and } I_{rr} = \sqrt{\frac{2Q_{rr}\frac{di_R}{dt}}{(S!\ +!\ 1)}}$$

- If stored charge removed mostly by sweep-out $Q_{rr} \approx Q_F \approx I_F\,\tau$

- Using this in eqs. for I_{rr} and t_{rr} and assuming $S + 1 \approx 1$ gives

$$t_{rr} = \sqrt{\frac{2"\ I_F"\ \tau}{\frac{di_R}{dt}}} \text{ and}$$

$$I_{rr} = \sqrt{2"\ I_F"\ \tau"\ \frac{di_R}{dt}}$$

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Carrier Lifetime-Breakdown Voltage Tradeoffs

- Low on-state losses require

$$L = \sqrt{D\,\tau} = \sqrt{\frac{kT}{q\,[\mu_n + \mu_p]}\,\tau}$$

$$L = W_d \geq W(V) = 10^{-5} BV_{BD}$$

- Solving for the lifetime yields

$$\tau = \frac{W_d^2}{(kT/q)\,[\mu_n + \mu_p]} = 4x10^{-12}\,(BV_{BD})^2$$

- Substituting for τ in I_{rr} and t_{rr} equations gives
  - $t_{rr} = 2.8x10^{-6}\,BV_{BD}\sqrt{\frac{I_F}{(di_R/dt)}}$
  - $I_{rr} = 2.8x10^{-6}\,BV_{BD}\sqrt{I_F\,\frac{di_R}{dt}}$

Conclusions

1. Higher breakdown voltages require larger lifetimes if low on-state losses are to be maintained.
2. High breakdown voltage devices slower than low breakdown voltage devices.
3. Turn-off times shortened by large $\frac{di_R}{dt}$ but I_{rr} is increased.

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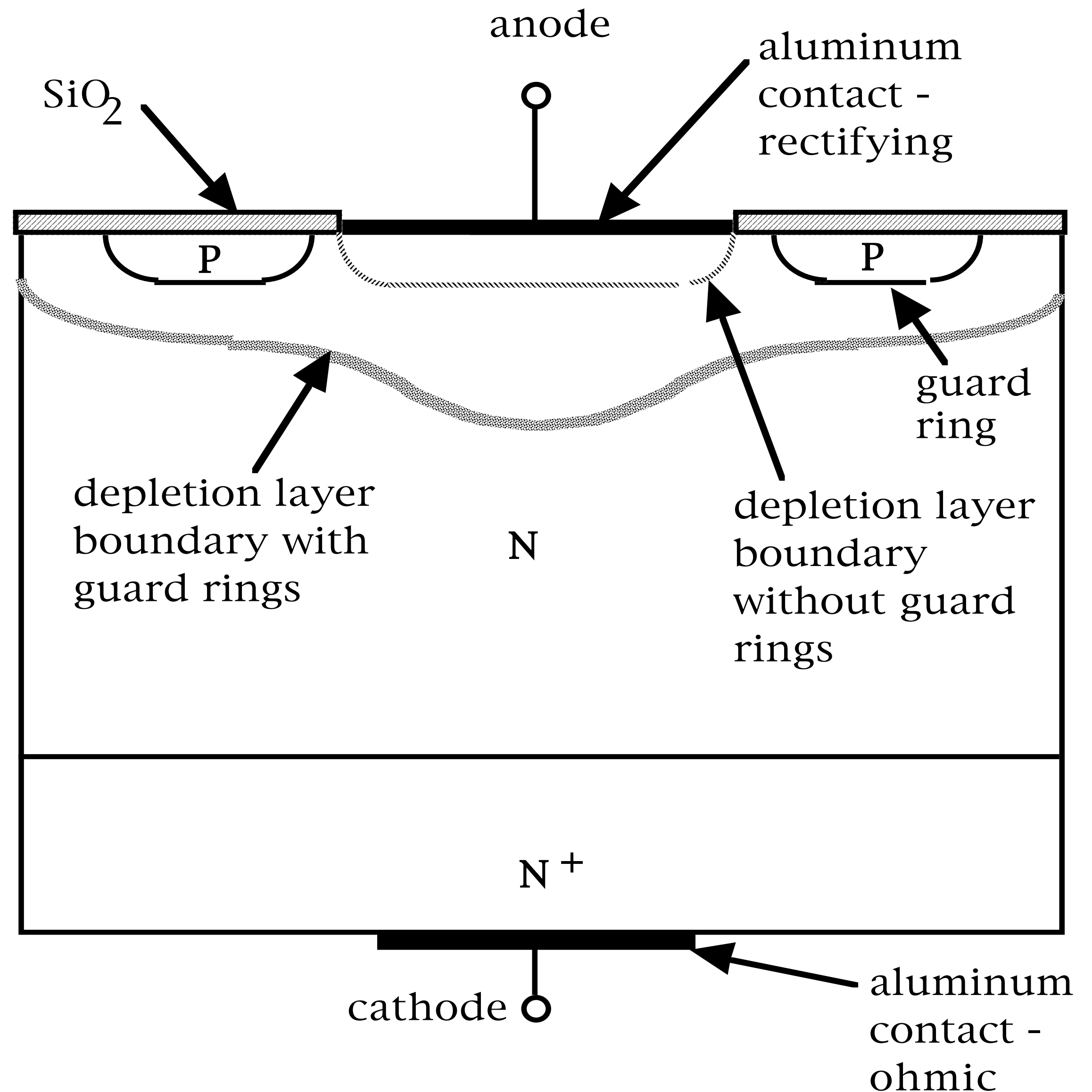
Schottky Diodes



Characteristics

- V(on) = 0.3 - 0.5 volts.
- Breakdown voltages ≤ 100-200 volts.
- Majority carrier device - no stored charge.
- Fast switching because of lack of stored charge.

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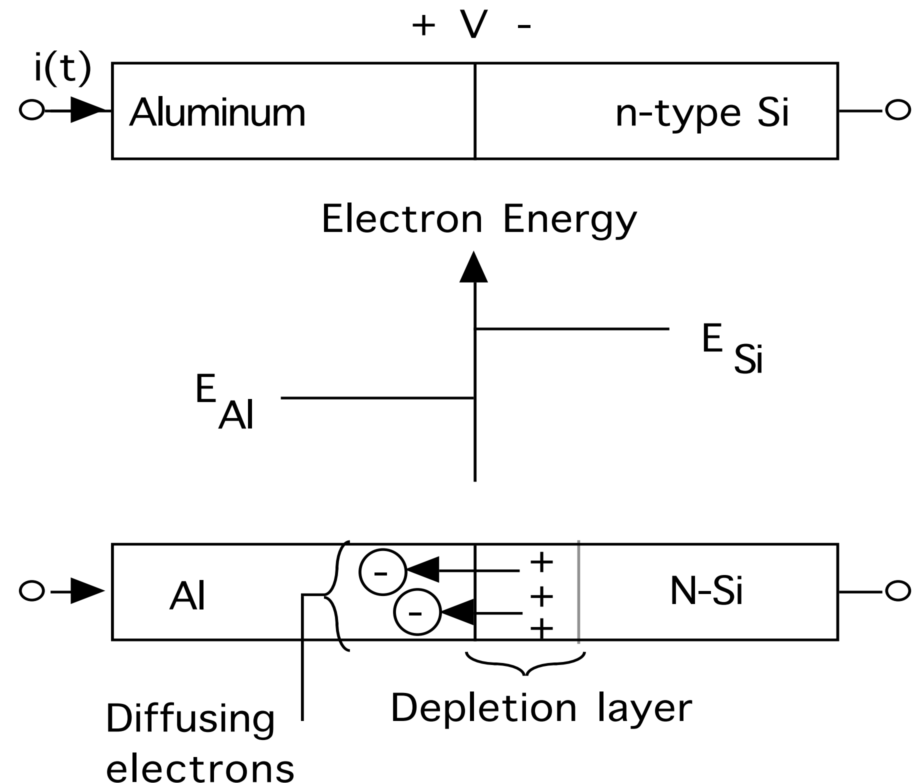
Physics of Schottky Diode Operation

- Electrons diffuse from Si to Al because electrons have larger average energy in silicon compared to aluminum.
- Depletion layer and thus potential barrier set up. Gives rise to rectifying contact.
- No hole injection into silicon. No source of holes in aluminum. Thus diode is a majority carrier device.
- Reverse saturation current much larger than in pn junction diode. This leads to smaller V(on) (0.3 - 0.5 volts)



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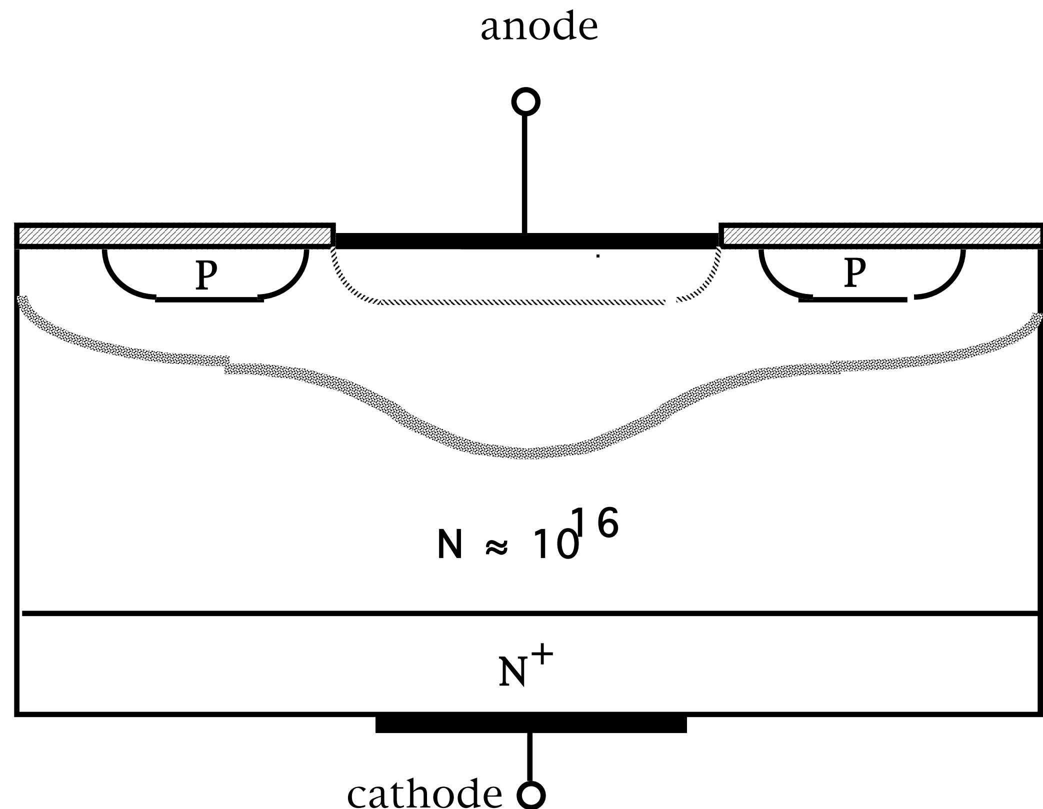
Schottky Diode Breakdown Voltage

- Breakdown voltage limited to 100-200 volts.
- Narrow depletion region widths because of heavier drift region doping needed for low on-state losses.
- Small radius of curvature of depletion region where metallization ends on surface of silicon. Guard rings help to mitigate this problem.
- Depletion layer forms right at silicon surface where maximum field needed for breakdown is less because of imperfections, contaminants.



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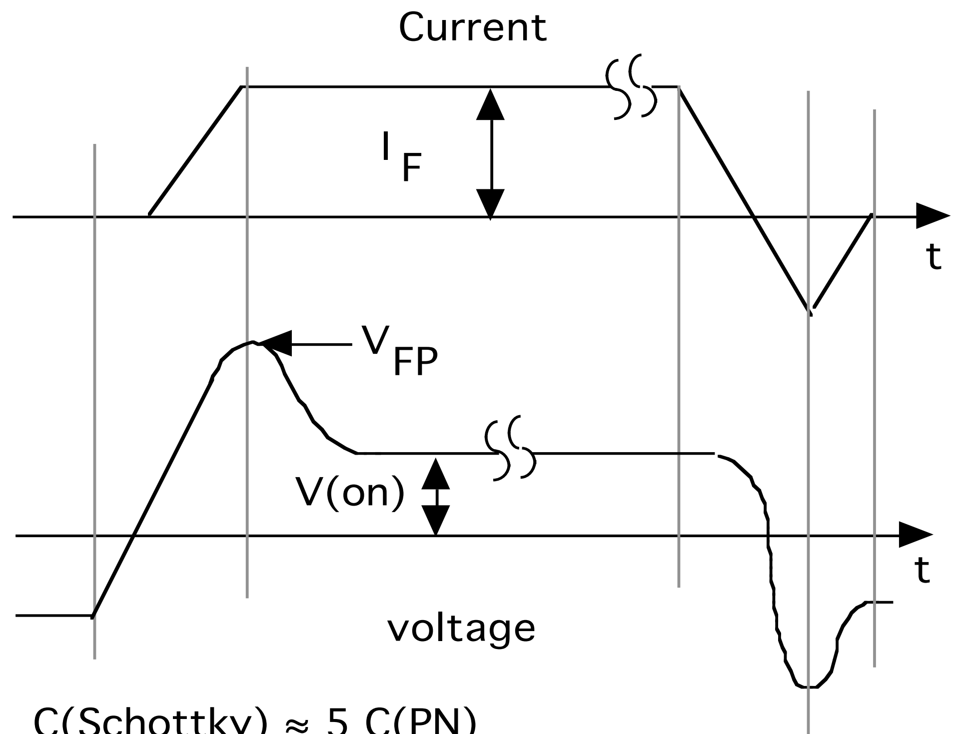
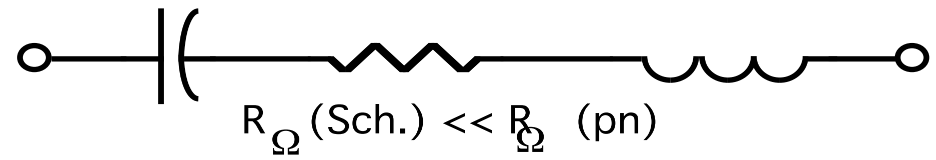
Schottky Diode Switching Waveforms

- Schottky diodes switch much faster than pn junction diodes. No minority carrier storage.
- Foreward voltage overshoot V_{FP} much smaller in Schottky diodes. Drift region ohmic resistance R_{Ω}.
- Reverse recovery time t_{rr} much smaller in Schottky diodes. No minority carrier storage.
- Reverse recovery current I_{rr} comparable to pn junction diodes. space charge capacitance in Schottky diode larger than in pn junction diode becasue of narrower depletion layer widths resulting from heavier dopings.





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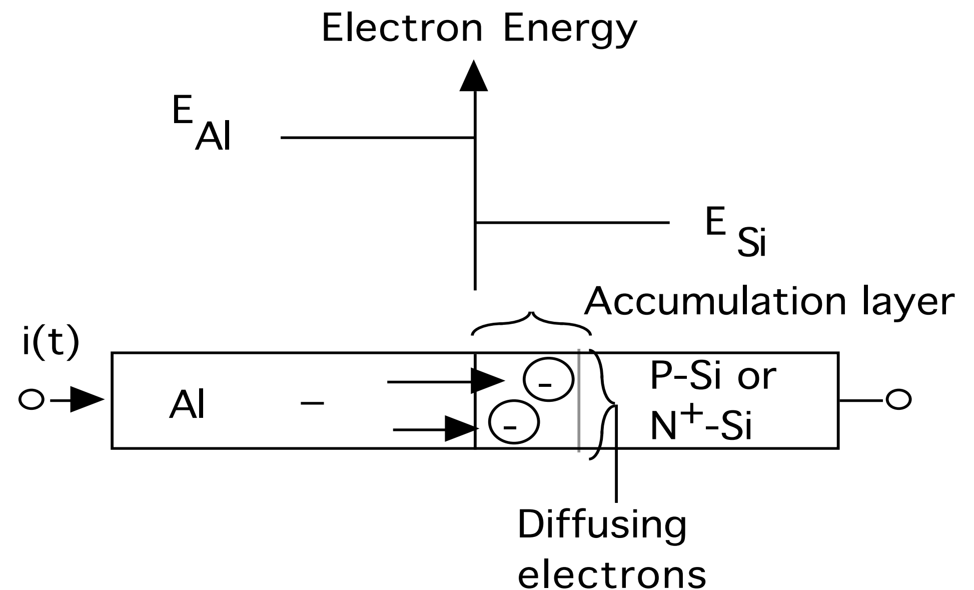
Ohmic Contacts

- Electrons diffuse from Al into p-type Si becasue electrons in Al have higher average energy.

- Electrons in p-type Si form an accumulation layer of greatly enhanced conductivity.

- Contact potential and rectifying junction completely masked by enhanced conductivity. So-called ohmic contact.

- In N^+ Si depletion layer is very narrow and electric fields approach impact ionization values. Small voltages move electrons across barrier easily becasue quantum mechanical tunneling occurs.



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PN Vs Schottkys at Large BV_{BD}

- Minority carrier drift region relationships
  - $I_F \approx \frac{q" [\mu_n" +" \mu_p]" n_a" A" V_d}{W_d}$
- Maximum practical value of $n_a = 10^{17}$ cm^{-3} and corresponding to $\mu_n + \mu_p = 900\ cm^2/(V\text{-sec})$
- Desired breakdown voltage requires $W_d \geq 10^{-5}\ BV_{BD}$

  $\frac{I_F}{A} = 1.4 \times 10^6 \frac{Vd}{BV_{BD}}$
- Majority carrier drift region relationships
  - $I_F \approx \frac{q" [\mu_n" +" \mu_p]" N_d" A" V_d}{W_d}$

- Desired breakdown voltage

  requires $N_d = \frac{1.3 \times 10^{17}}{BV_{BD}}$ and

  $W_d \geq 10^{-5}\ BV_{BD}$
- Large BV_{BD} (1000 V) requires $N_d = 10^{14}\ cm^{-3}$ where $\mu_n + \mu_p = 1500\ cm^2/(V\text{-sec})$
- $\frac{I_F}{A} \approx 3.1 \times 10^6 \frac{V_d}{[BV_{BD}]^2}$
- Conclusion: Minority carrier devices have lower on-state losses at large BV_{BD}.

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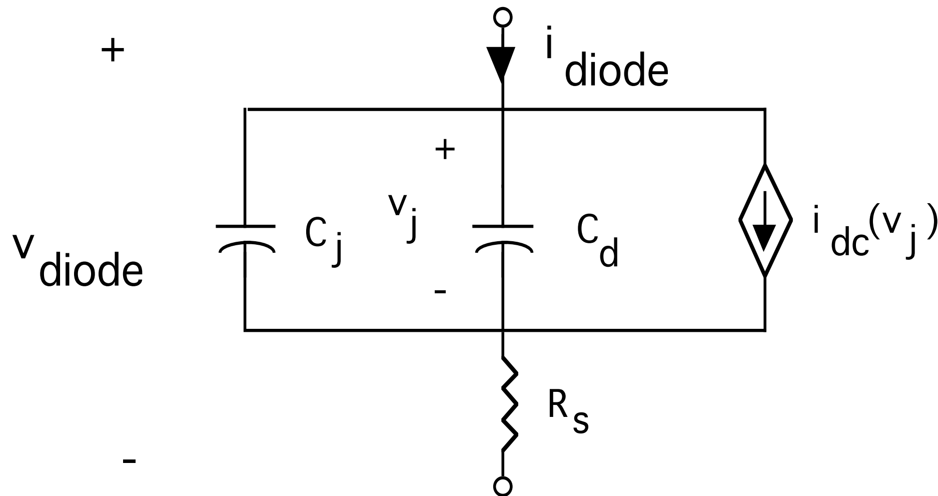
PSPICE Built-in Diode Model

- Circuit diagram



- Components

- C_j - nonlinear space-charge capacitance
- C_d - diffusion capacitance. Caused by excess carriers. Based on quasi-static description of stored charge in drift region of diode.
- Current source $i_{dc}(v_j)$ models the exponential I-V characteristic.
- R_s accounts for parasitic ohmic losses at high currents.

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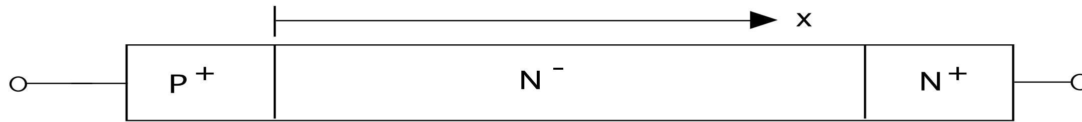
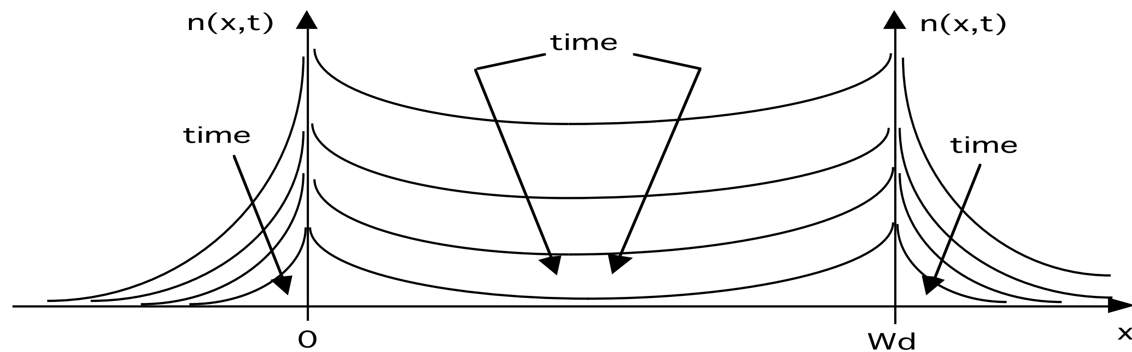
Stored Charge in Diode Drift Region - Actual Versus Quasi-static Approximation

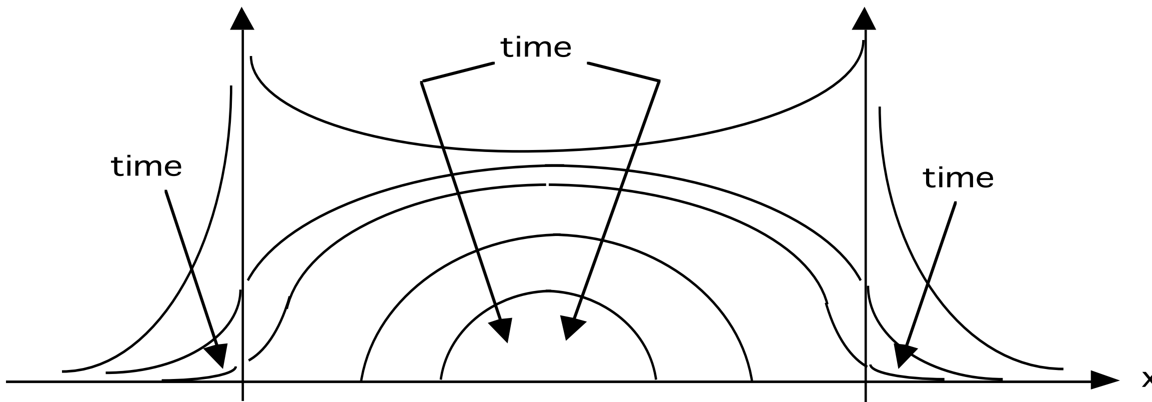


- One dimensional diagram of a power diode.



- Quasistatic view of decay of excess carrier distribution during diode turn-off. n(x,t) = n(x=0,t) f(x)

- Redistribution of excess carriers via diffusion ignored. Equ;ivalent to carriers moving with inifinte velocity.



- Actual behavior of stored charge distribution during turn-off.

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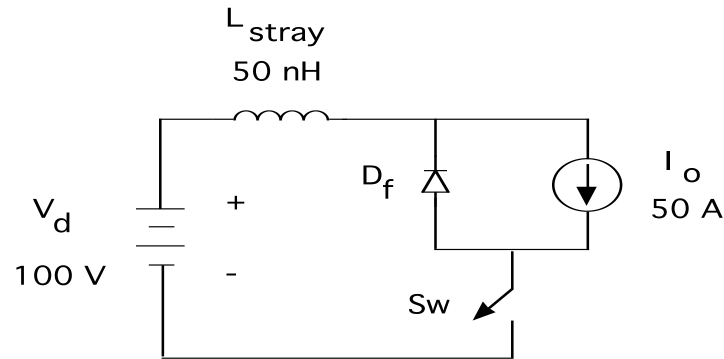
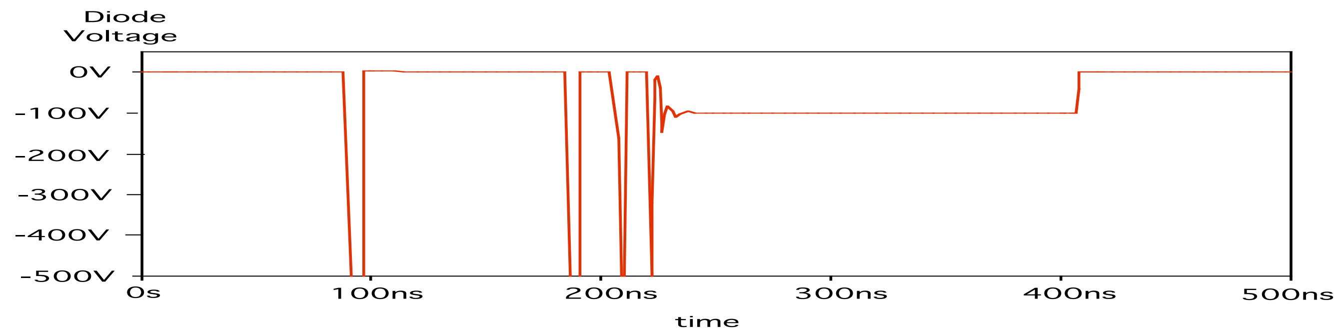
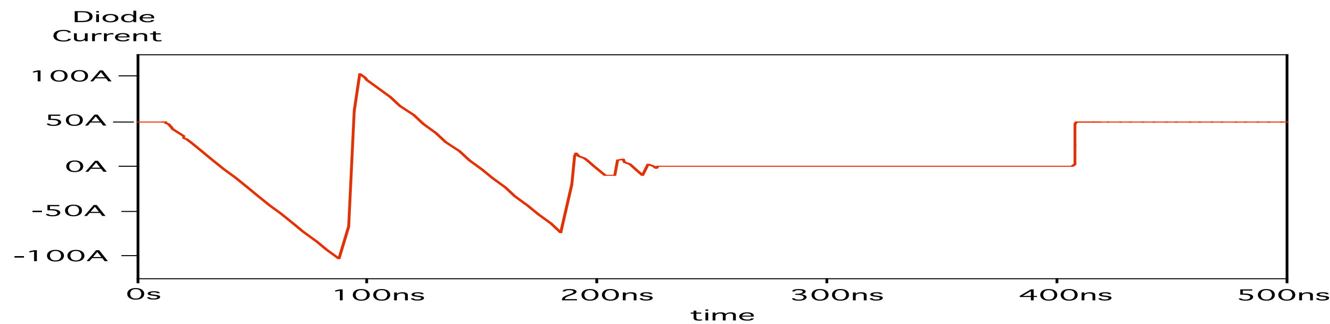
Example of Faulty Simulation Using Built-in Pspice Diode Model



- Test circuit example - step-down converter.
- PSPICE diode model parameters - (TT=100ns Cjo=100pF Rs=.004 Is=20fA)



- Diode voltage transient



- Diode current transient.

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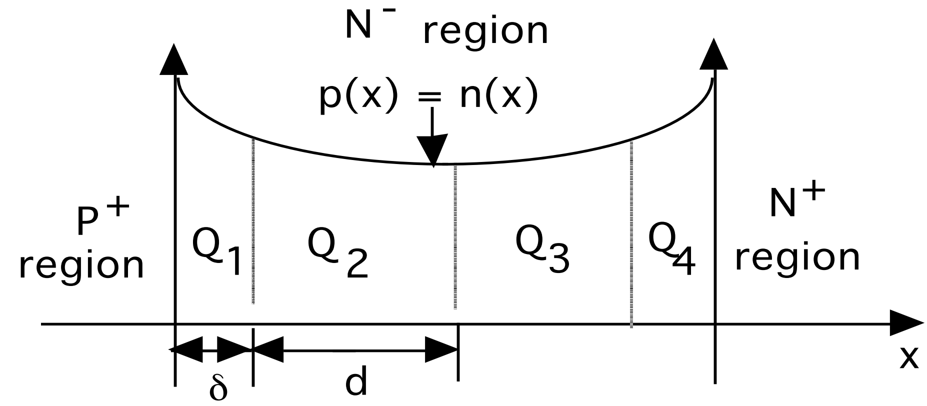
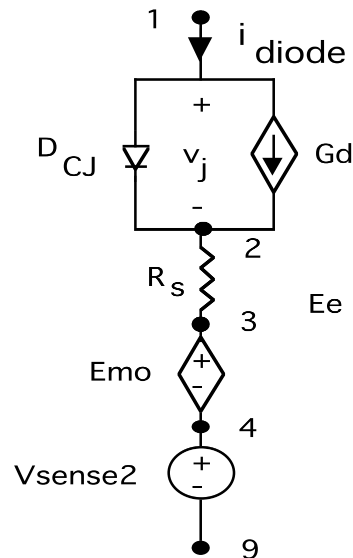
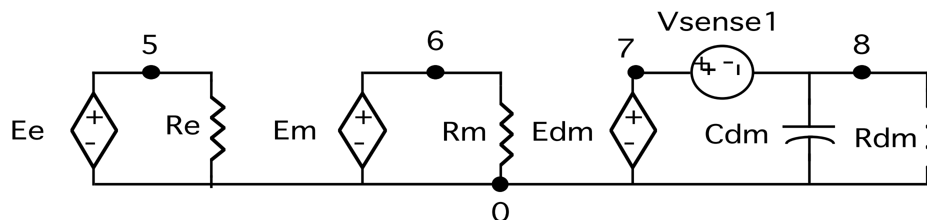
Improved (lumped-charge) Diode Model

- More accurately model distributed nature of excess carrier distribution by dividing it into several regions, each described by a quasi-static function. Termed the lumped-charge approach.





- Circuit diagram of improved diode model. Circuit written in terms of physical equations of the lumped-charge model.



- Detailed equations of model given in subcircuit listing.
- Many other even better (but more complicated models available in technical literature..

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Details of Lumped-Charge Model

Subcircuit Listing

```
.Subckt DMODIFY 1 9 Params: Is1=1e-6, Ise=1e-40, Tau=100ns,
+Tm=100ns,Rmo=Rs=.001, Vta=.0259, CAP=100p, Gde=.5,
+ Fbcoeff=.5, Phi=1, Irbk=1e20,Vrbk=1e20
*Node 1= anodeand  Node 9 = cathode
Dcj 1 2 Dcap ; Included for space charge capacitance and reverse
*breakdown.
.model Dcap D (Is=1e-25 Rs=0 TT=0 Cjo={CAP} M={Gde}
+FC={Fbcoeff} Vj={Phi} +IBV={Irbk} BV=Vrbk})
Gd 1 2 Value={(v(5)-v(6))/Tm +Ise*(exp(v(1,2)/Vta)-1)}
*Following components model forward and reverse recovery.
Ee 5 0 VALUE = {Is1*Tau*(exp(V(1,2)/(2*Vta))-1)}; Ee=Qe
Re 5 0 1e6
Em 6 0 VALUE = {(V(5)/Tm-i(Vsense1))*Tm*Tau/(Tm+Tau)}
*Em=Qm
Rm 6 0 1e6
Edm 7 0 VALUE = {v(6)};Edm=Qm
Vsense1 7 8 dc 0 ; i(vsense1)=dQm/dt
Cdm 8 0 1
Rdm 8 0 1e9
Rs 2 3 4e-3
Emo 3 4 VALUE={2*Vta*Rmo*Tm*i(Vsense2)
+/(v(6)*Rmo+Vta*Tm)}; Vm
Vsense2 4 9 dc 0
.ends
```

- Symbolize subcircuit listing into SCHEMATICS using SYMBOL WIZARD
- Pass numerical values of parameters Tau, Tm, Rmo,Rs, etc. by entering values in PART ATTRIBUTE window (called up within SCHEMATICS).
- See reference shown below for more details and parameter extraction procedures.
- Peter O. Lauritzen and Cliff L. Ma, "A Simple Diode Model with Forward and Reverse Recovery", IEEE Trans. on Power Electronics, Vol. 8, No. 4, pp. 342-346, (Oct., 1993)

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Simulation Results Using Lumped-Charge Diode Model

Diode voltage and current waveforms

Diode Voltage

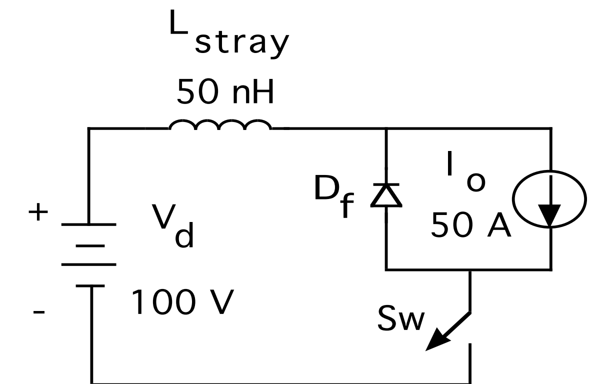
10V
0V
-10V
410ns 415ns 420ns

0V
-100V
-200V
0s 100ns 200ns 300ns 400ns 500ns
time

Diode Current

50A
0A
-50A
0s 100ns 200ns 300ns 400ns 500ns
time

Simulation Circuit



- Note soft reverse recovery and forward voltage overshoot. Qualitatively matches experimental measurements.

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Lecture Notes

Bipolar Junction Transistors (BJTs)

Outline

- BJT structure and I-V characteristics
- Physical operation of power BJTs
- Switching characteristics
- Breakdown voltage
- Second breakdown
- On-state voltage
- Safe operating areas

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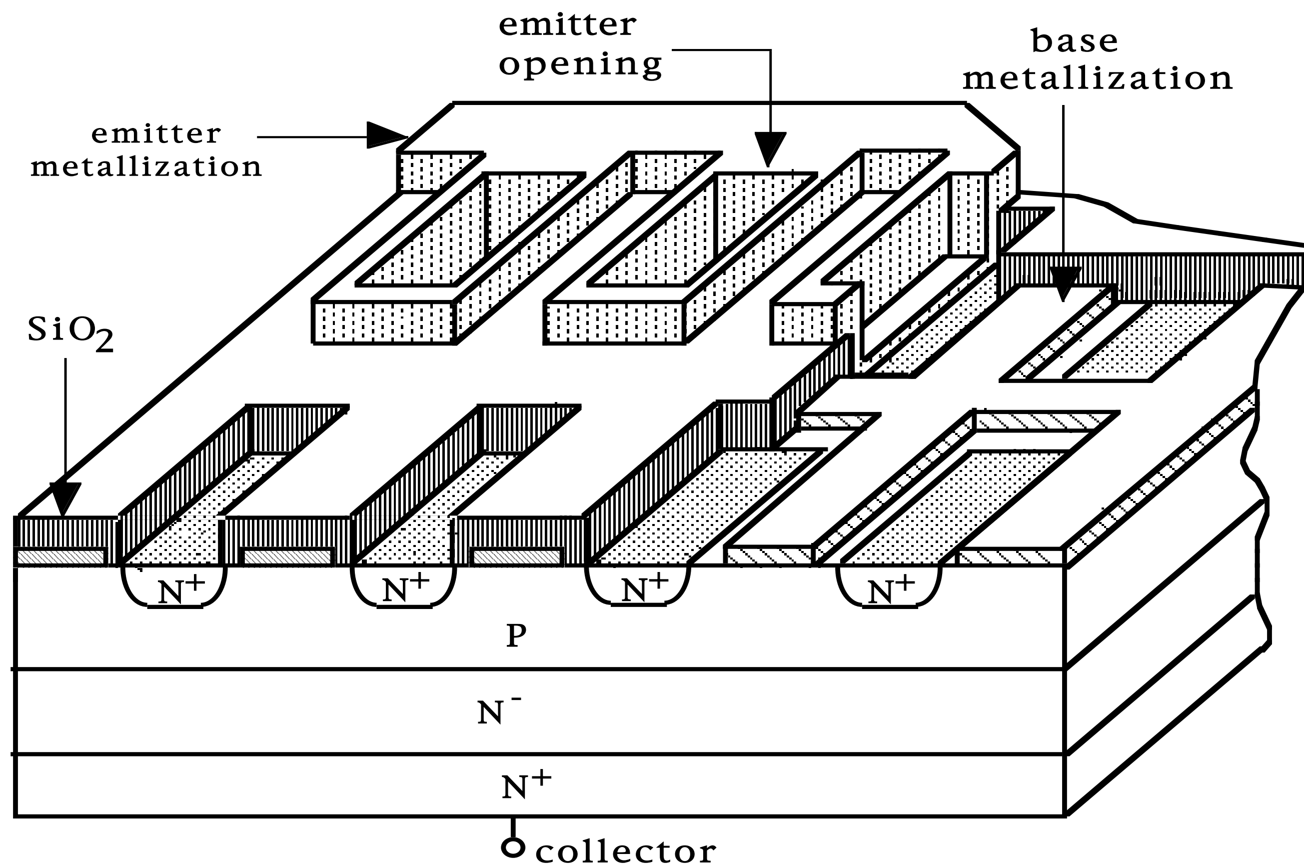
Basic Geometry of Power BJTs



Features to Note

- Multiple narrow emitters - minimize emitter current crowding.
- Multiple parallel base conductors - minimize parasitic resistance in series with the base.

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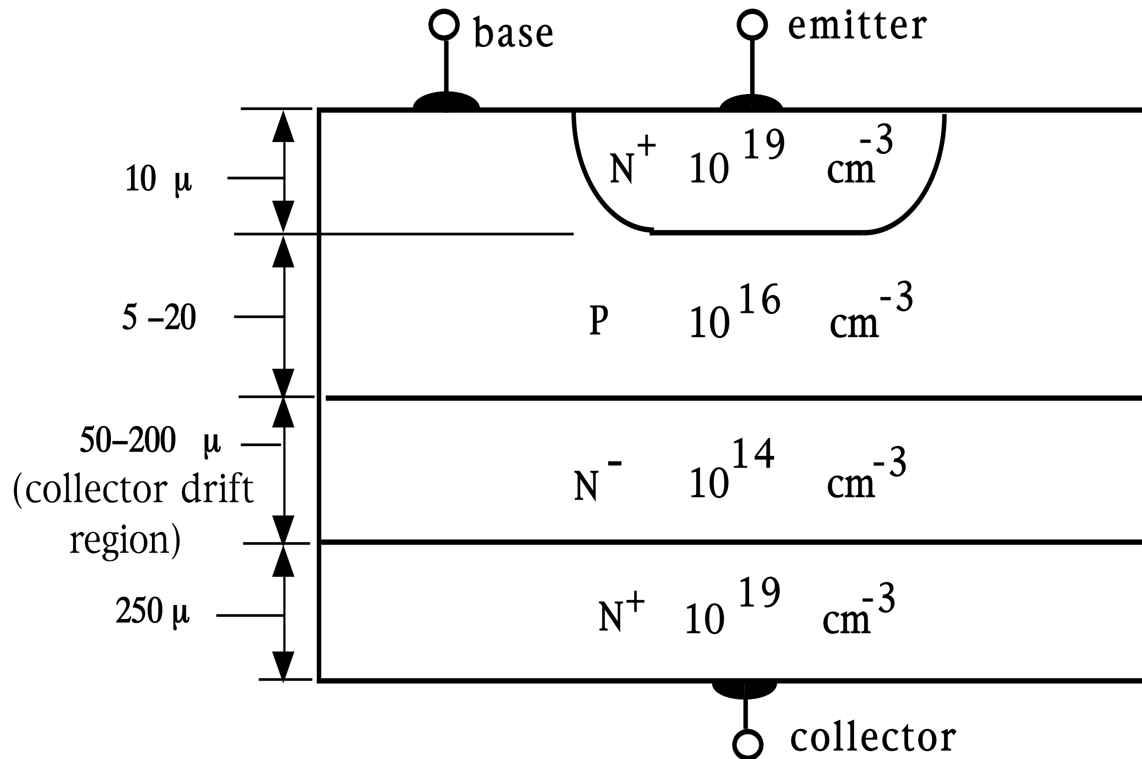
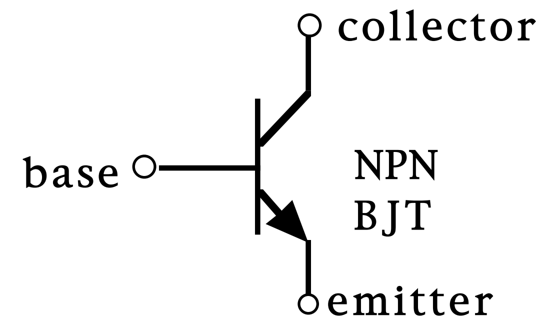
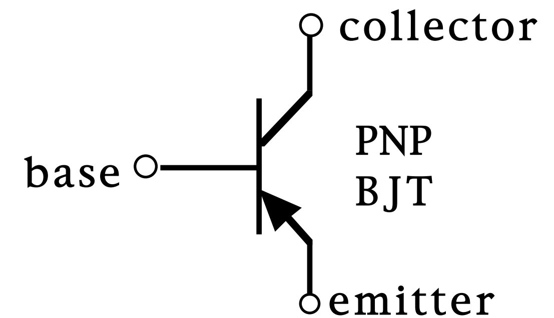
BJT Construction Parameters







Features to Note

- Wide base width - low (<10) beta.
- Lightly doped collector drift region - large breakdown voltage.

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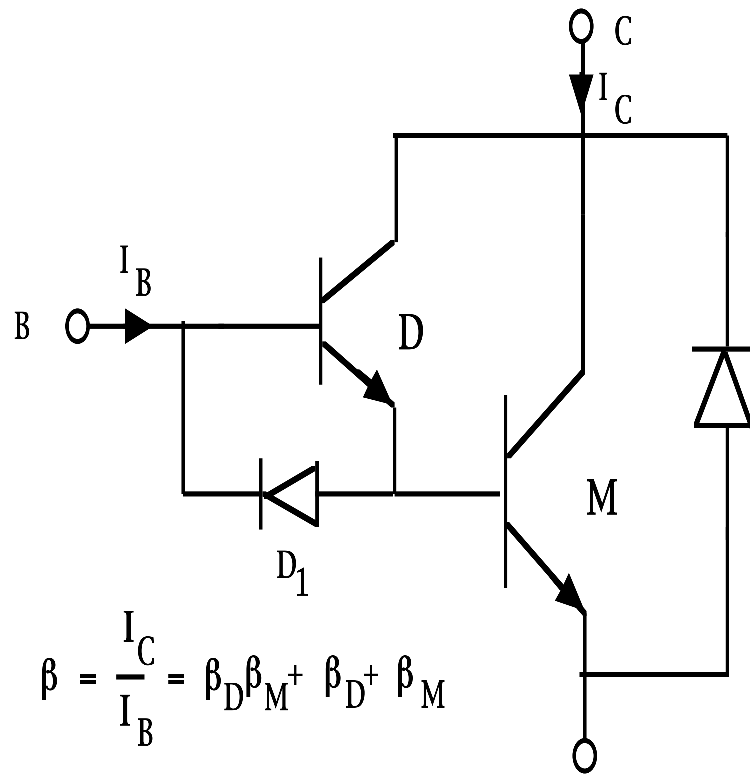
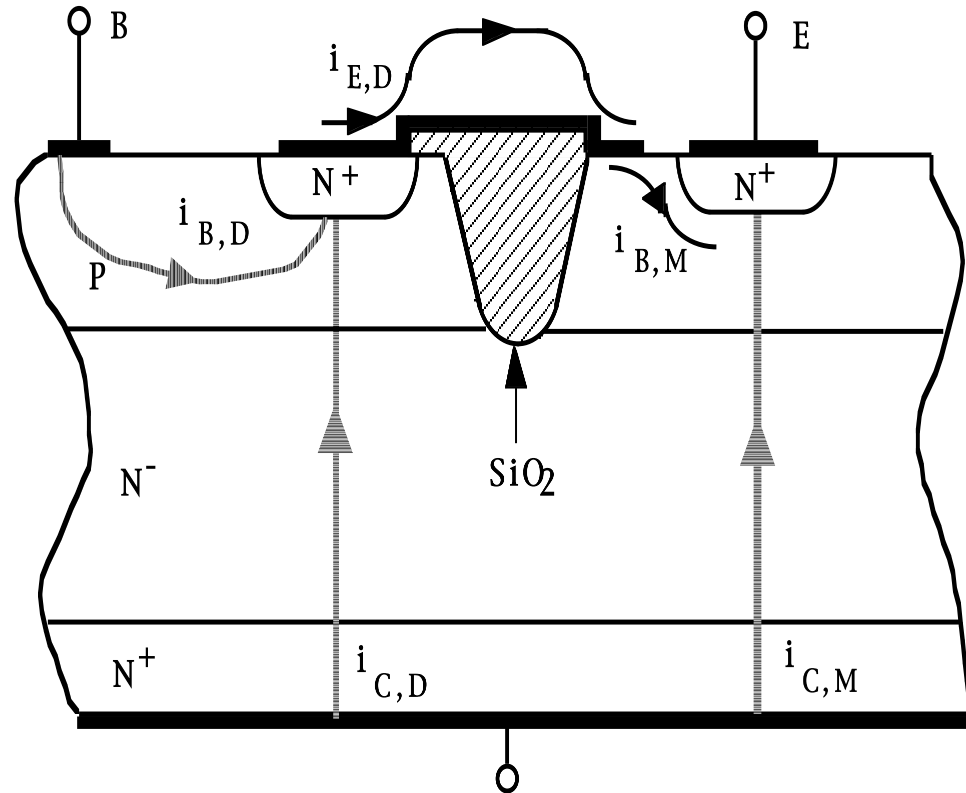
Darlington-connected BJTs





- Composite device has respectable beta.

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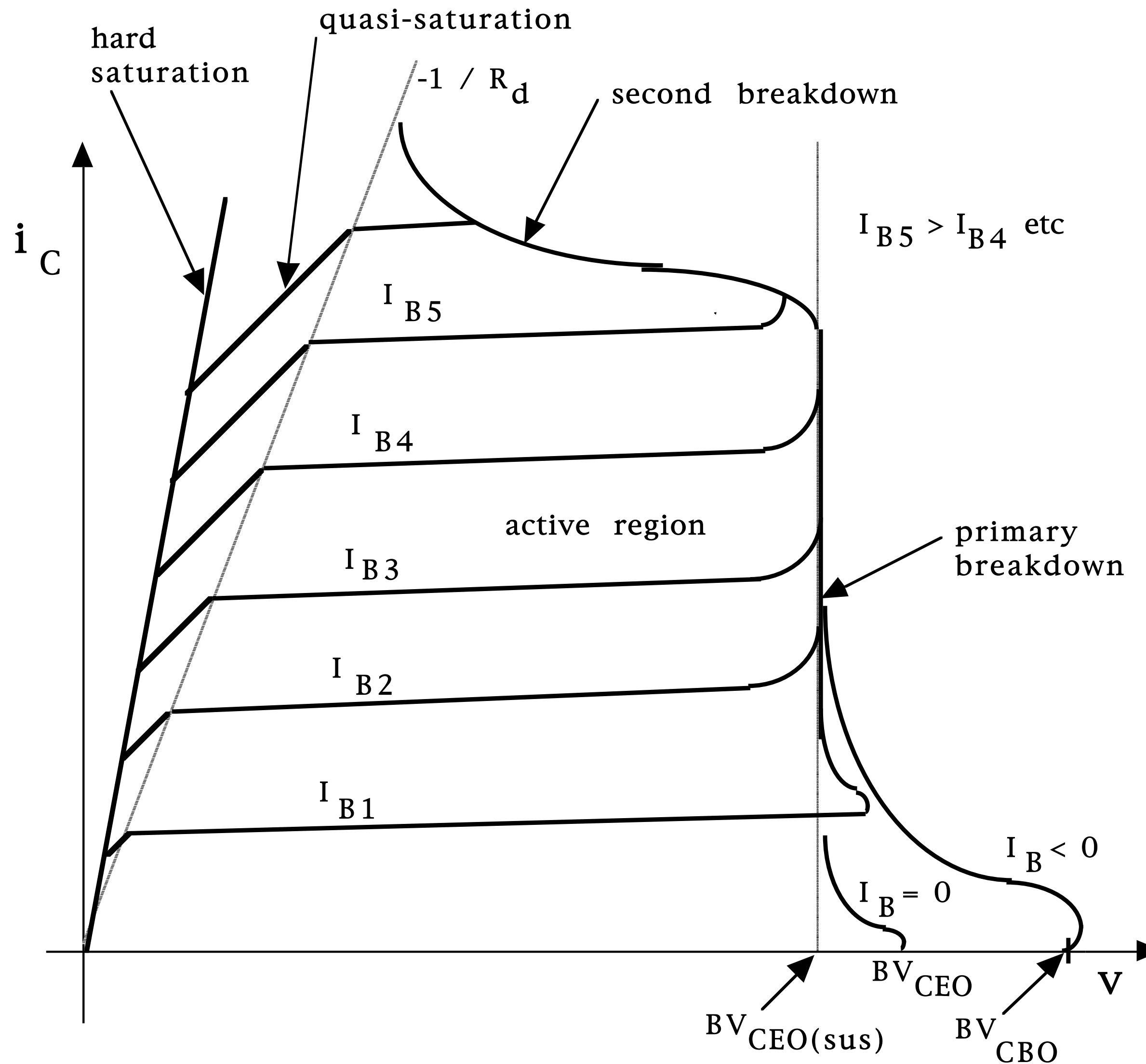
Power BJT I-V Characteristic



Features to Note

- 2nd breakdown - must be avoided.
- Quasi-saturation - unique to power BJTs
- $BV_{CBO} > BV_{CEO}$ - extended blocking voltage range.

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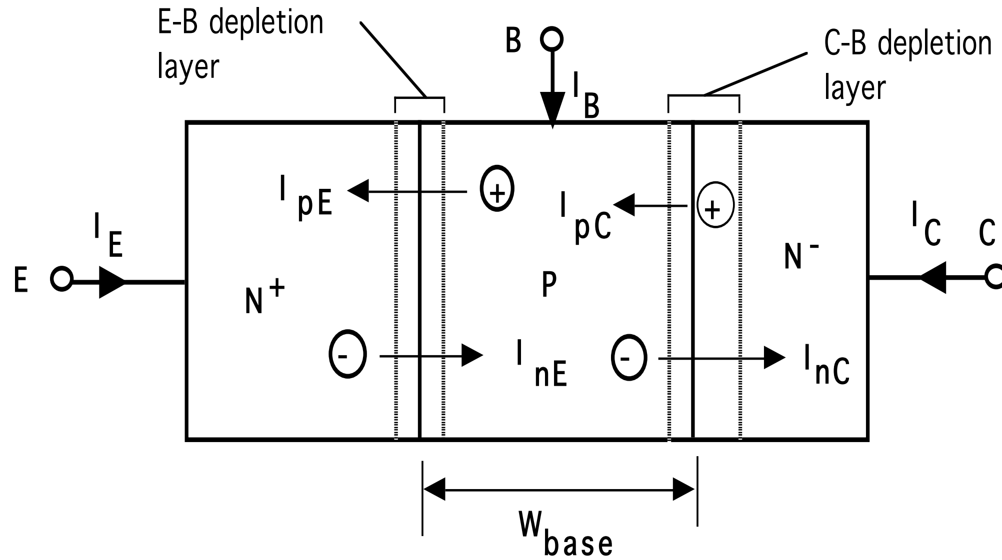
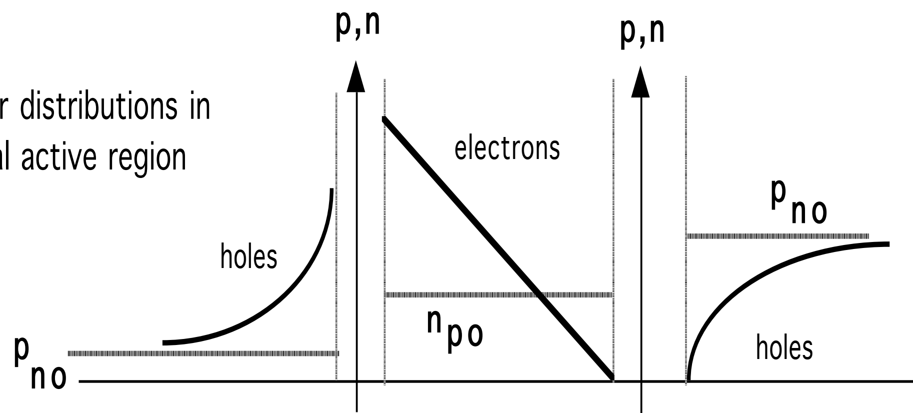
BJT Internal Current Components





- I_{ne} and I_{pe} flow via diffusion. I_{nc} and I_{pc} flow via drift.
- $I_{ne} >> I_{pe}$ because of heavy emitter doping.
- $I_{ne} \approx I_{nc}$ because $L_{nb} = \{D_{nb}\ \tau_{nb}\}^{1/2} << W_{base}$ and collector area much larger than emitter area.
- I_{pc} << other current components because very few holes in b-c space charge region.

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Power BJT Current Gain β

- $I_C \approx I_{nc}$ since I_{pc} very small : $I_B = - I_C - I_B = - I_{nc} + I_{ne} + I_{pe}$
- $I_B / I_C = 1/\beta = (I_{ne} - I_{nc})/I_{nc} + I_{pe}/I_{nc}$
- $(I_{ne} - I_{nc})/I_{nc}$ represents fraction of electrons injected into base that recombine in the base. Minimize by having large values of τ_{nb} (for long diffusion lengths) and short base widths W_{base}
- I_{pe} proportional to $p_{no} = (n_i)^2/N_{de}$; Minimize via large N_{de}
- Short base width conflicts with need for larger base width needed in HV BJTs to accomodate CB depletion region.
- Long base lifetime conflicts with need for short lifetime for faster switching speeds
- Trade-offs (compromises) in these factors limit betas in power BJTs to range of 5 to 20

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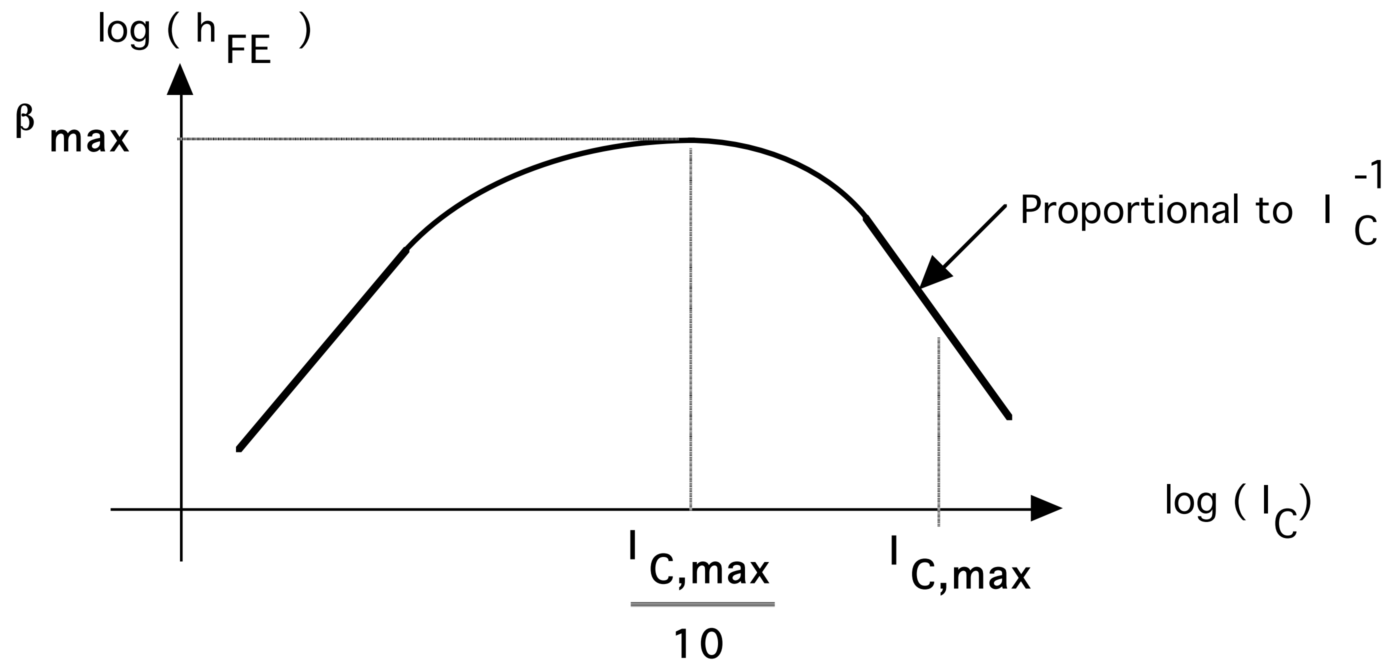
Beta versus Collect Current



- Beta decrease at large collector current due to high level injection effects (conductivity modulation where $\delta n = \delta p$) in base.

- When $\delta n = \delta p$, base current must increase faster than collector current to provide extra holes. This constitutes a reduction in beta.

- High level injection conditions aided by emitter current crowding.

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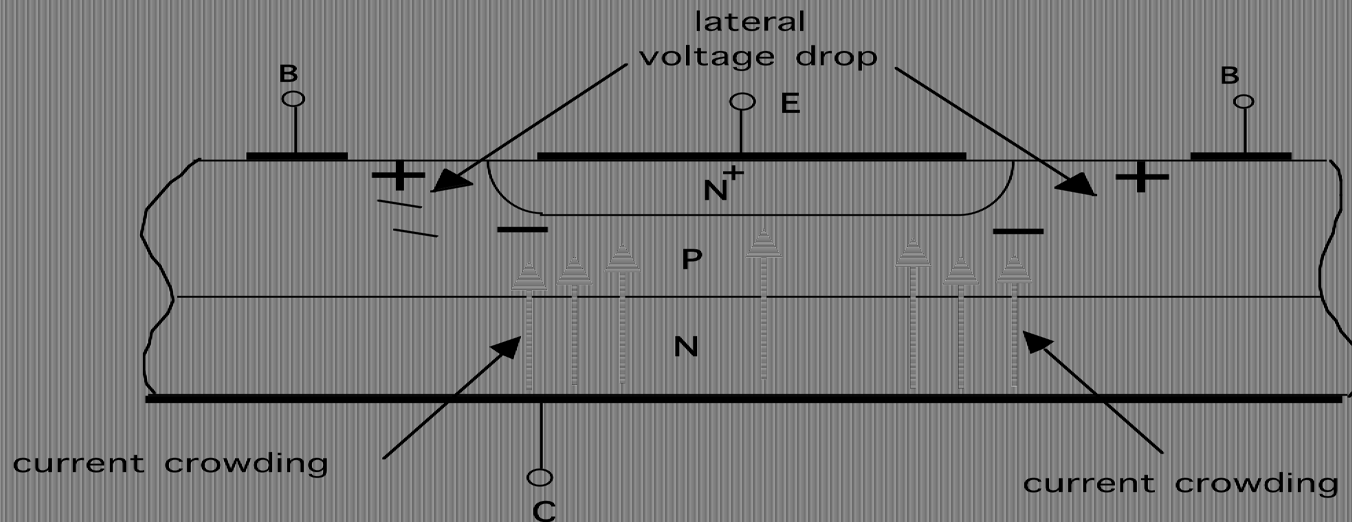
Emitter Current Crowding



- I_B proportional to $\exp\{qV_{BE}/(kT)\}$
- Later voltage drops make V_{BE} larger at edge of emitters.
- Base/emitter current and thus carrier densities larger at edge of emitters. So-called emitter current crowding.
- This emitter current crowding leads to high level injection at relatively modest values of current.
- Reduce effect of current crowding by breaking emitters into many narrow regions connected electrically in parallel.

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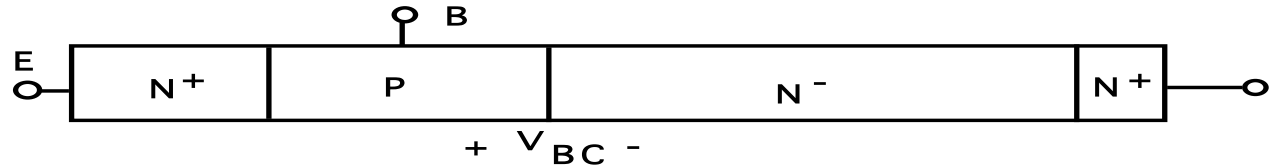
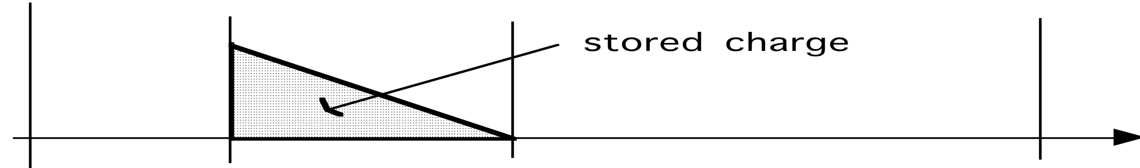
Quasi-saturation in Power BJTs

Power BJT



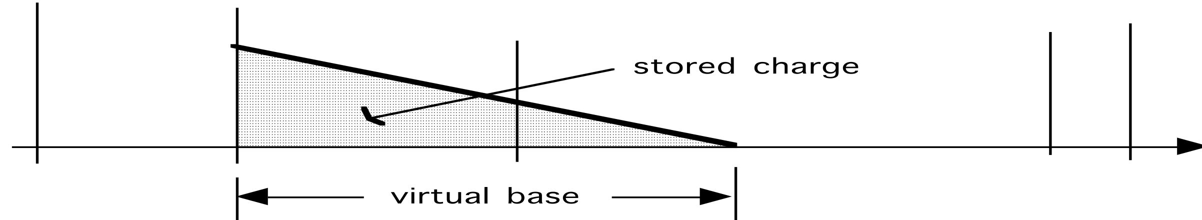
Active region

$V_{BC} < 0$



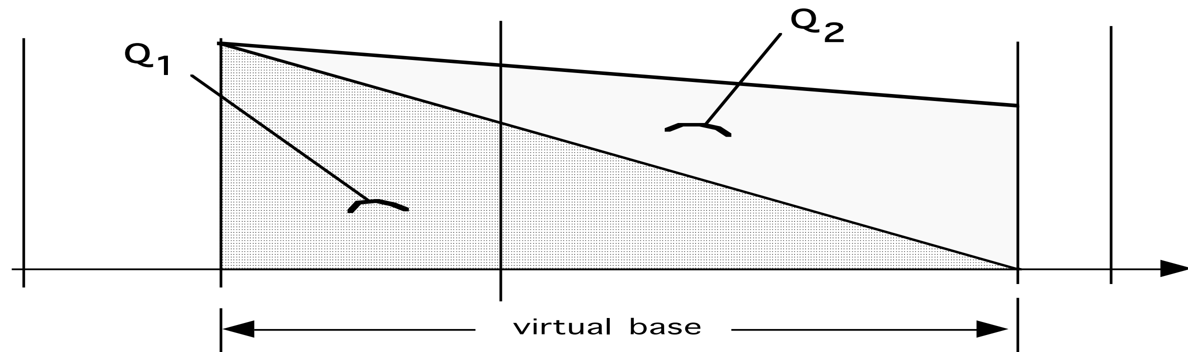
Quasi-saturation

$V_{BC} > 0$ but drift region not completely filled with excess carriers.



Hard saturation

$V_{BC} > 0$ and drift region filled with excess carriers.



- Beta decreases in quasi-saturation because effective base width (virtual base) width has increased.

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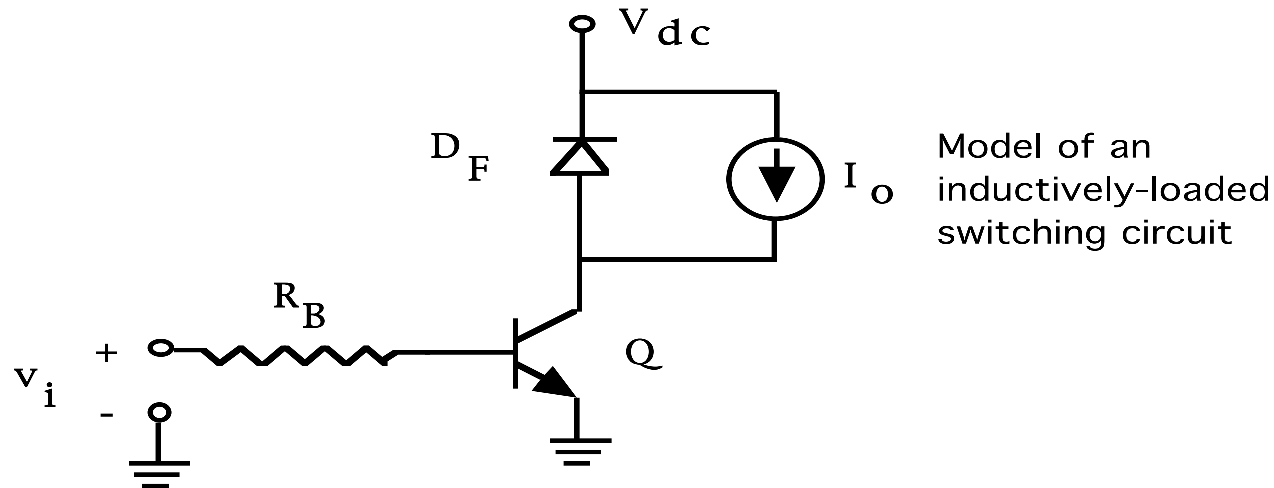
Generic BJT Application - Clamped Inductive Load



- Current source I_o models an inductive load with an L/R time constant >> than switching period.
- Positive base current turns BJT on (hard saturation). So-called forward bias operation.
- Negative base current/base-emitter voltage turns BJT off. So-called reverse bais operation.
- Free wheeling diode DF prevents large inductive overvoltage from developing across BJT collector-emitter terminals.

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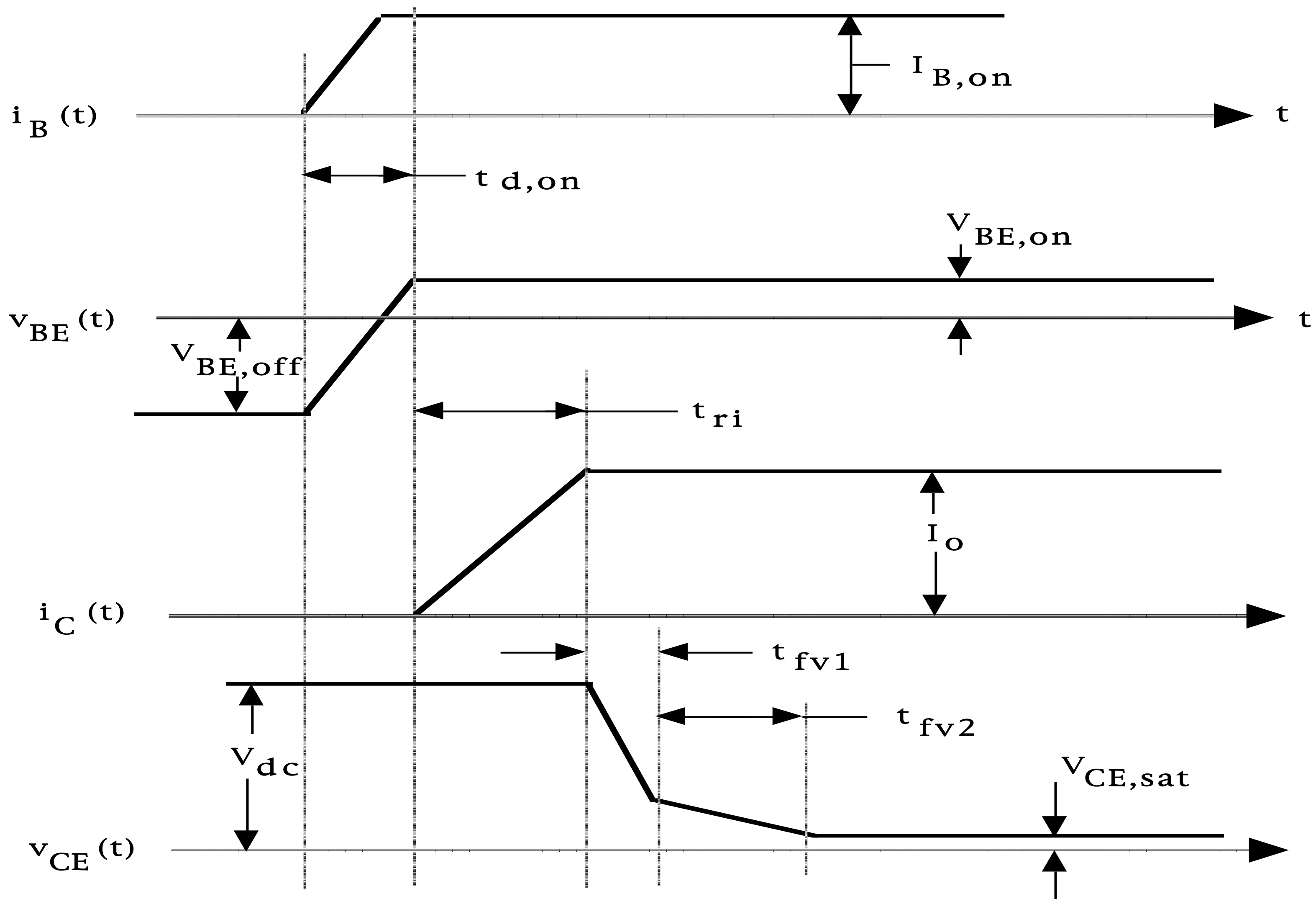
Power BJT Turn-on Waveforms



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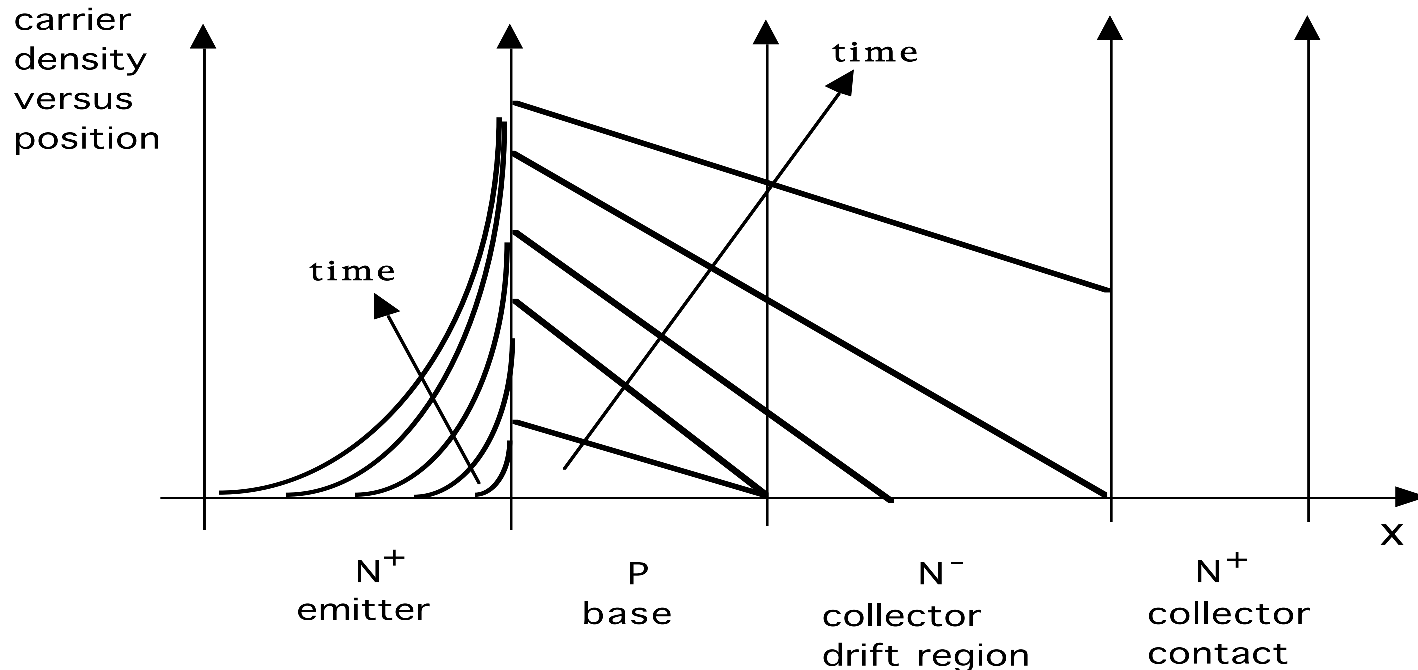
Excess Carrier Growth During BJT Turn-on



- Growth of excess carrier distributions begins after $t_{d(on)}$ when B-E junction becomes forward biased.
- Entrance into quasi-saturation discernable from voltage or current waveform at start of time t_{vf2}.
- Collector current "tailing" due to reduced beta in quasi-saturation as BJT turns off.
- Hard saturation entered as excess carrier distribution has swept across dirft region.

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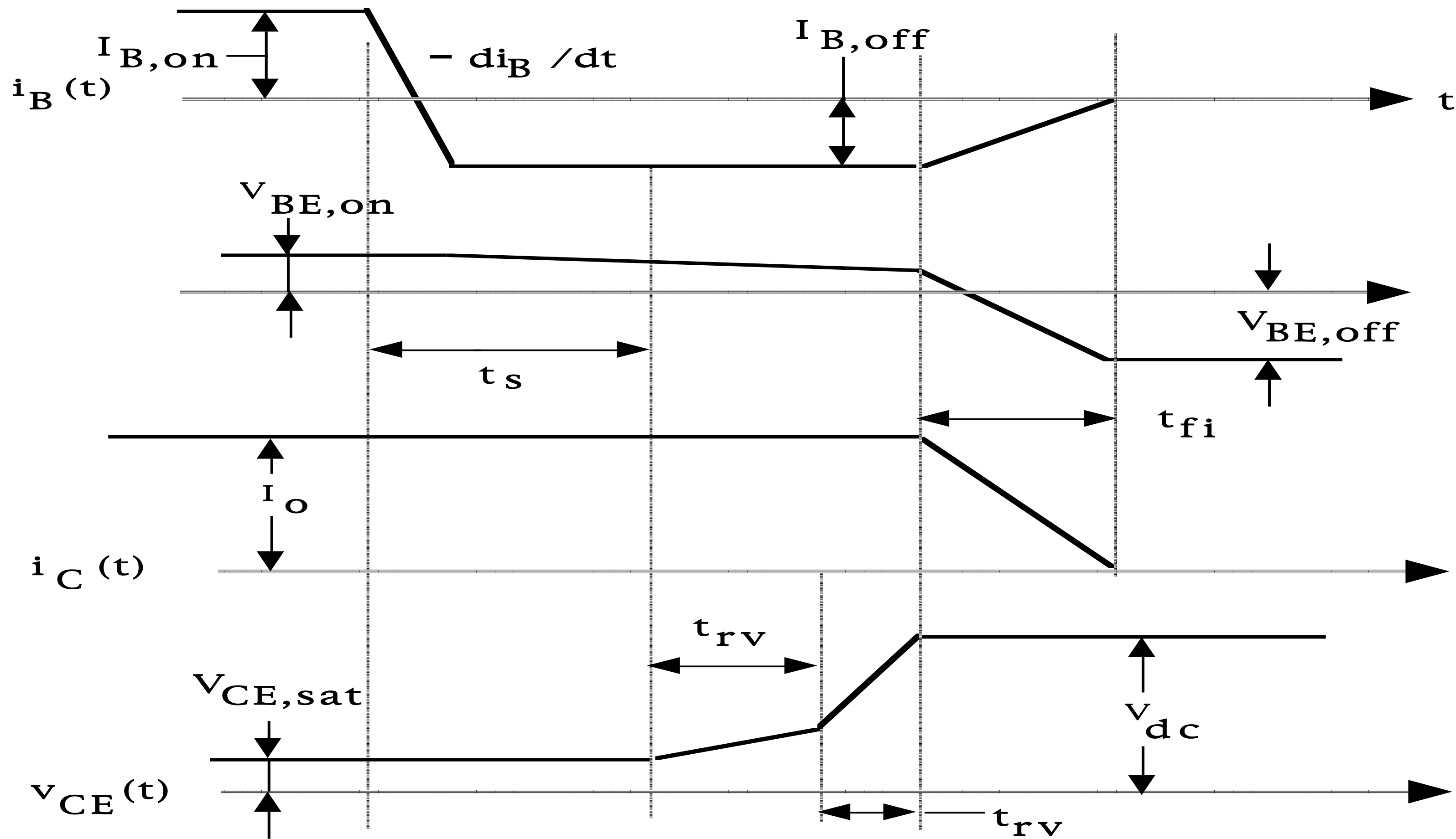
Turn-off Waveforms with Controlled Base Current



- Base current must make a controlled transition (controlled value of $-di_B/dt$) from positive to negative values in order to minimize turn-off times and switching losses.

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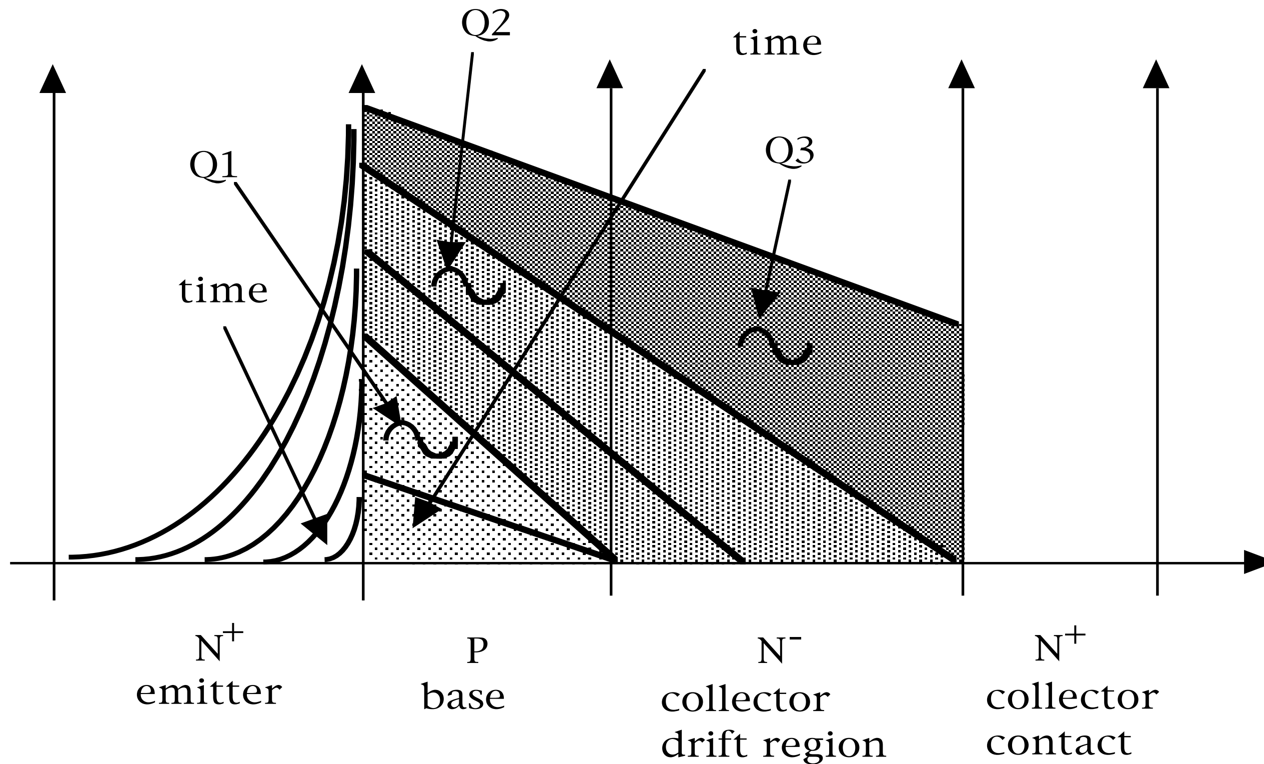
Controlled Turn-off Excess Carrier Removal



- t_s = storage time = time required to remove excess charge Q3.
- t_{rv1} = time to remove charge Q2 holding transistor in quasi-saturation.
- t_{rv2} = time required for VCE to complete its growth to Vdc with BJT in active region.
- t_{fi} = time required to remove remaining stored charge Q1 in base and each edge of cut-off.

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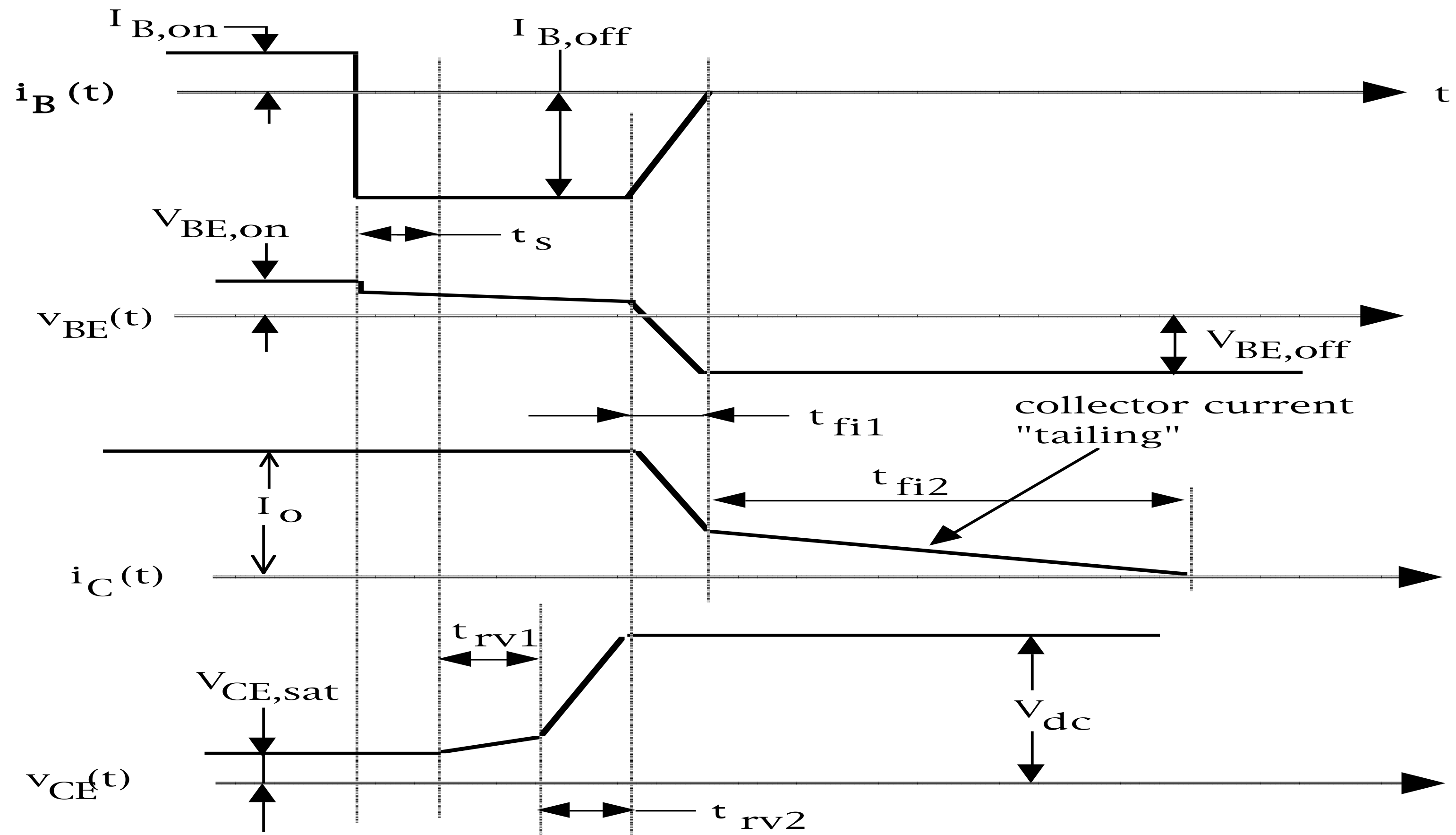
Turn-off Waveforms with Uncontrolled Base Current



- Excessive switching losses with collector current tailing.

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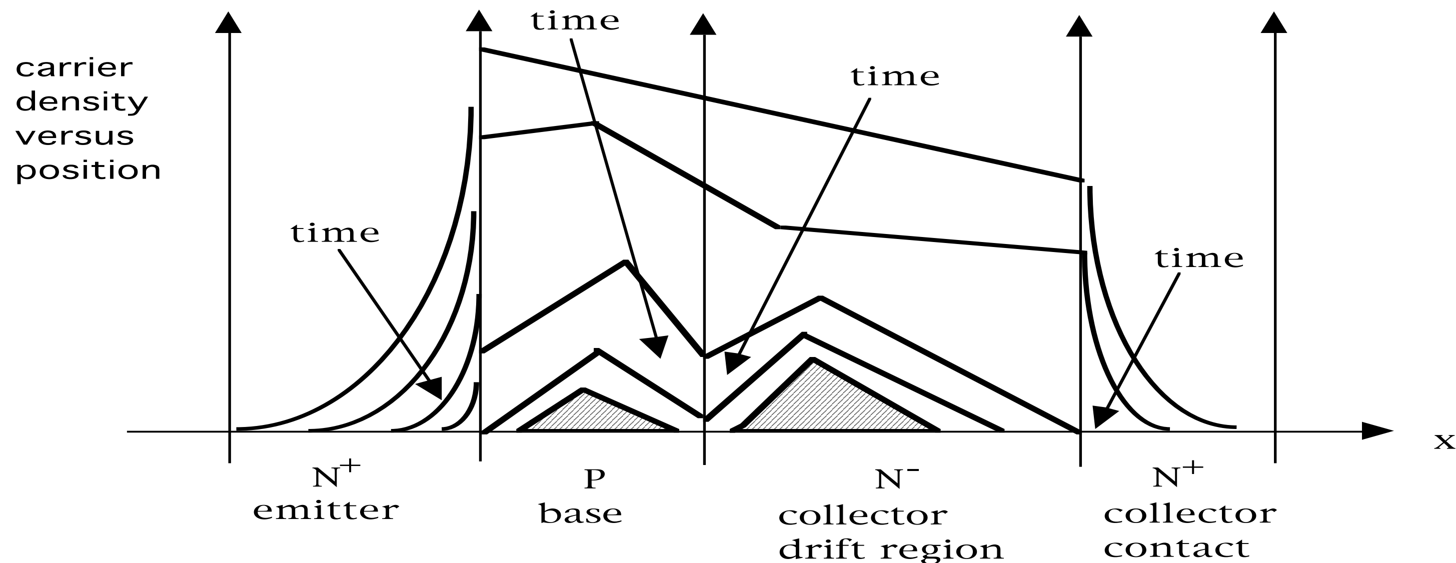
Uncontrolled Turn-off Excess Carrier Removal



- Uncontrolled base current removes stored charge in base faster than in collector drift region.
- Base-emitter junction reverse biased before collector-base junction.
- Stored charge remaining in drift region now can be only removed by the negative base current rather than the much larger collector current which was flowing before the B-E junction was reverse biased.
- Takes longer time to finish removal of drift region stored charge thus leading to collector current "tailing" and excessive switching losses.

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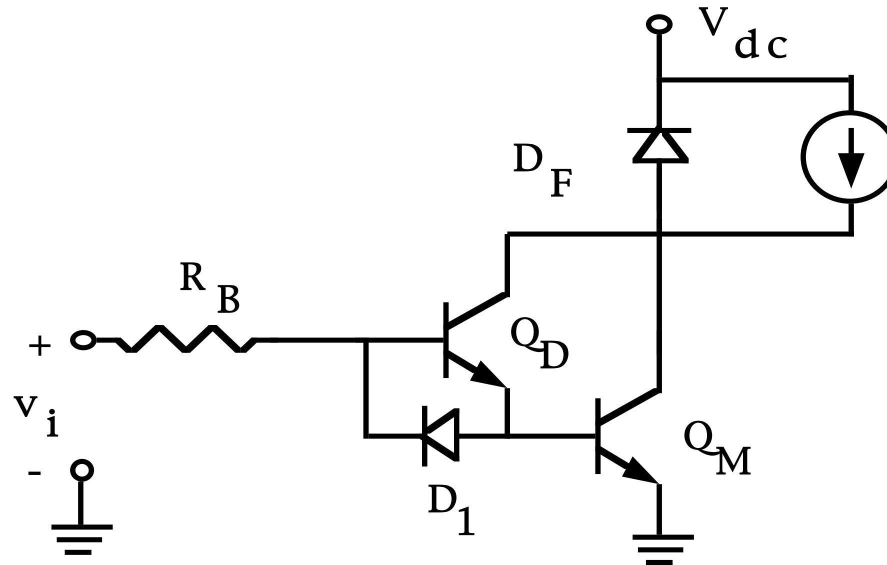
Darlington Switching Behavior



- Turn-on waveforms for Darlington very similar to single BJT circuit.
- Turn-on times somewhat shorter in Darlington circuit because of large base drive for main BJT.
- Turn-off waveforms significantly different for Darlington.
- Diode D_1 essential for fast turn-off of Darlington. With it, Q_M would be isolated without any negative base current once Q_D was off.
- Open base turn-off of a BJT relies on internal recombination to remove excess carriers and takes much longe than if carriers are removed by carrier sweepout via a large collector current.

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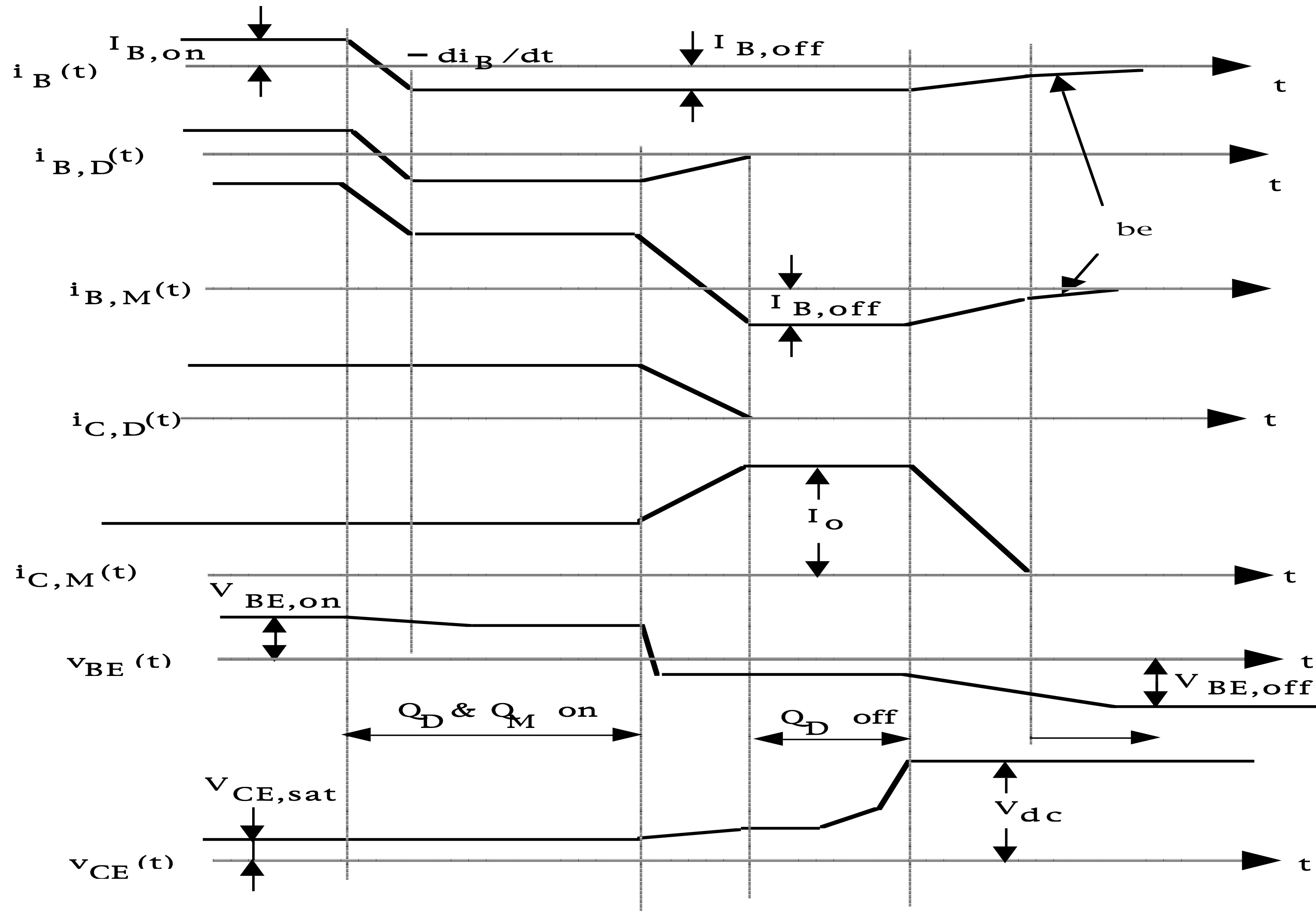
Darlington Turn-off Waveforms



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Power BJT Breakdown Voltage

- Blocking voltage capability of BJT limited by breakdown of CB junction.
  - BV_{CBO} = CB junction breakdown with emitter open.
  - BV_{CEO} = CB junction breakdown with base open.
  - $BV_{CEO} = BV_{CBO}/(\beta)^{1/n}$; n = 4 for npn BJTs and n = 6 for PNP BJTs
- BE junction forward biased even when base current = 0 by reverse current from CB junction.
- Excess carriers injected into base from emitter and increase saturation current of CB junction.
- Extra carriers at CB junction increase likelyhood of impact ionization at lower voltages , thus decreasing breakdown voltage.
- Wide base width to lower beta and increase BV_{CEO} .
- Typical base widths in high voltage (1000V) BJTs = 5 to 10 and BV_{CEO} = 0.5 BV_{CBO} .

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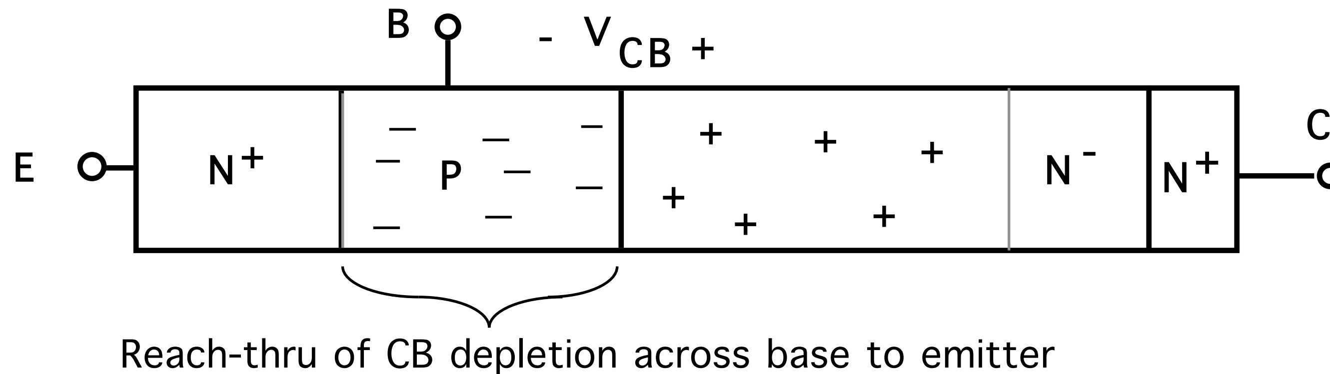
Avoidance of Reach-thru



- Large electric field of depletion region will accelerate electrons from emitter across base and into collector. Resulting large current flow will create excessive power dissipation.

- Avoidance of reach-thru
  - Wide base width so depletion layer width less than base width at CB junction breakdown.
  - Heavier doping in base than in collector so that most of CB depletion layer is in drift region and not in the base.

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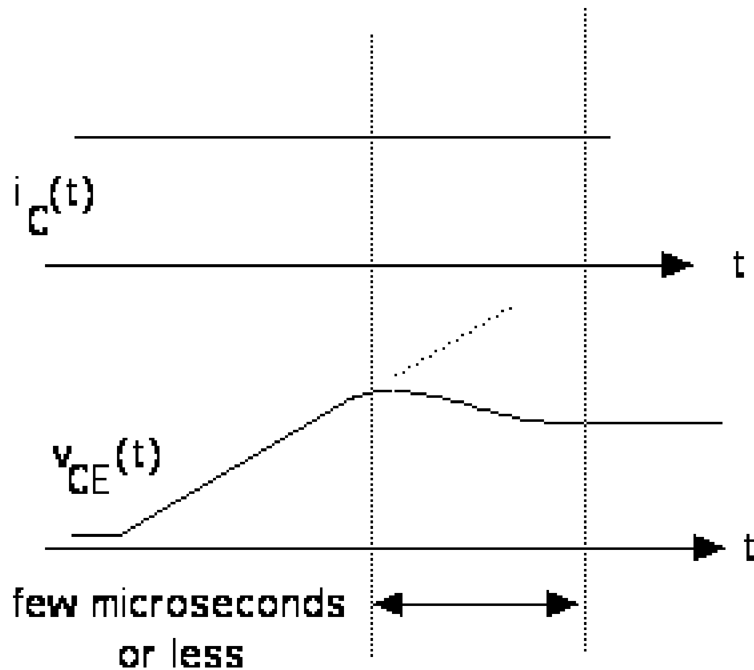
Second Breakdown



- 2nd breakdown during BJT turn-off in step-down converter circuit.

- Precipitious drop in C-E voltage and perhaps rise in collector current.

- Simultaneous rise in highly localized regions of power dissipation and increases in temperature of same regions.

  1. Direct observations via infrared cameras.
  2. Evidence of crystalline cracking and even localized melting.

- Permanent damage to BJT or even device failure if 2nd breakdown not terminated within a few μsec.

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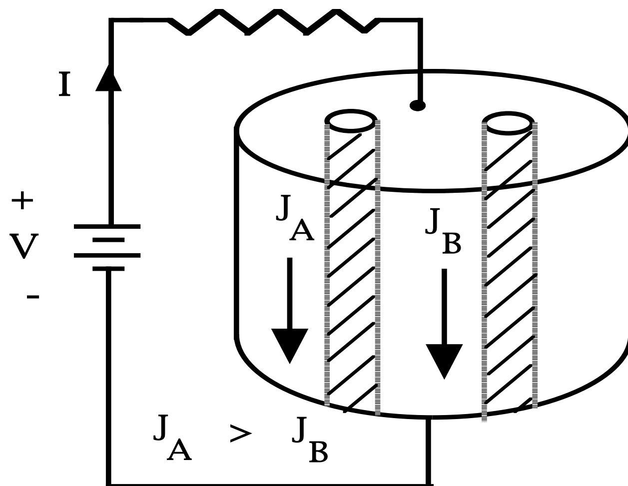
2nd Breakdown and Current Density Nonuniformities

- Minority carrier devices prone to thermal runaway.
  - Minority carrier density proportional to $n_i(T)$ which increases exponentially with temperature.
  - If constant voltage maintained across a minority carrier device, power dissipation causes increases in temp. which in turn increases current because of carrier increases and thus better conduction characteristic.
  - Increase in current at constant voltage increases power dissipation which further increases temperature.
  - Positive feedback situation and potentially unstable. If temp. continues to increase, situation termed thermal runaway.



- Current densities nonuniformities in devices an accenuate problems.
- Assume $J_A > J_B$ and $T_A > T_B$
- As time proceeds, differences in J and T between regions A and B become greater.
- If temp. on region A gets large enough so that n_i > majority carrier doping density, thermal runaway will occur and device will be in 2nd breakdown.

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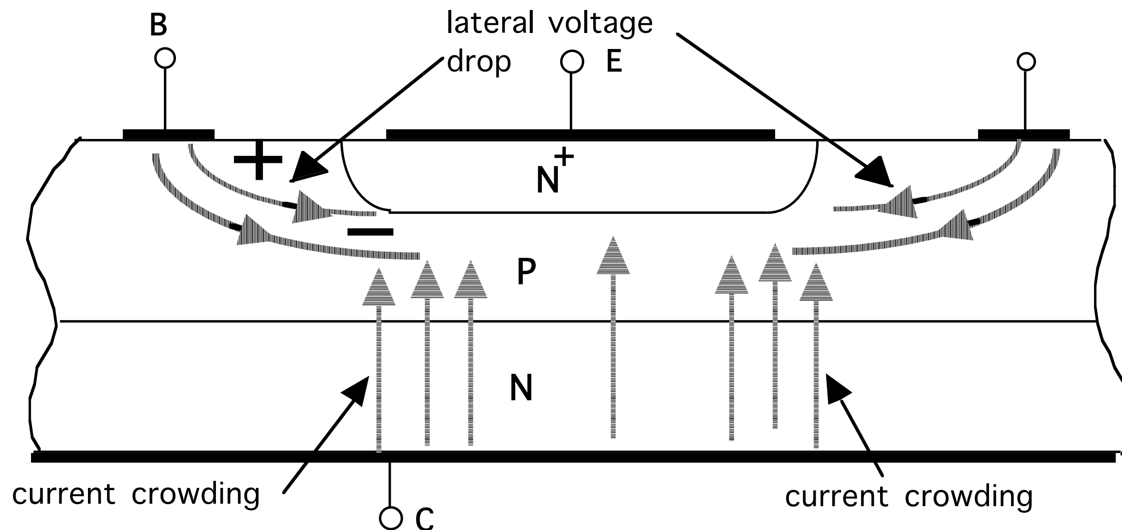
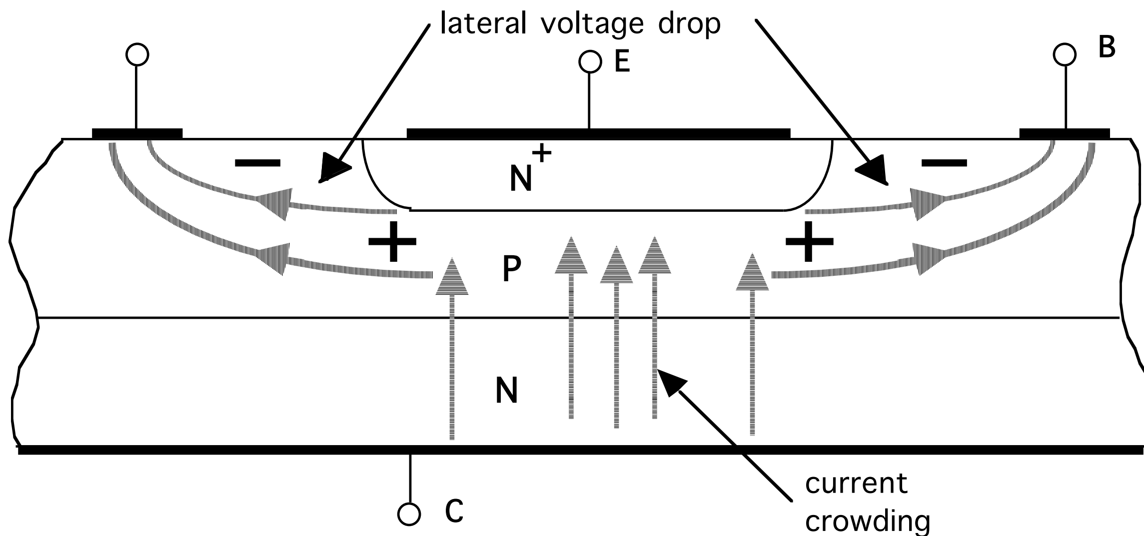
Current Crowding Enhancement of 2nd Breakdown Susceptibility





- Emitter current crowding during either turn-on or turn-off accenuates propensity of BJTs to 2nd breakdown.
- Minimize by dividing emitter into many narrow areas connected electrically in parallel.

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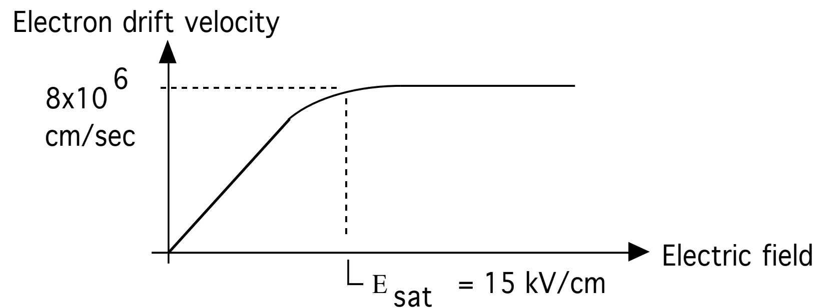
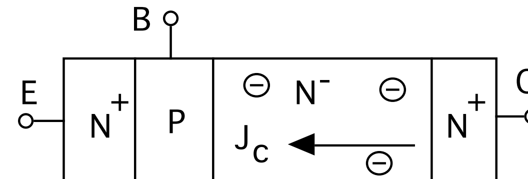
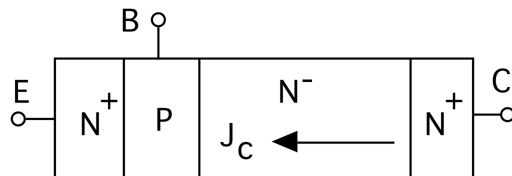
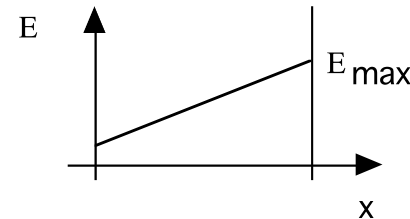
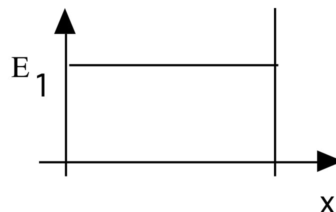
Velocity Saturation and Second Breakdown











- Moderate current in drift region - BJT active
- Electric field $E_1 = J_c/(q\mu_n N_d) < E_{sat}$

- Large current density in drift region - BJT active.
- $J_c > q\mu_n N_d E_{sat}$. Extra electrons needed to carry extra current.
- Negative space density gives rise to nonuniform electric field.
- E_{max} may exceed impact ionization threshold while total voltage < BV_{CEO}.

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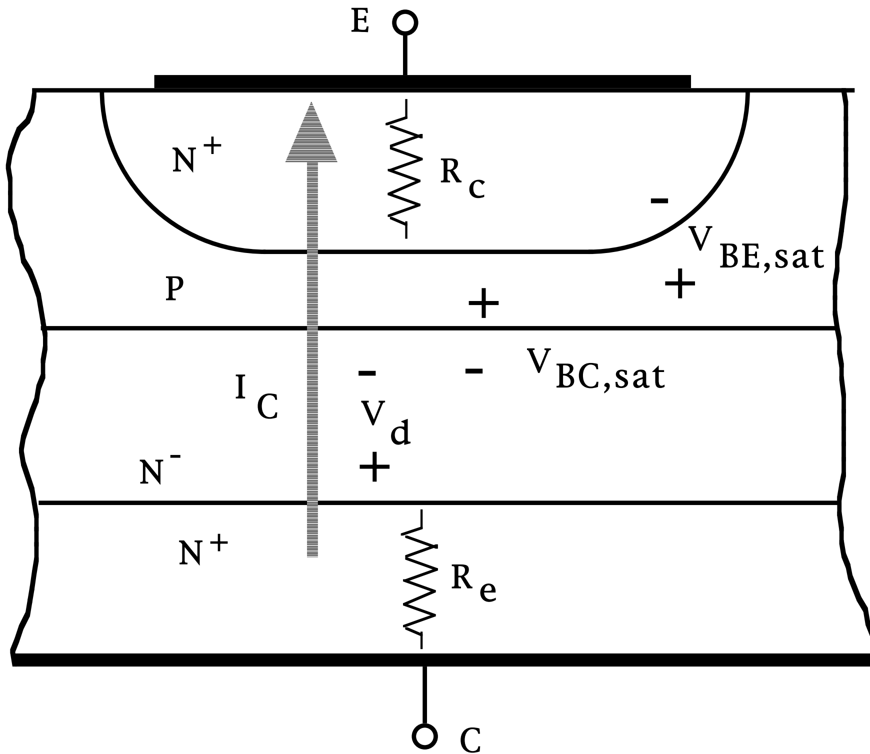
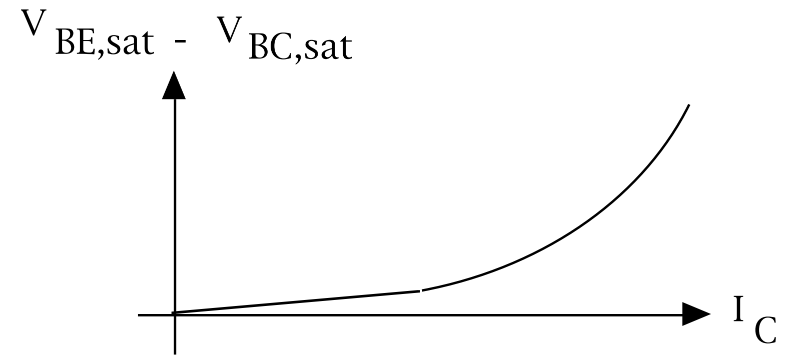
Contributions to BJT On-State Losses





- $P_{on} = I_C V_{CE,sat}$
- $V_{CE,sat} = V_{BE,sat} - V_{BC,sat} + V_d + I_C(R_c + R_e)$
- $V_{BE,sat} - V_{BC,sat}$ typically 0.1-0.2 V at moderate values of collector current.
- Rise in $V_{BE,sat} - V_{BC,sat}$ at larger currents due to emitter current crowding and conductivity modulation in base.

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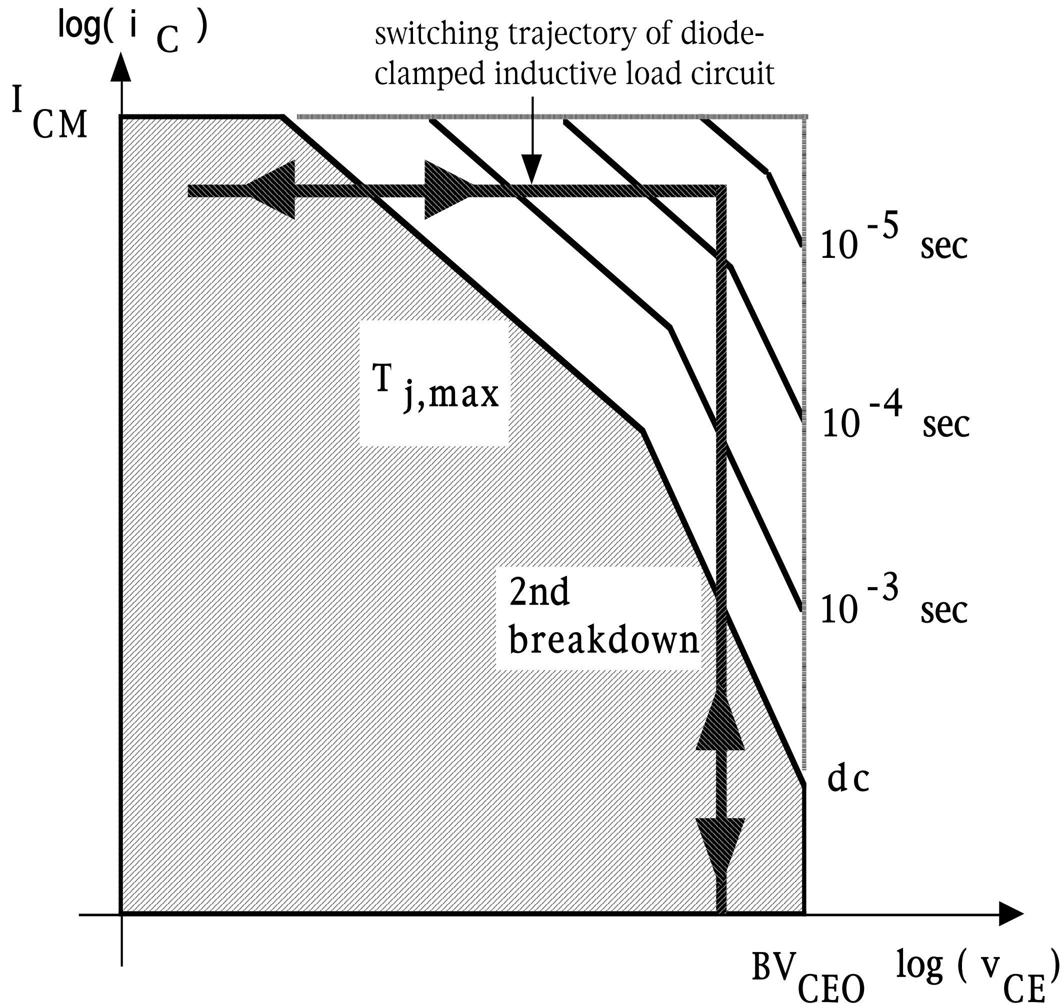
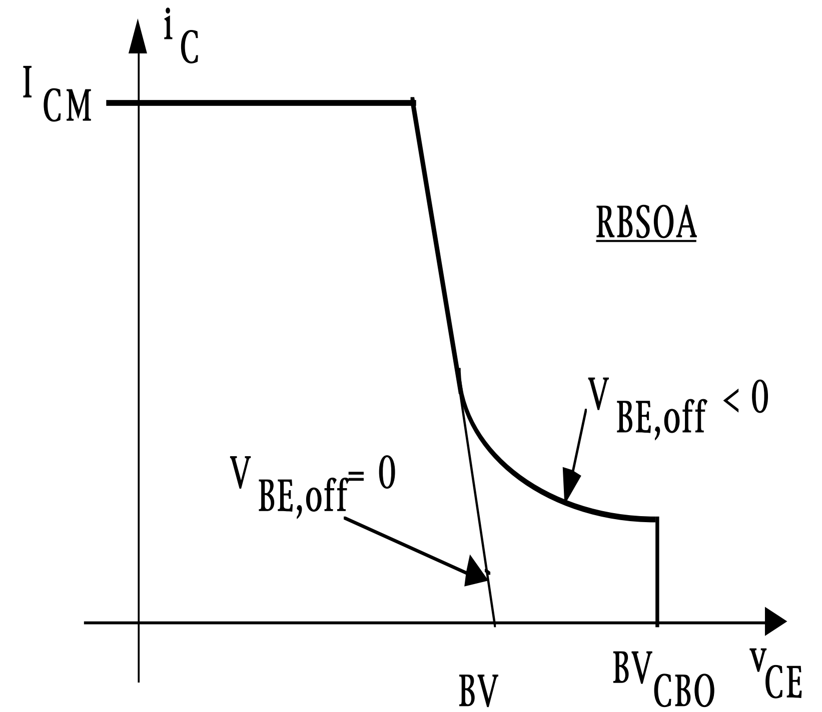
BJT Safe Operating Areas

Forward bias safe operating area



Reverse bias safe operating area



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Lecture Notes

Power MOSFETs

Outline

- Construction of power MOSFETs
- Physical operations of MOSFETs
- Power MOSFET switching Characteristics
- Factors limiting operating specfications of MOSFETs
- COOLMOS
- PSPICE and other simulation models for MOSFETs

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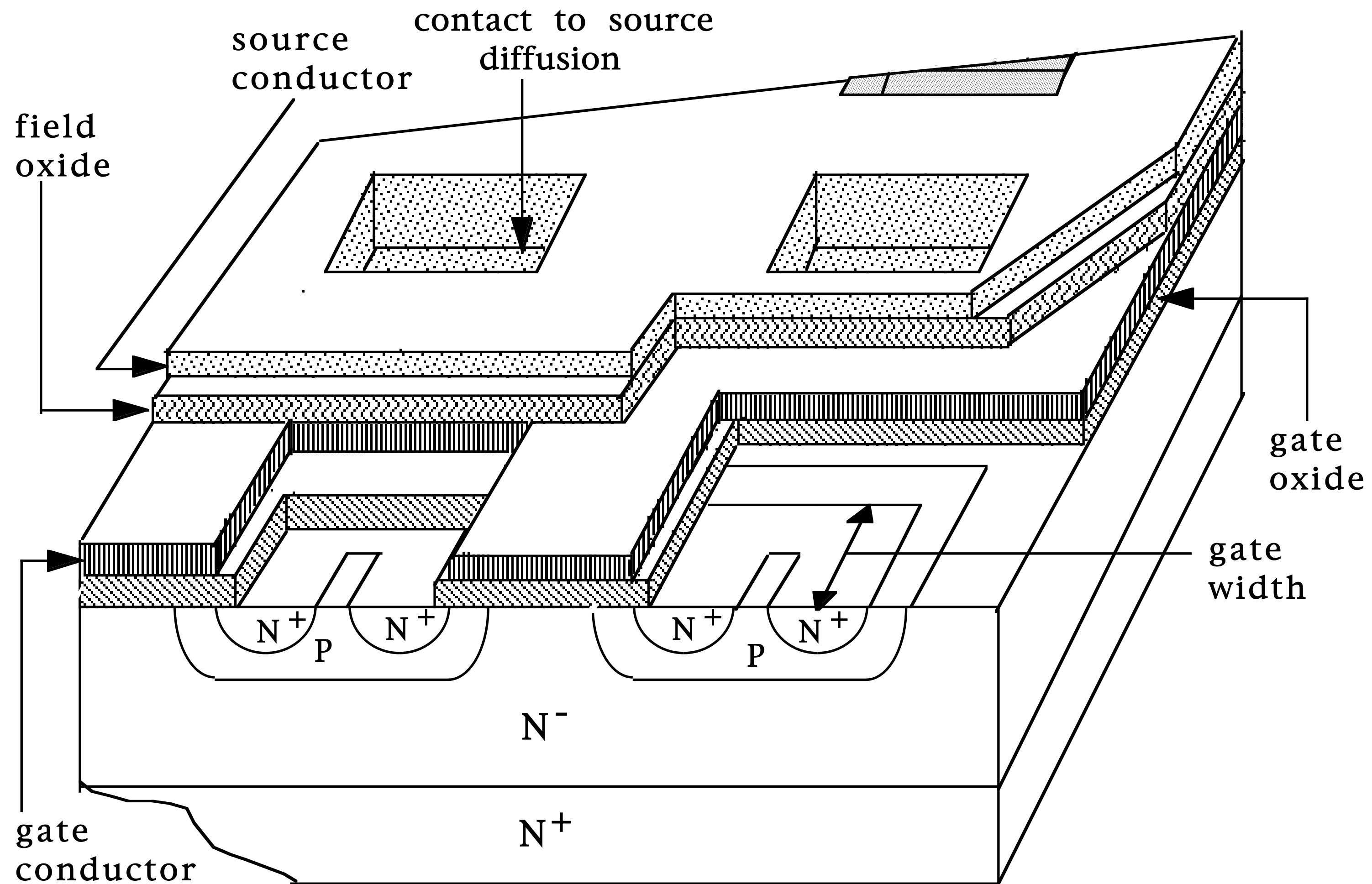
Multi-cell Vertical Diffused Power MOSFET (VDMOS)



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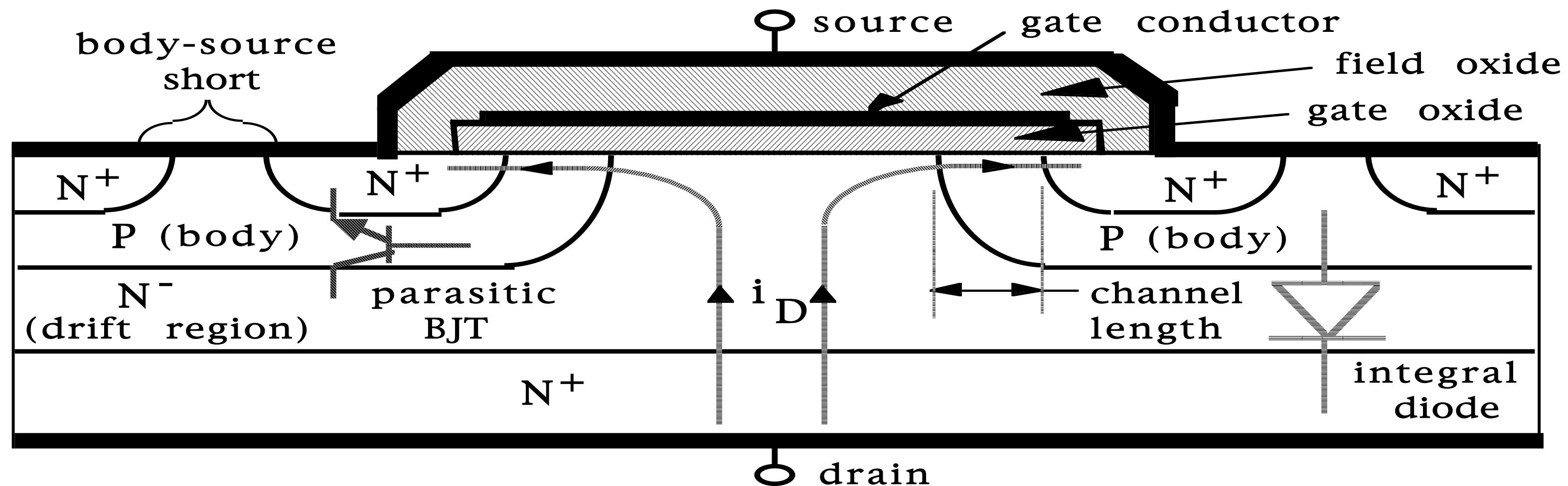
Important Structural Features of VDMOS



1. Parasitic BJT. Held in cutoff by body-source short

2. Integral anti-parallel diode. Formed from parasitic BJT.

3. Extension of gate metallization over drain drift region. Field plate and accumulation layer functions.

4. Division of source into many small areas connected electrically in parallel. Maximizes gate width-to-channel length ratio in order to increase gain.

5. Lightly doped drain drift region. Determines blocking voltage rating.

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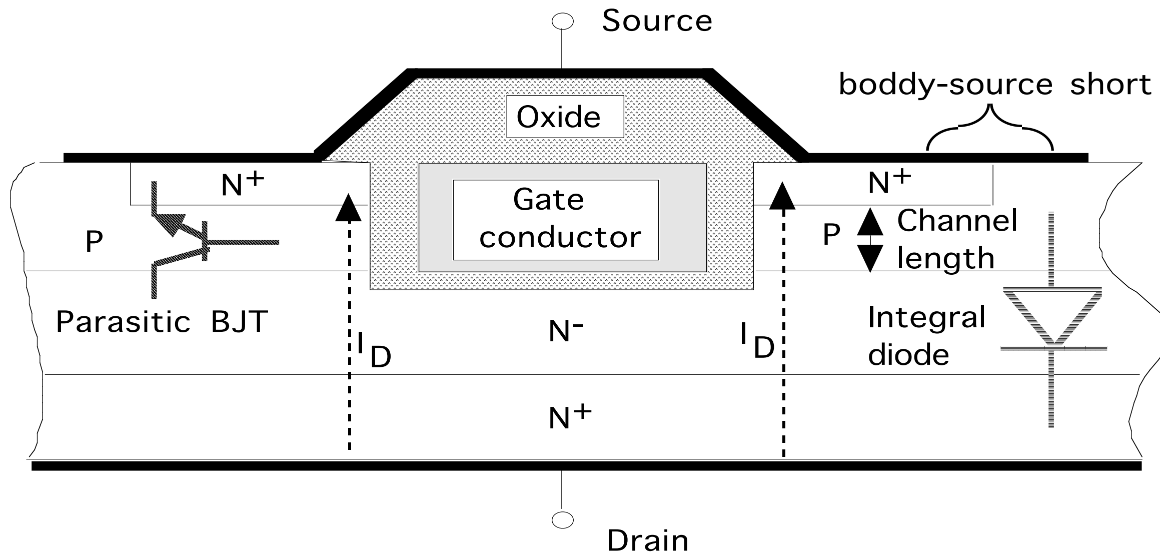
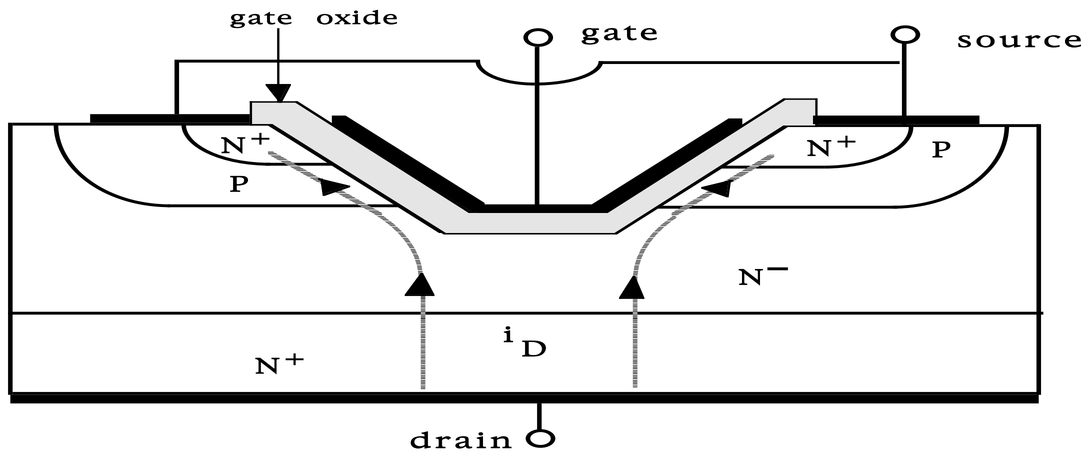
Alternative Power MOSFET Geometries



- Trench-gate MOSFET
- Newest geometry. Lowest on-state resistance.



- V-groove MOSFET.
- First practical power MOSFET.
- Higher on-state resistance.

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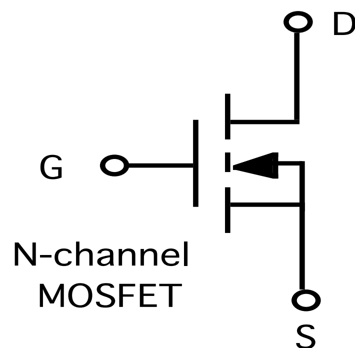
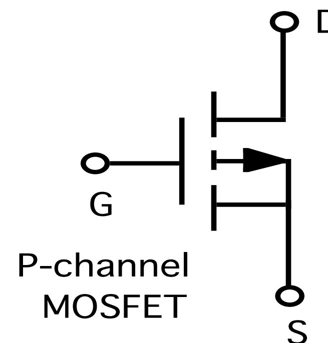
MOSFET I-V Characteristics and Circuit Symbols

i_D
ohmic
$[v_{GS} - V_{GS(th)} = v_{DS}]$
v_{GS5}
active
v_{GS4}
v_{GS3}
v_{GS2}
v_{GS1}
$v_{GS} < V_{GS(th)}$
BV_{DSS}
v_{DS}

actual
linearized
$V_{GS(th)}$
v_{GS}





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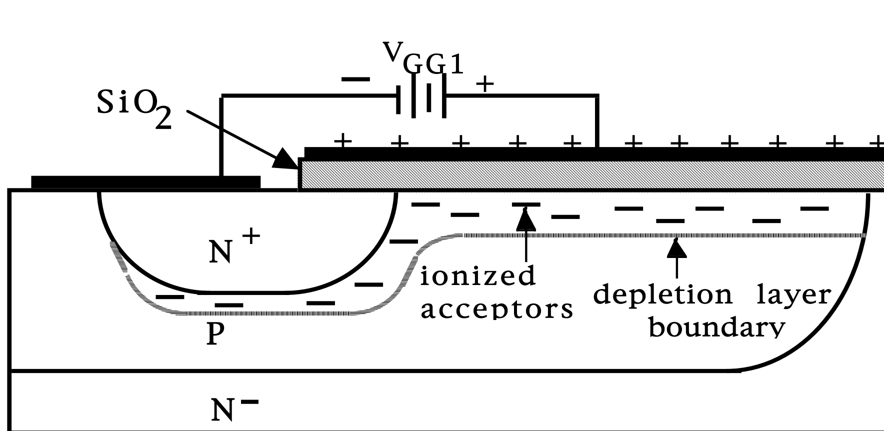
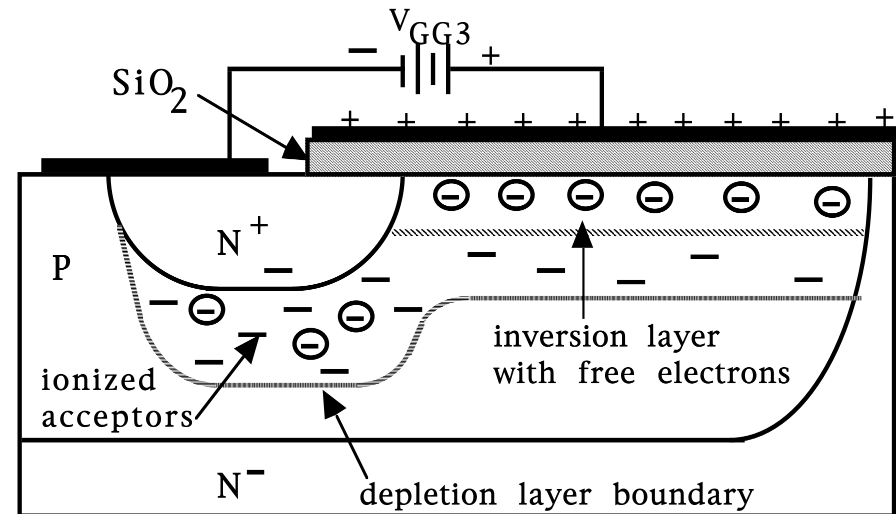
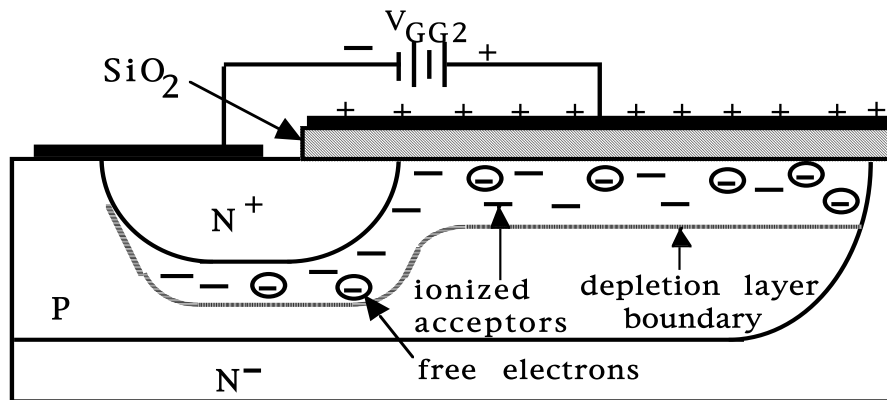
The Field Effect - Basis of MOSFET Operation







Threshold Voltage $V_{GS(th)}$

- V_{GS} where strong inversion layer has formed. Typical values 2-5 volts in power MOSFETs

- Value determined by several factors
  1. Type of material used for gate conductor
  2. Doping density of body region directly beneath gate
  3. Impurities/bound charges in oxide
  4. Oxide capacitance per unit area $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

  t_{ox} = oxide thickness

- Adjust threshold voltage during device fabrication via an ion implantation of impurities into body region just beneath gate oxide.

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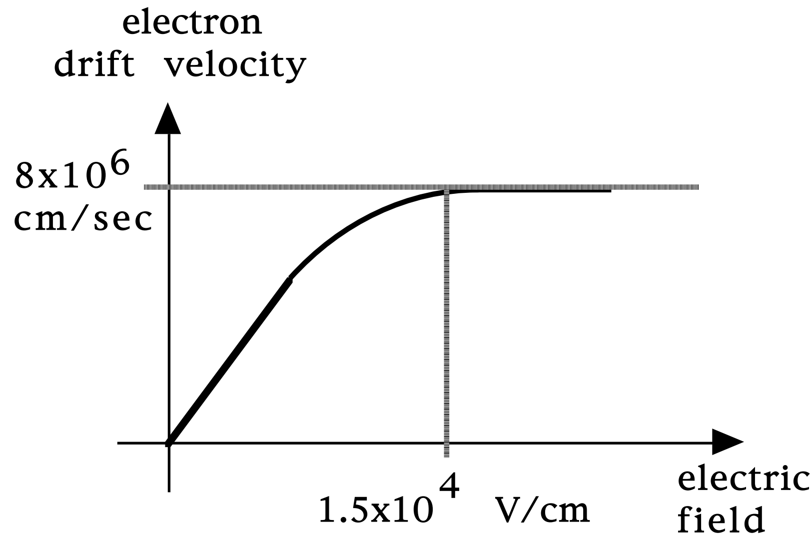
Drift Velocity Saturation



- In MOSFET channel, $J = q\,\mu_n\,n\,E = q\,n\,v_n$; velocity $v_n = \mu_n E$
- Velocity saturation means that the mobility μ_n inversely proportional to electric field E.

- Mobility also decreases because large values of V_{GS} increase free electron density.
- At larger carrier densities, free carriers collide with each other (carrier-carrier scattering) more often than with lattice and mobility decreases as a result.
- Mobilty decreases, especially via carrier-carrier scattering leead to linear transfer curve in power devices instead of square law transfer curve of logic level MOSFETs.

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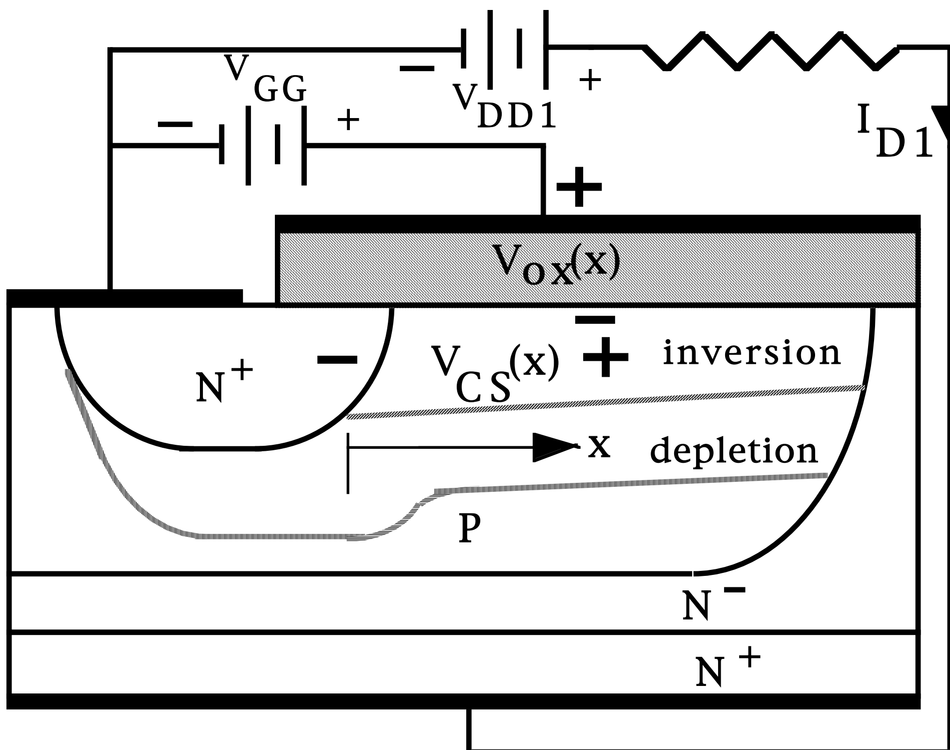
Channel-to-Source Voltage Drop



- $V_{GS} = V_{GG} = V_{ox} + V_{CS}(x)$; $V_{CS}(x) = I_{D1}R_{CS}(x)$
- Larger x value corresponds be being closer to the drain and to a smaller V_{ox}.
- Smaller V_{ox} corresponds to a smaller channel thickness. Hence reduction in channel thickness as drain is approached from the source.

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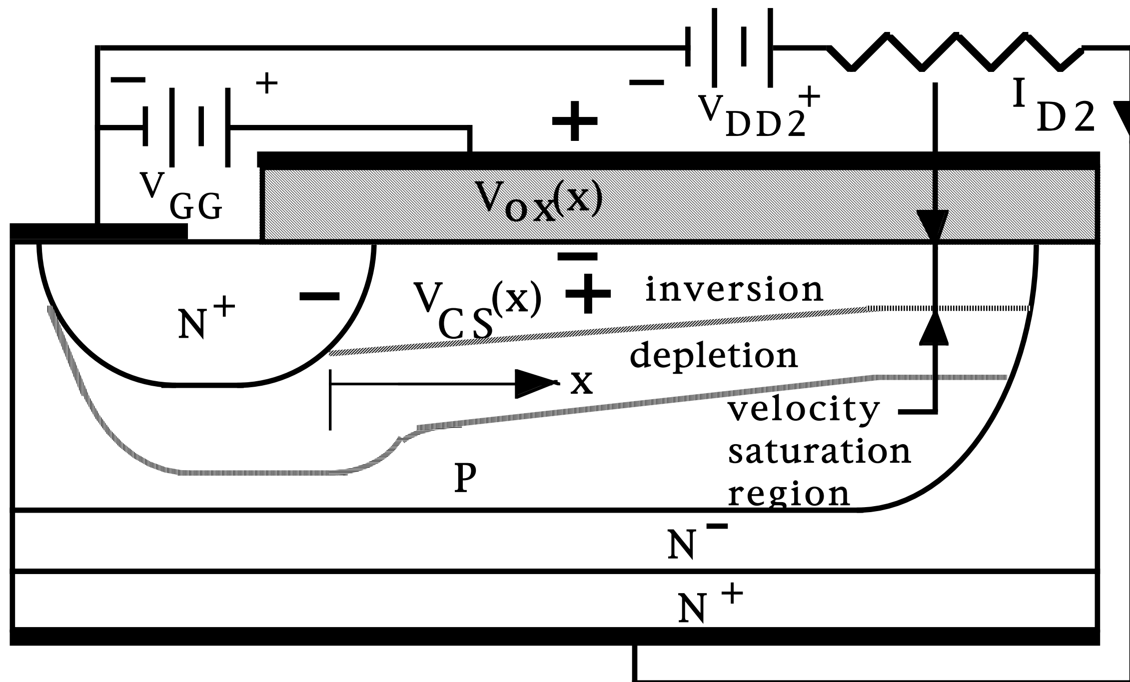
Channel Pinch-off at Large Drain Current



- $I_{D2} > I_{D1}$ so $V_{CS2}(x) > V_{CS1}(x)$ and thus channel narrower at an given point.
- Total channel resistance from drain to source increasing and curve of I_D vs V_{DS} for a fixed V_{GS} flattens out.

- Apparent dilemma of channel disappearing at drain end for large I_D avoided.

1. Large electric field at drain end oriented parallel to drain current flow. Arises from large current flow in channel constriction at drain.
2. This electric field takes over maintenance of minimum inversion layer thickness at drain end.

- Larger gate-source bias V_{GG} postpones flattening of I_D vs V_{DS} until larger values of drain current are reached.

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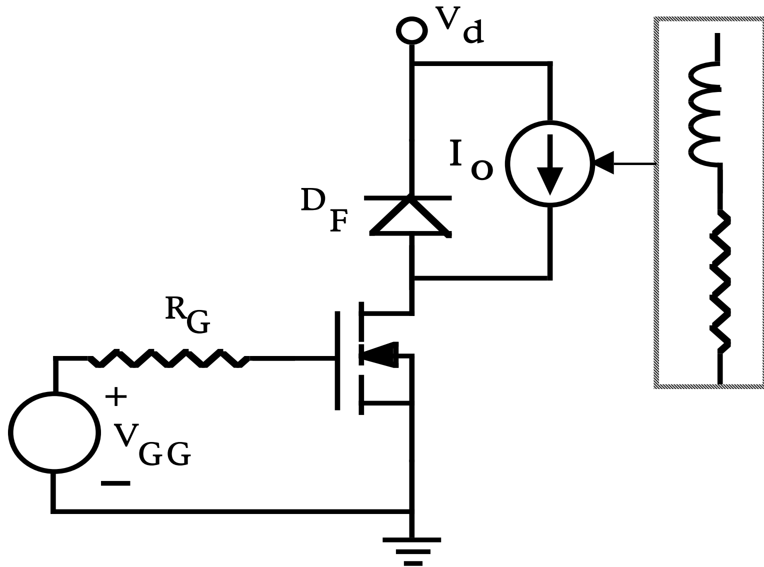
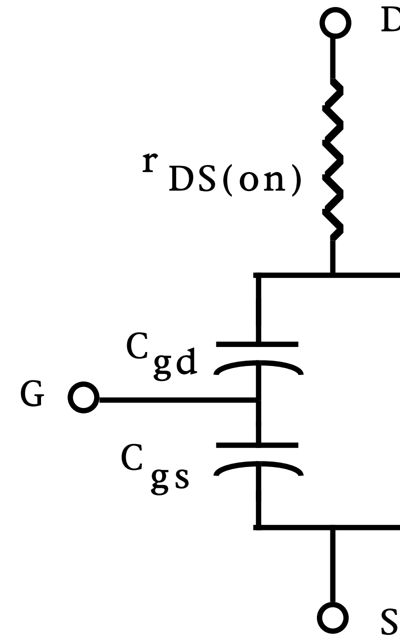
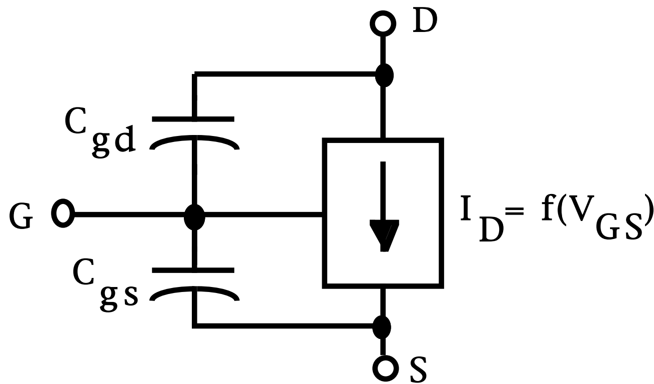
MOSFET Switching Models for Buck Converter



• Buck converter using power MOSFET.



• MOSFET equivalent circuit valid for on-state (triode) region operation.



• MOSFET equivalent circuit valid for off-state (cutoff) and active region operation.

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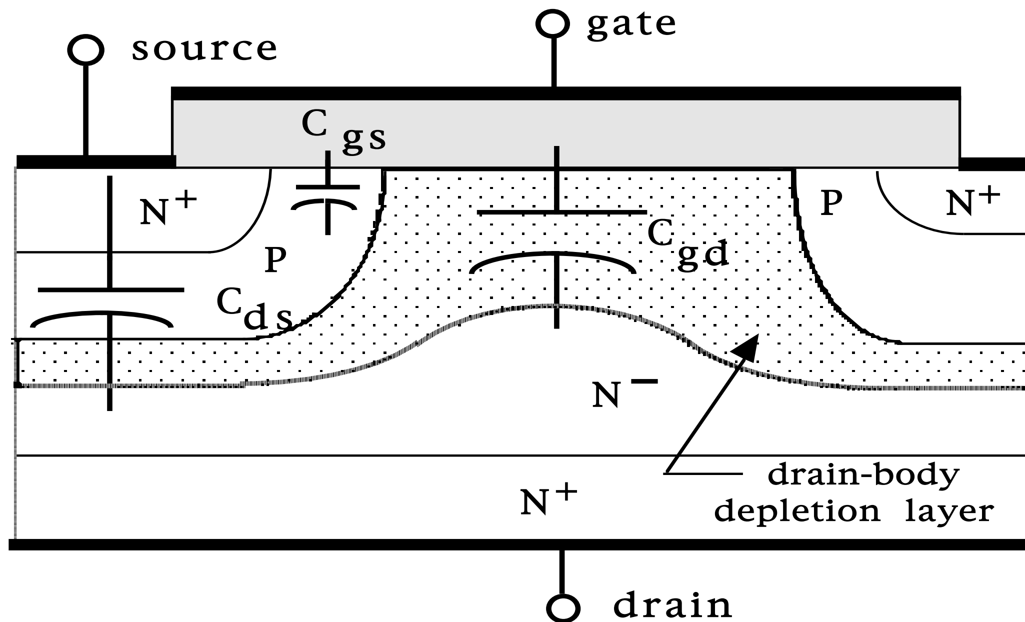
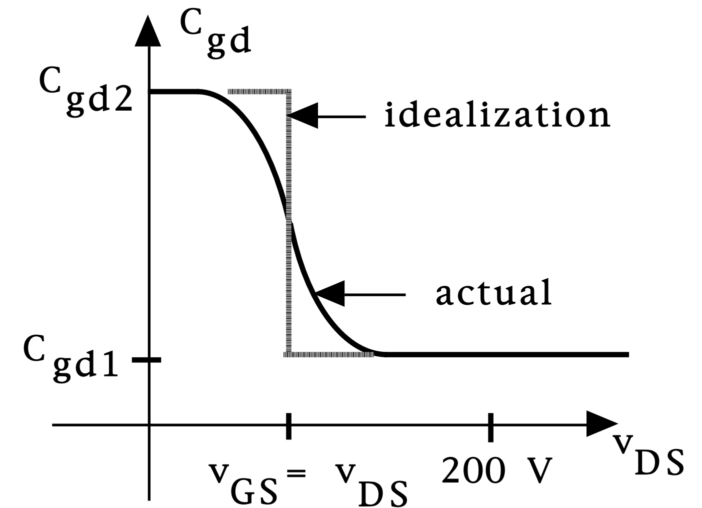
MOSFET Capacitances Determining Switching Speed





- Gate-source capacitance Cgs approximately constant and independent of applied voltages.
- Gate-drain capacitance C_{gd} varies with applied voltage. Variation due to growth of depletion layer thickness until inversion layer is formed.

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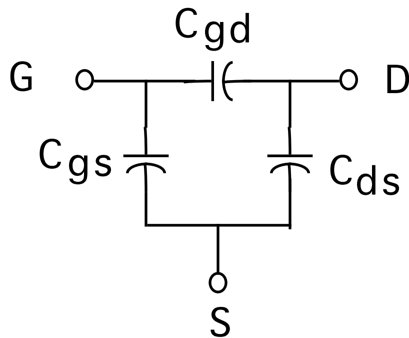
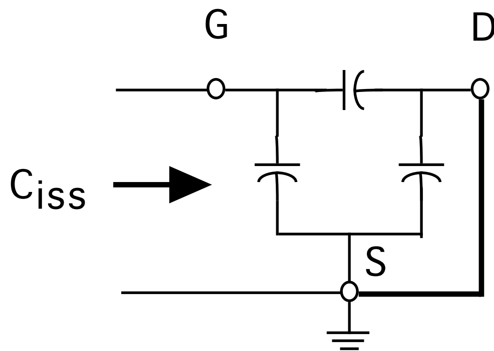
Internal Capacitances Vs Spec Sheet Capacitances

MOSFET internal capacitances

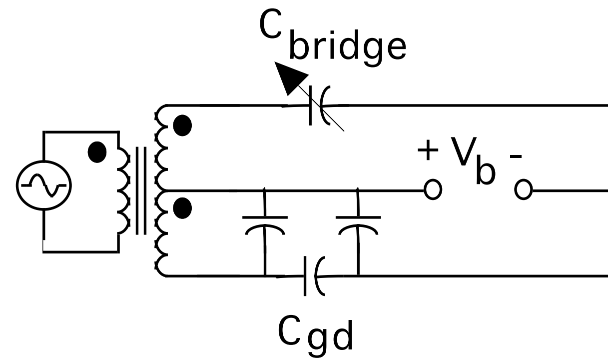


Input capacitance



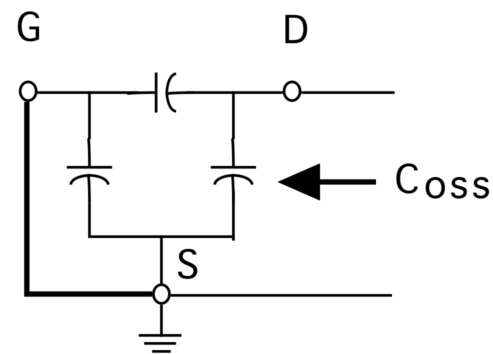
$C_{iss} = C_{gs} + C_{gd}$

Reverse transfer or feedback capacitance



Bridge balanced (Vb=0) Cbridge = Cgd $= C_{rss}$

Output capacitance



$C_{oss} = C_{gd} + C_{ds}$

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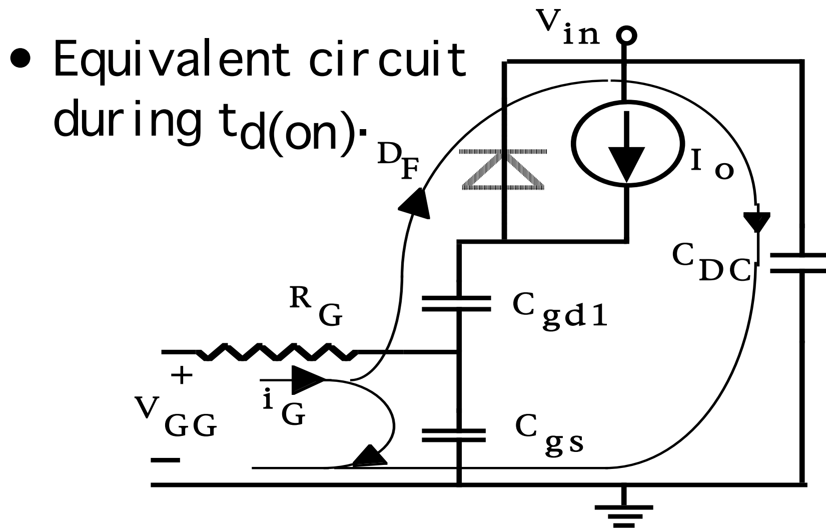
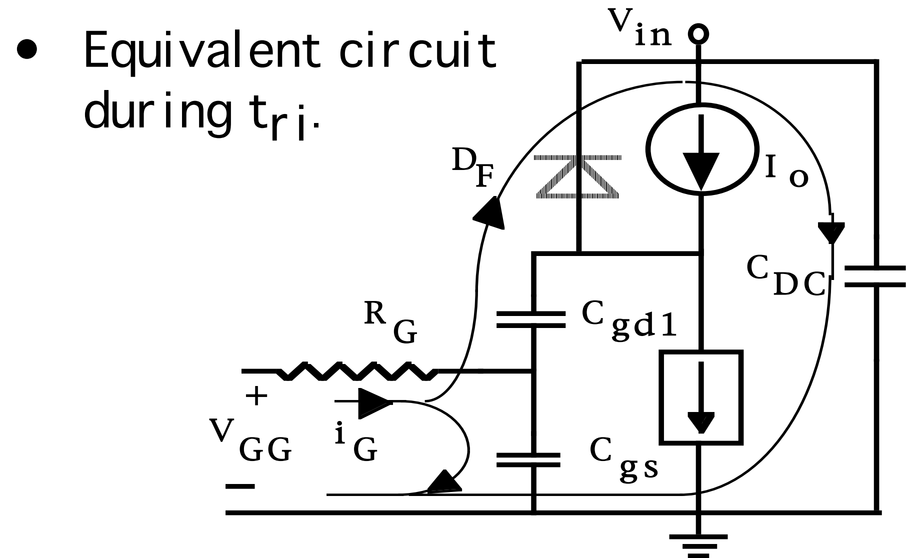
Turn-on Equivalent Circuits for MOSFET Buck Converter

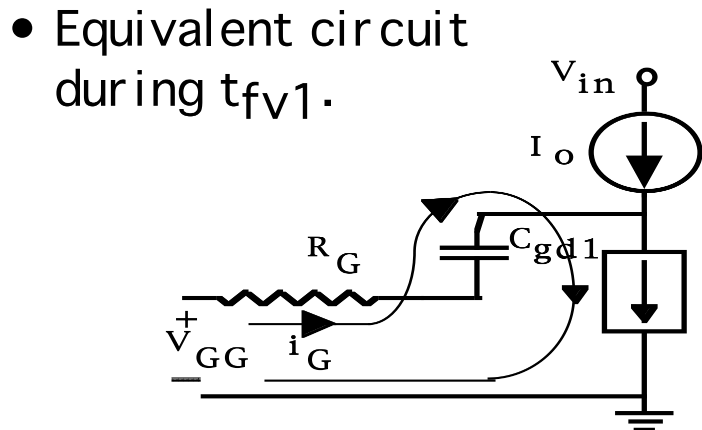
- Equivalent circuit during $t_{d(on)}$.



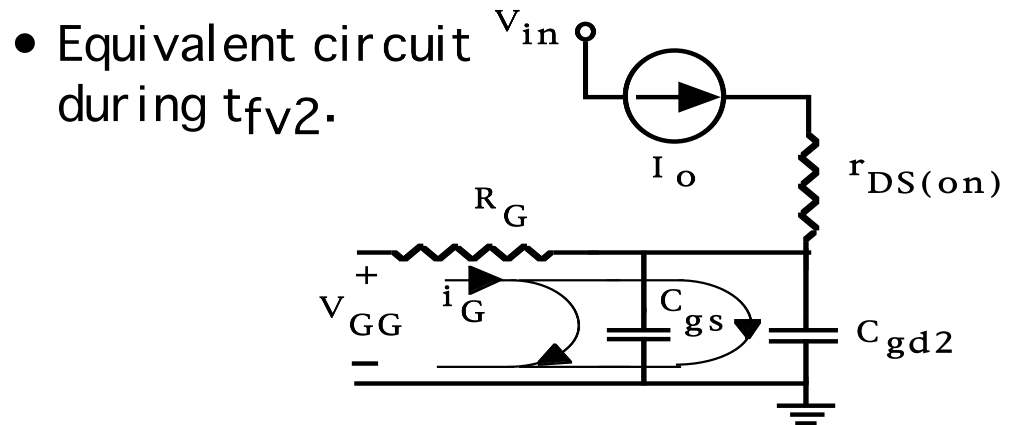
- Equivalent circuit during t_{ri}.



- Equivalent circuit during t_{fv1}.



- Equivalent circuit during t_{fv2}.



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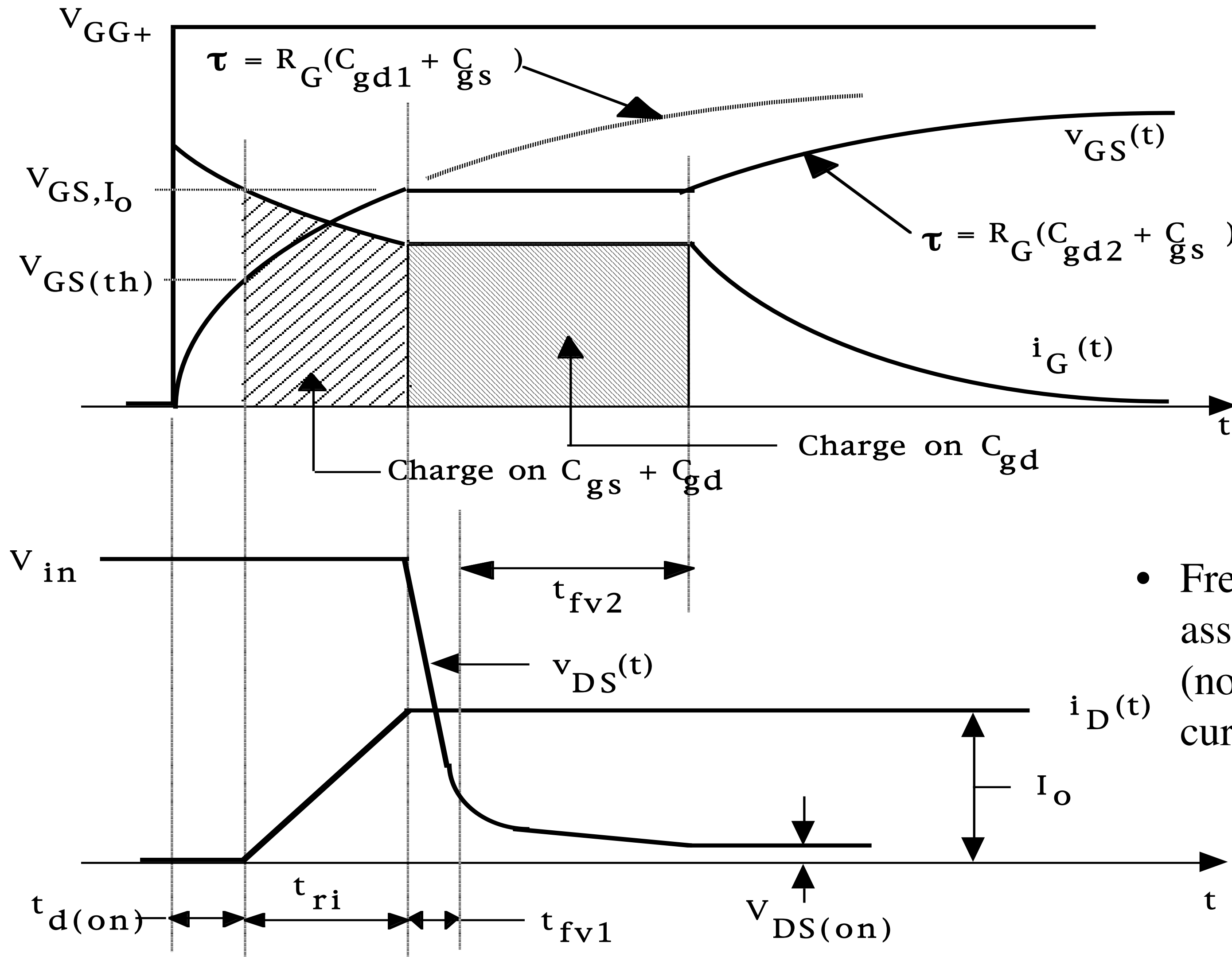
MOSFET-based Buck Converter Turn-on Waveforms



- Free-wheeling diode assumed to be ideal. (no reverse recovery current).

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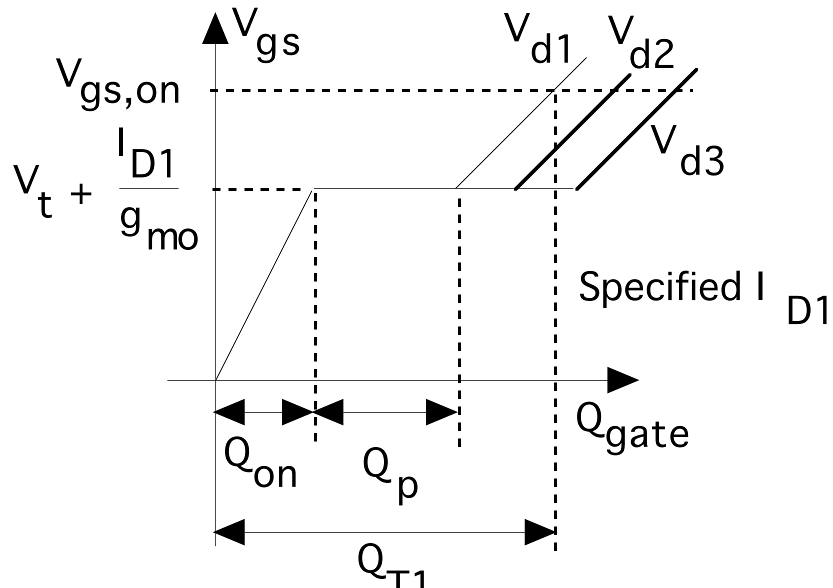
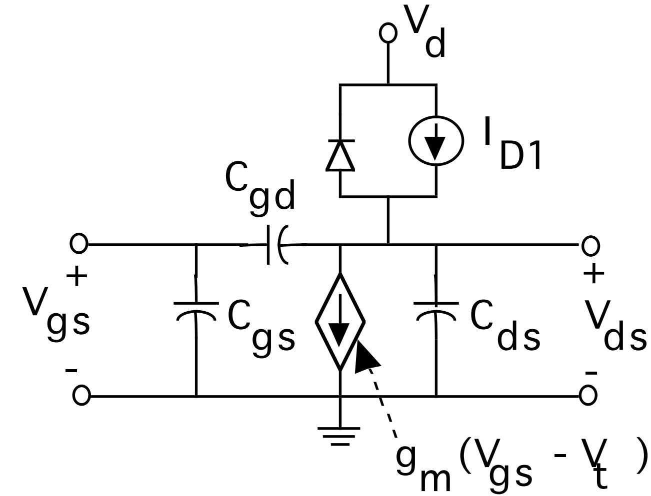
Turn-on Gate Charge Characteristic

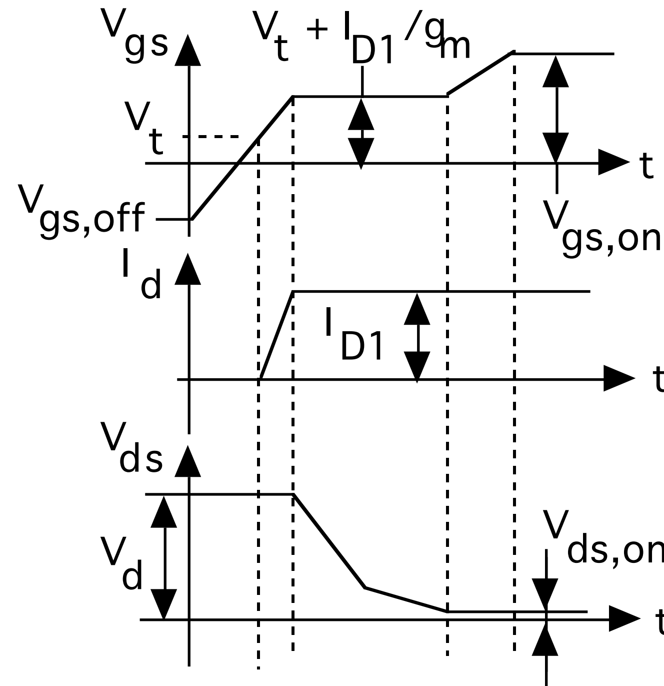




$$Q_{on} = \int_{V_{gs,off}}^{(V_t+I_{D1}/g_m)} [C_{gs}(V_{gs}) + C_{gd}(V_{gs})]\, V_{gs}\, dV_{gs}$$

$$Q_p = \int_{V_d}^{V_{ds,on}} C_{gd}(V_{ds})\, V_{ds}\, dV_{ds}$$

$$Q_T = Q_{on} + Q_p + \int_{(V_t+I_{D1}/g_m)}^{V_{gs,on}} [C_{gs}(V_{gs}) + C_{gd}(V_{gs})]\, V_{gs}\, dV_{gs}$$



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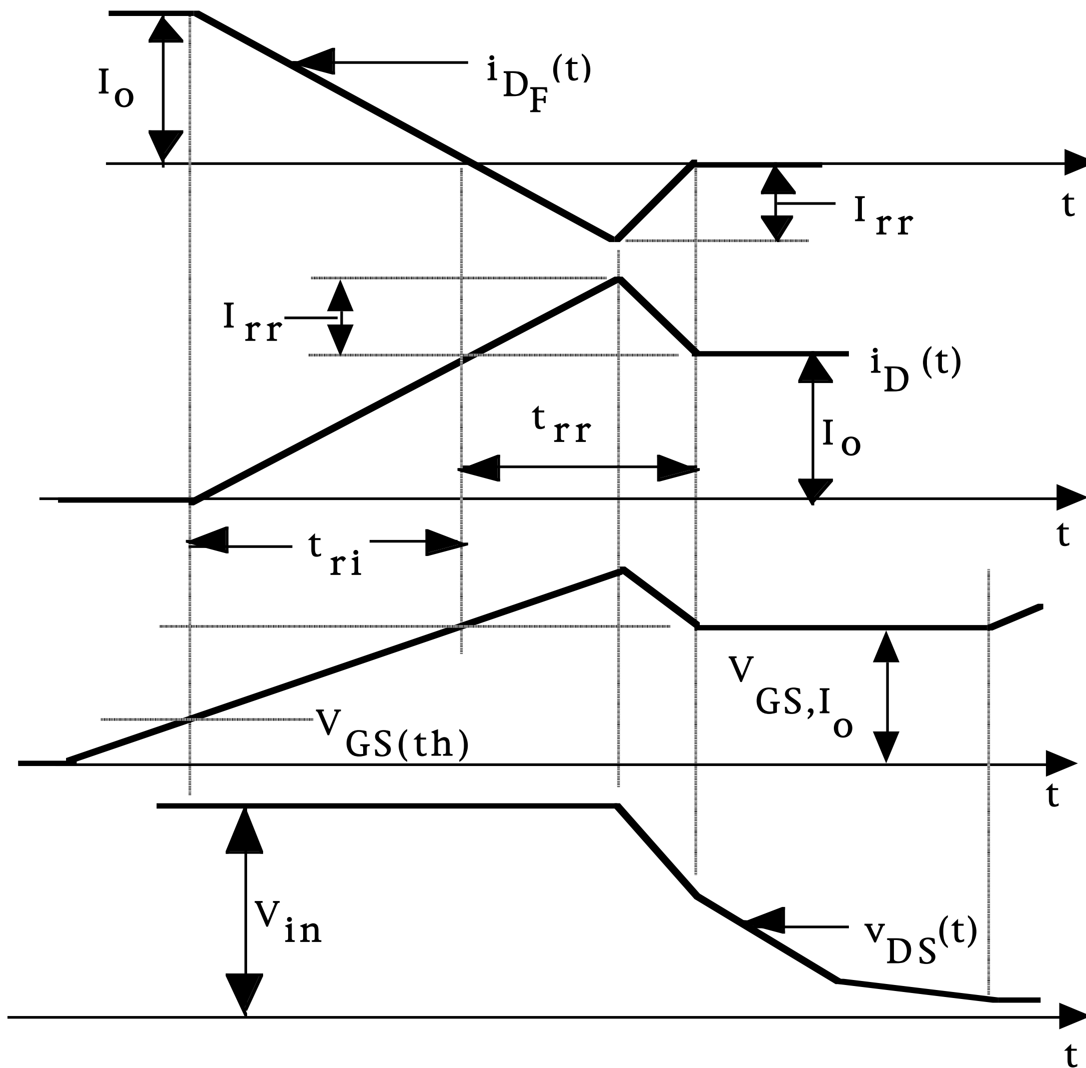
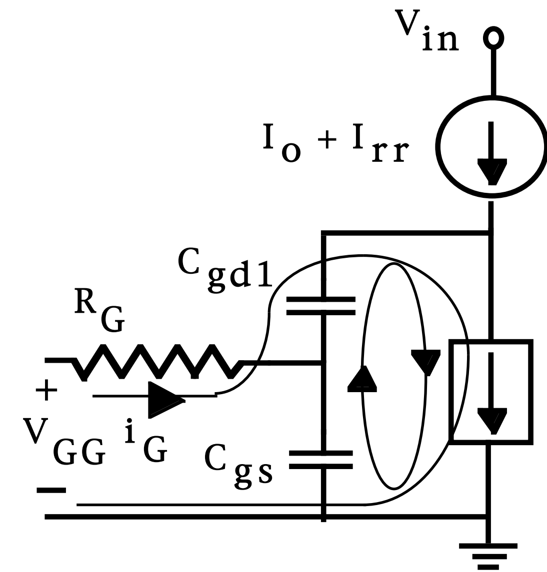
Turn-on Waveforms with Non-ideal Free-wheeling Diode





- Equivalent circuit for estimating effect of free-wheeling diode reverse recovery.

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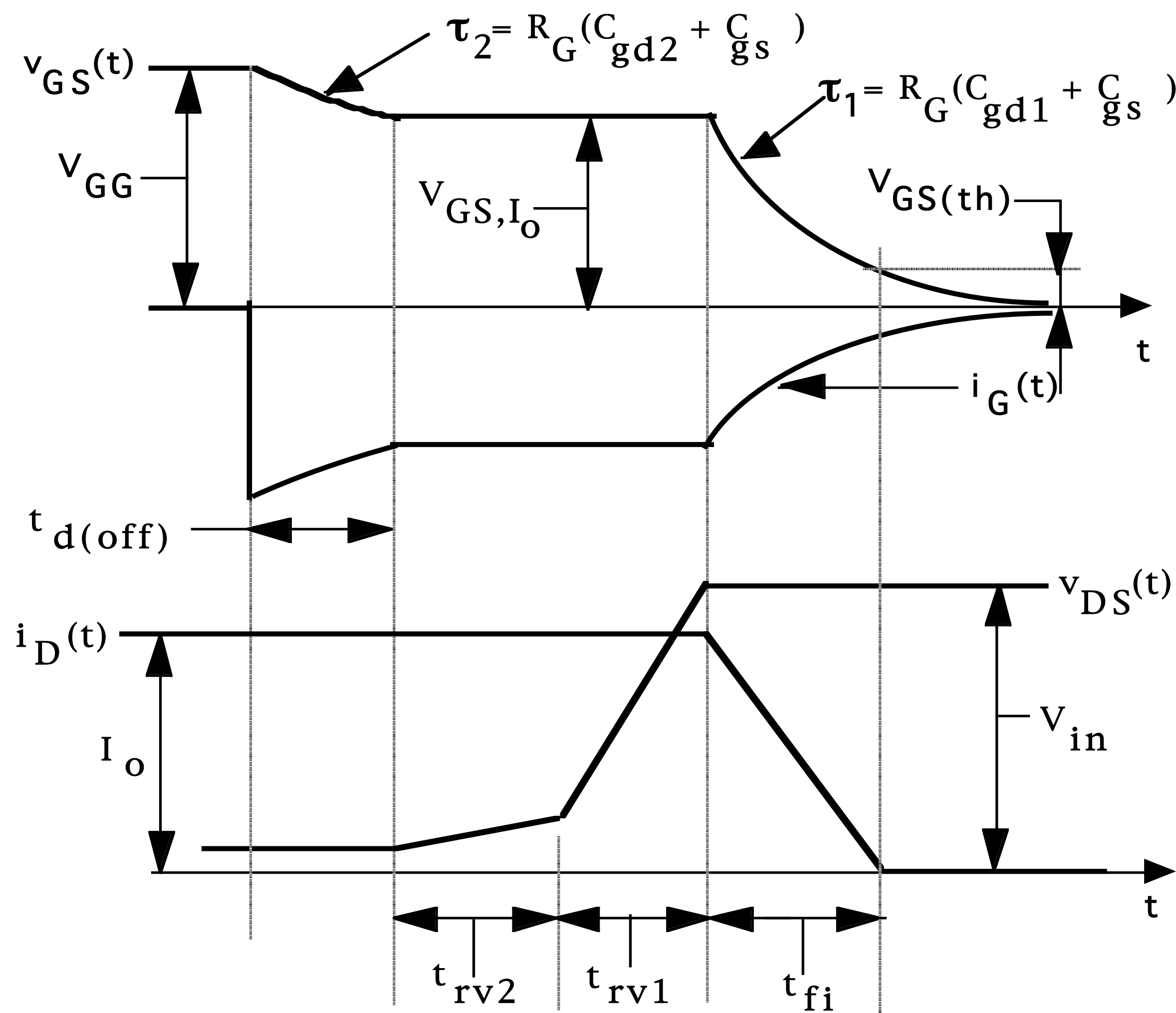
MOSFET-based Buck Converter Turn-off Waveforms



- Assume ideal free-wheeling diode.
- Essentially the inverse of the turn-on process.
- Model quanitatively using the same equivalent circuits as for turn-on. Simply use correct driving voltages and initial conditions

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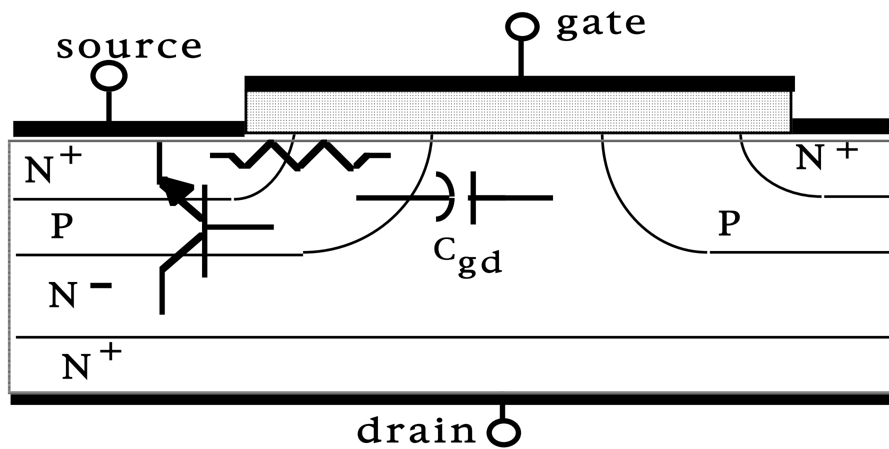
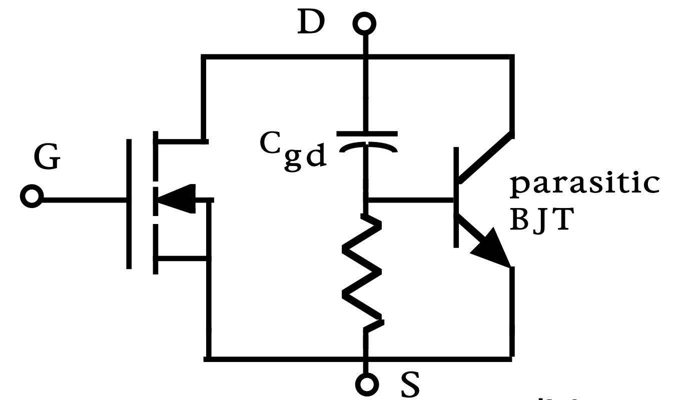
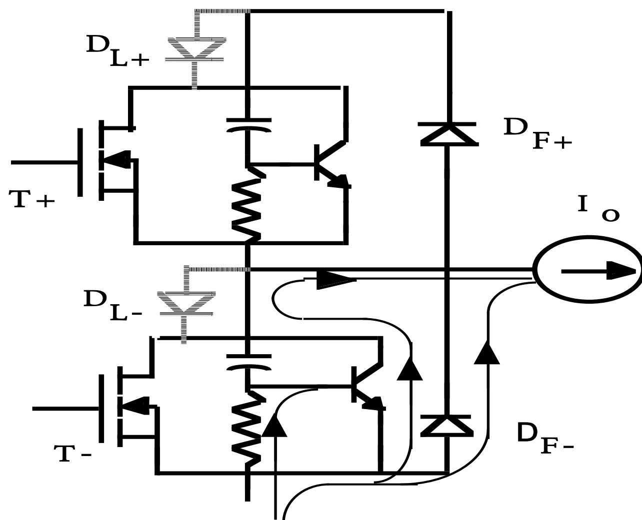
dV/dt Limits to Prevent Parasitic BJT Turn-on





- Large positive $C_{gd} \frac{dV_{DS}}{dt}$ could turn on parasitic BJT.



- Turn-on of T_+ and reverse recovery of D_{f-} will produce large positive $C_{gd} \frac{dv_{DS}}{dt}$ in bridge circuit.

- Parasitic BJT in T_- likely to have been in reverse active mode when D_{f-} was carrying current. Thus stored charge already in base which will increase likeyhood of BJT turn-on when positive $C_{gd} \frac{dv_{DS}}{dt}$ is generated.

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Maximum Gate-Source Voltage

- $V_{GS(max)}$ = maximum permissible gate-source voltage.
- If $V_{GS} > V_{GS(max)}$ rupture of gate oxide by large electric fields possible.
- E_{BD}(oxide) ≈ 5-10 million V/cm
  - Gate oxide typically 1000 anstroms thick
  - $V_{GS(max)} < [5x10^6][10^{-5}] = 50$ V
  - Typical $V_{GS(max)}$ 20 - 30 V
- Static charge on gate conductor can rupture gate oxide
  - Handle MOSFETs with care (ground yourself before handling device)
  - Place anti-parallel connected Zener diodes between gate and source as a protective measure

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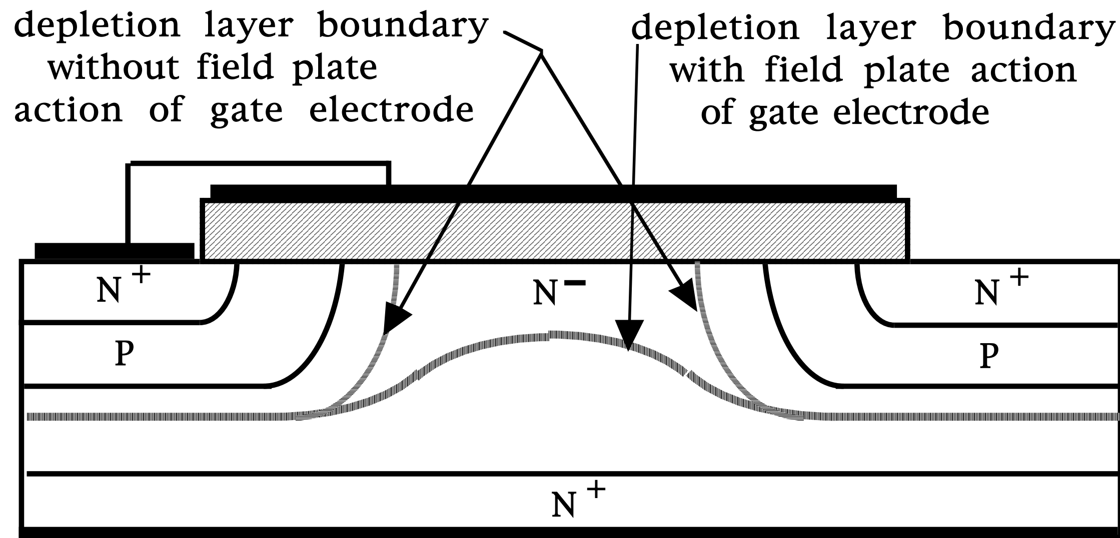
MOSFET Breakdown Voltage



- BV_{DSS} = drain-source breakdown voltage with V_{GS} = 0
- Caused by avalanche breakdown of drain-body junction
- Achieve large values by

  1. Avoidance of drain-source reach-through by heavy doping of body and light doping of drain drift region
  2. Appropriate length of drain drift region
  3. Field plate action of gate conductor overlap of drain region
  4. Prevent turn-on of parasitic BJT with body-source short (otherwise BV_{DSS} = BV_{CEO} instead of BV_{CBO})

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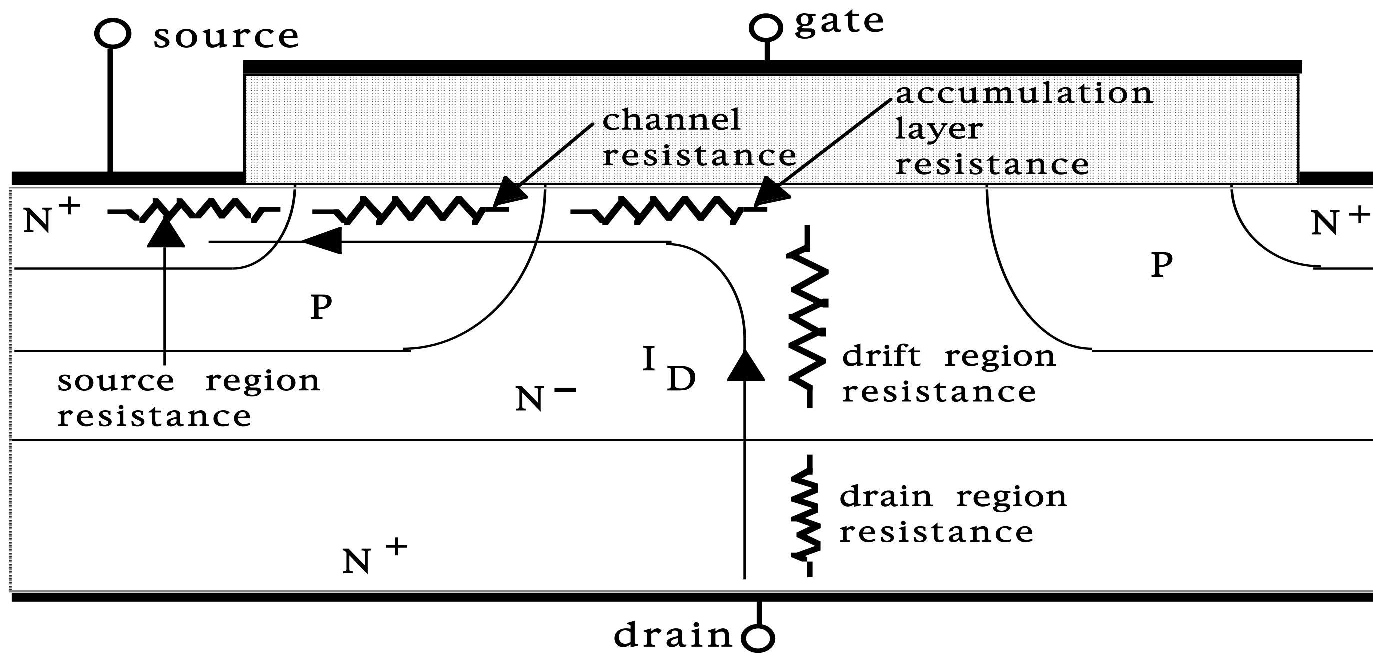
MOSFET On-state Losses



- On-state power dissipation $P_{on} = I_o^2 \, r_{DS(on)}$
- Large V_{GS} minimizes accumulation layer resistance and channel resistance
- $r_{DS(on)}$ dominated by drain drift resistance for BV_{DSS} > few 100 V
- $r_{DS(on)} = \frac{V_d}{! \, I_D} \approx 3 \times 10^{-7} \frac{BV_{DSS}^2}{A}$
- $r_{DS(on)}$ increases as temperature increases. Due to decrease in carrier mobility with increasing temperature.

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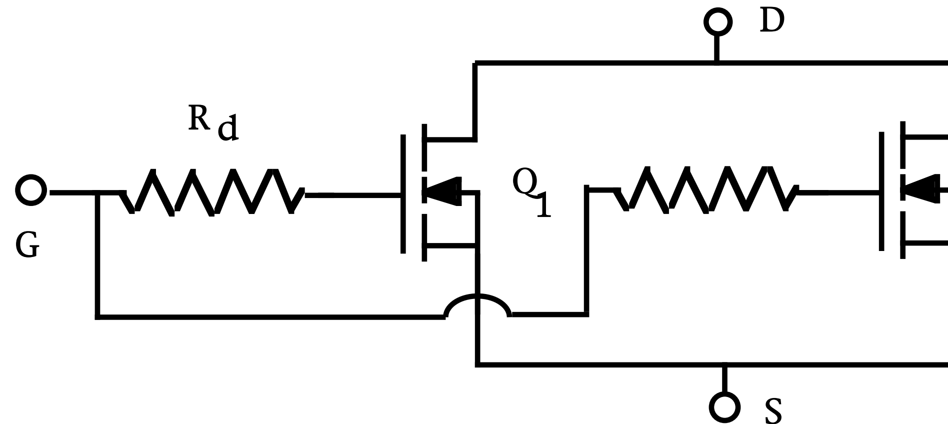
Paralleling of MOSFETs

- MOSFETs can be easily paralleled because of positive temperature coefficient of $r_{DS(on)}$.



- Positive temperature coefficient leads to thermal stabilization effect.
  - If $r_{DS(on)1} > r_{DS(on)2}$ then more current and thus higher power dissipation in Q_2.
  - Temperature of Q_2 thus increases more than temperature of Q_1 and $r_{DS(on)}$ values become equalized.

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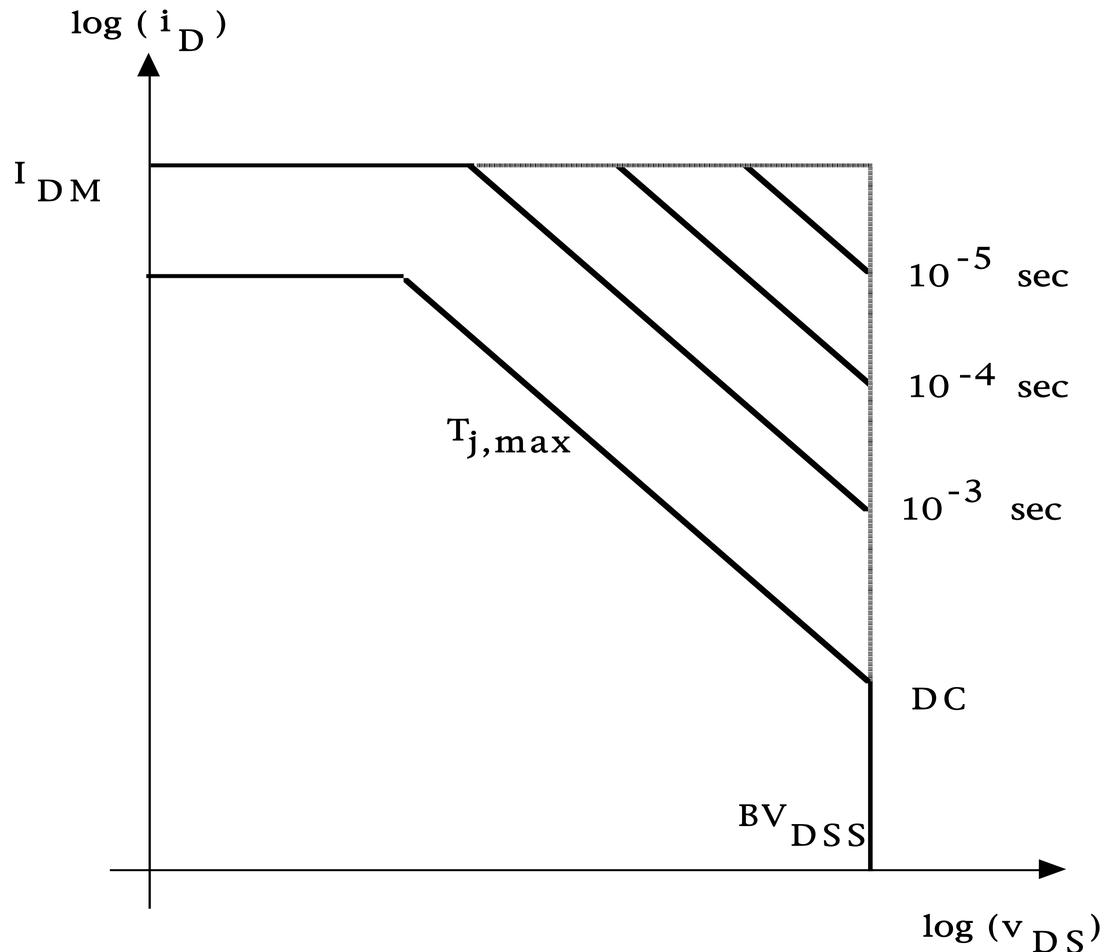
MOSFET Safe Operating Area (SOA)



- No distinction between FBSOA and RBSOA. SOA is square.
  - FB = forward bias. $V_{GS} \geq 0$.
  - RB = reverse bias. $V_{GS} \leq 0$.
- No second breakdown.

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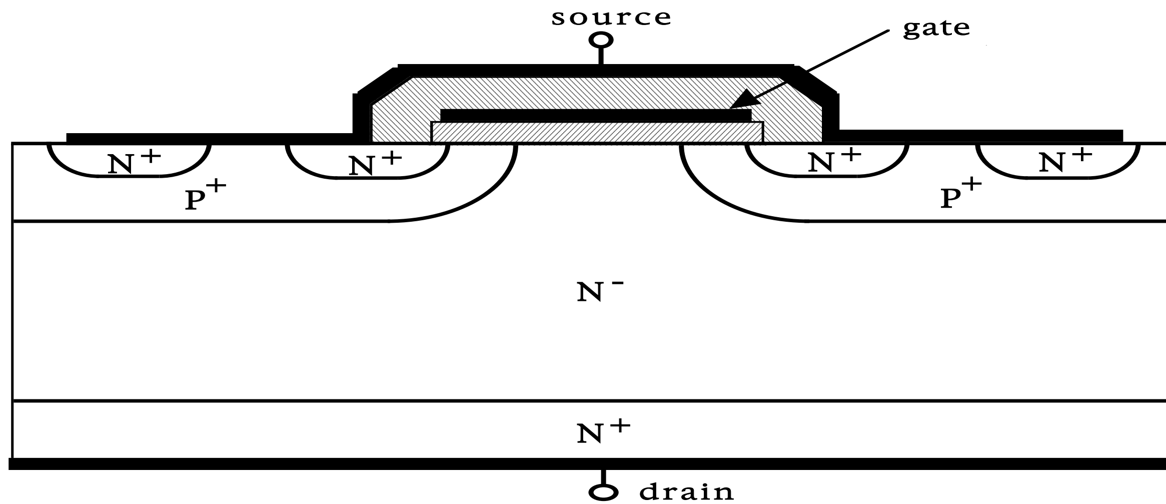
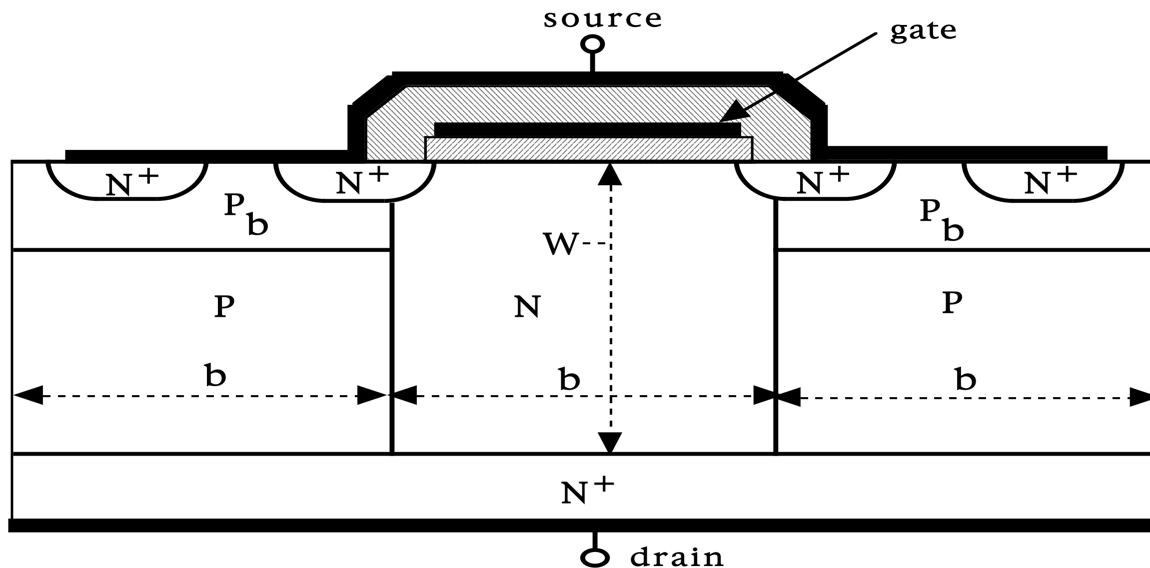
Structural Comparison: VDMOS Versus COOLMOS™



- Conventional vertically oriented power MOSFET



- COOLMOS™ structure (composite buffer structure, super-junction MOSFET, super multi-resurf MOSFET)
- Vertical P and N regions of width b doped at same density ($N_a = N_d$)

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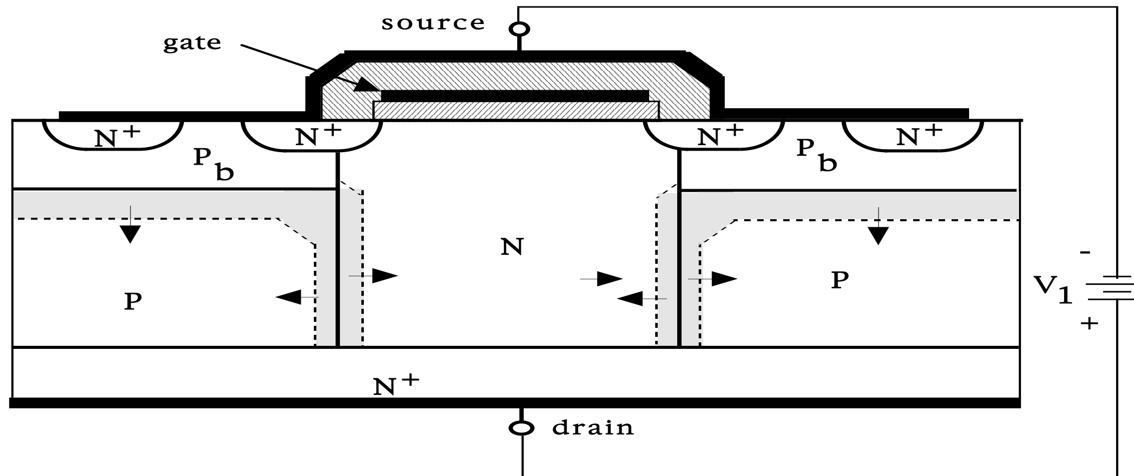
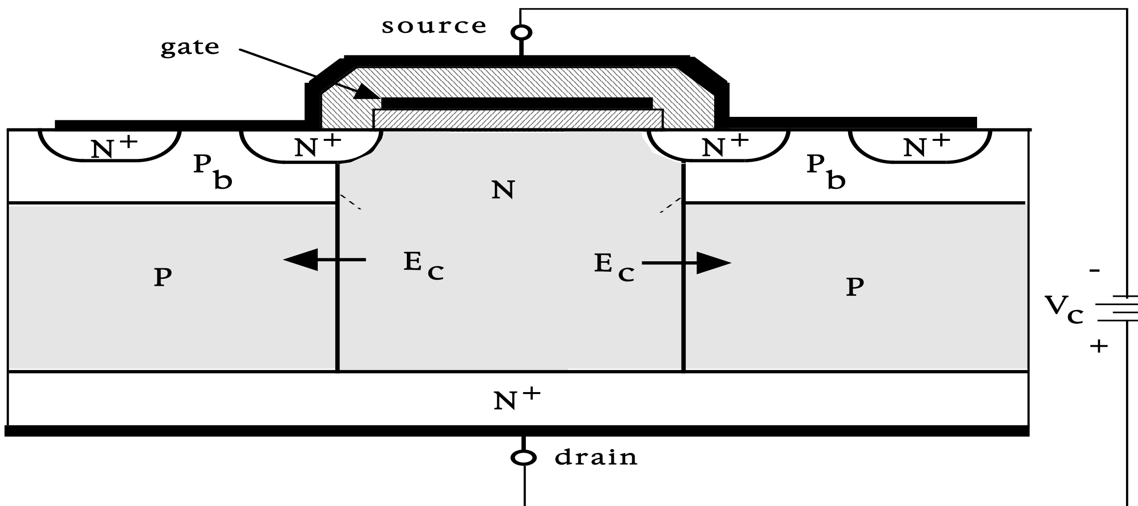
COOLMOS™ Operation in Blocking State



- COOLMOS™ structure partially depleted.
- Arrows indicate direction of depletion layer growth as device turns off.
- Note n-type drift region and adjacent p-type stripes deplete uniformly along entire vertical length.



- COOLMOS™ structure at edge of full depletion with applied voltage V_c. Depletion layer reaches to middle of vertical P and N regions at b/2.
- Using step junction formalism, $V_c = (q\, b^2\, N_d)/(4\, \varepsilon) = b\, E_{c,max}/2$
- Keep $E_{c,max} \leq E_{BD}/2$. Thus $N_d \leq (\varepsilon\, E_{BD})/(q\, b)$

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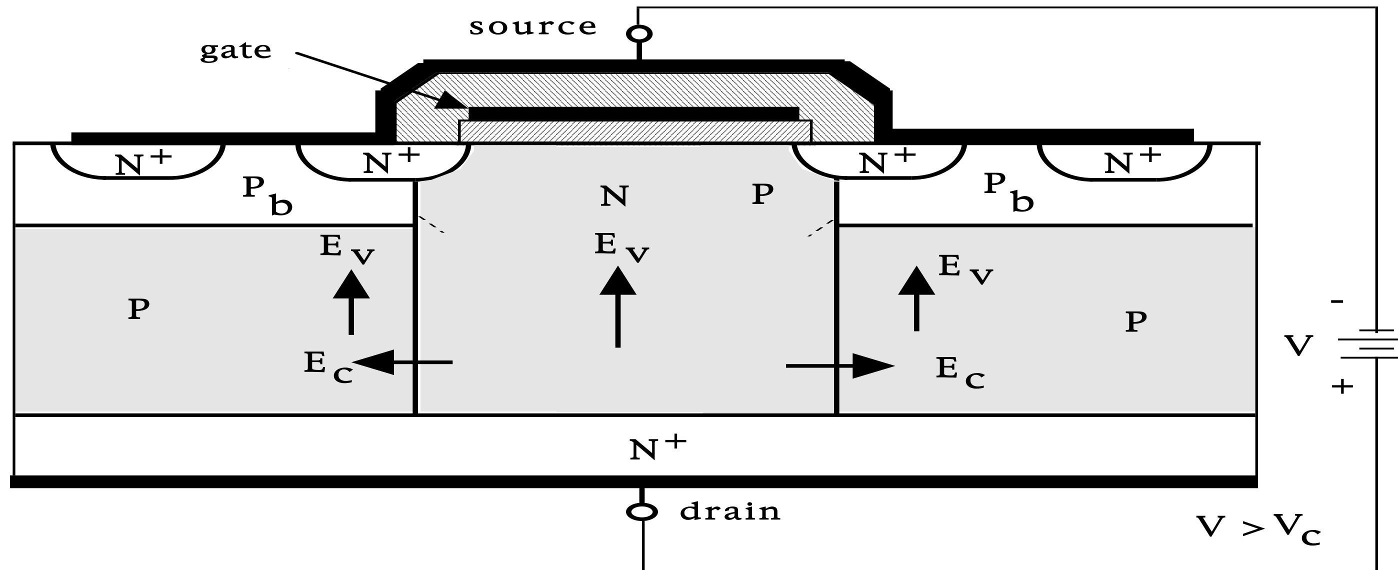
COOLMOS™ Operation in Blocking State (cont.)



- For applied voltages $V > V_c$, vertically oriented electric field E_v begins to grow in depletion region.
- E_v spatially uniform since space charge compensated for by E_c. $E_v \approx V/W$ for $V >> V_c$.
- Doping level N_d in n-type drift region can be much greater than in drift region of conventional VDMOS drift region of similar BV_{BD} capability.
- At breakdown $E_v = E_{BD} \approx 300$ kV/cm ; $V = BV_{BD} = E_{BD}W$

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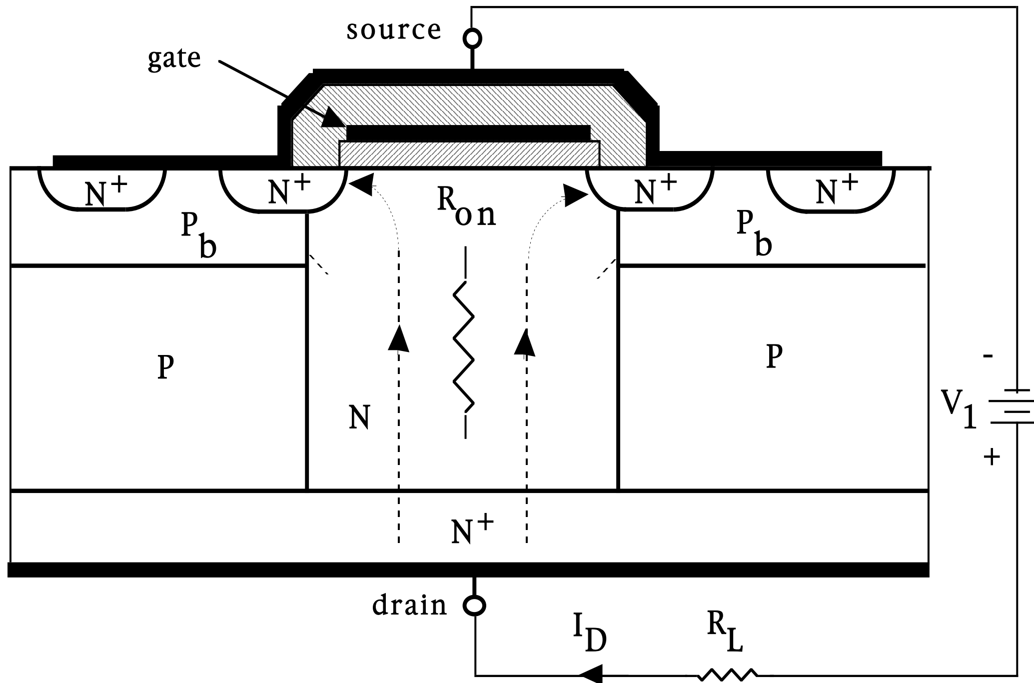
COOLMOS™ Operation in ON-State



- On-state specific resistance AR_{on} [Ω-cm^2] much less than comparable VDMOS because of higher drift region doping.
- COOLMOS™ conduction losses much less than comparable VDMOS.

- $R_{on} A = W/(q\ \mu_n N_d)$; Recall that $N_d = (\varepsilon\ E_{BD})/(q\ b)$
- Breakdown voltage requirements set $W = BV_{BD}/\ E_{BD}$.
- Substituting for W and N_d yields $R_{on} A = (b\ BV_{BD})/(\varepsilon\ \mu_n E_{BD}^2)$

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R_{on} A Comparison: VDMOS versus COOLMOS™

- COOLMOS at BV_{BD} = 1000 V. Assume b ≈ 10 μm. Use E_{BD} = 300 kV/cm.
  - $R_{on}A = (10^{-3}\ cm)(1000\ V)/[\ (9x10^{-14}\ F/cm)(12)(1500\ cm^2\ \text{-V-sec})(300\ kV/cm)^2]$

    $R_{on}A = 0.014\ \Omega\text{-cm}$. Corresponds to $N_d = 4x10^{15}\ cm^{-3}$

- Typical VDMOS, $R_{on}A = 3x10^{-7}\ (BV_{BD})^2$
  - $R_{on}A = 3x10^{-7}\ (1000)^2 = 0.3\ \Omega\text{-cm}$; Corresponding $N_d = 10^{14}\ cm^3$

- Ratio COOLMOS to VDMOS specific resistance = 0.007/0.3 = 0.023 or approximately 1/40
  - At BV_{BD} = 600 V, ratio = 1/26.
  - Experimentally at BV_{BD} = 600 V, ratio is 1/5.

- For more complete analysis see: Antonio G.M. Strollo and Ettore Napoli, "Optimal ON-Resistance Versus Breakdown Voltage Tradeoff in Superjunction Power Device: A Novel Analytical Model", IEEE Trans. On Electron Devices,Vol. 48, No. 9, pp 2161-2167, (Sept., 2001)

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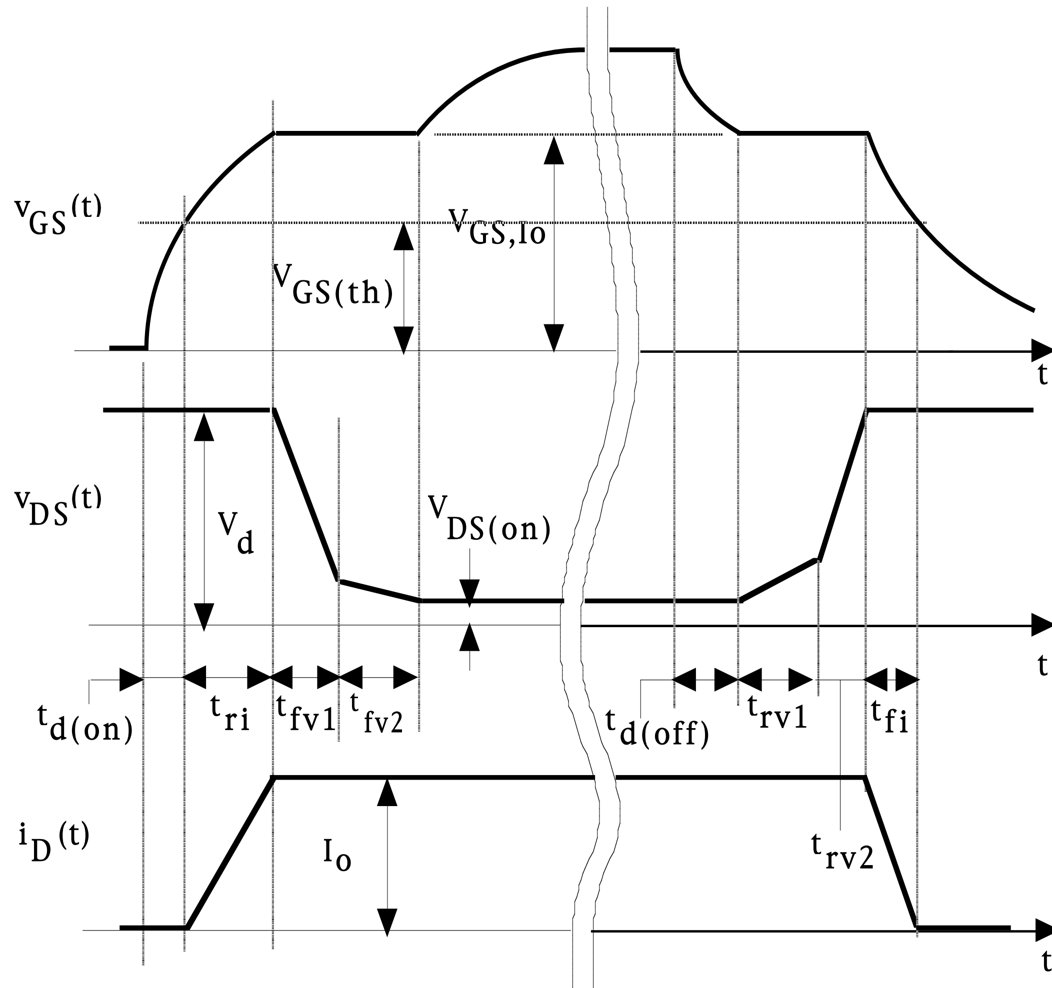
COOLMOS™ Switching Behavior

- MOSFET witching waveforms for clamped inductive load.



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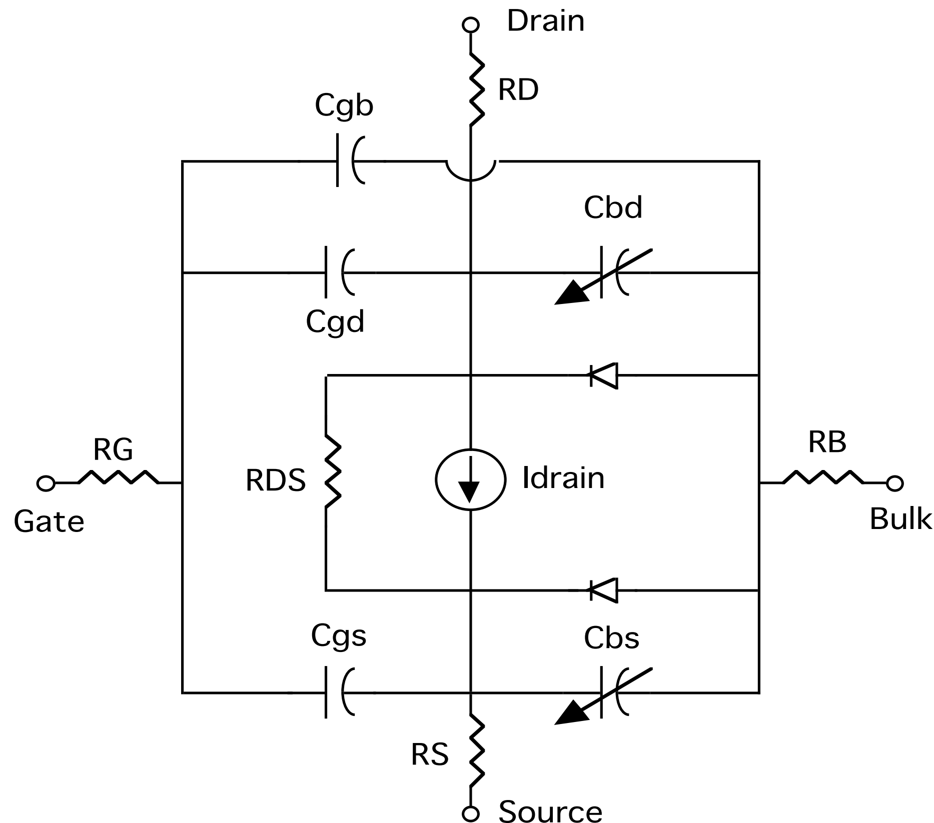
- Larger blocking voltages V_{ds} > depletion voltage V_c, COOLMOS has smaller C_{gs}, C_{gd}, and C_{ds} than comparable (same R_{on} and BV_{DSS}) VDMOS.
- Small blocking voltages V_{ds} < depletion voltage V_c, COOLMOS has larger C_{gs}, C_{gd}, and C_{ds} than comparable (same R_{on} and BV_{DSS}) VDMOS.
- Effect on COOLMOS switching times relative to VDMOS switching times.
  - Turn-on delay time - shorter
  - Current rise time - shorter
  - Voltage fall time1 - shorter
  - Voltage fall time2 - longer
  - Turn-off delay time - longer
  - Voltage rise time1 - longer
  - Voltage rise time2 - shorter
  - Current fall time - shorter

PSPICE Built-in MOSFET Model



Circuit components

- RG, RDS, RS, RB, and RD = parasitic ohmic resistances
- Cgs Cgd, and Cgb = constant voltage-independent capacitors
- Cbs and Cbd = nonlinear voltage-dependent capacitors (depletion layer capacitances)
- Idrain = f(Vgs, Vds) accounts for dc characteristics of MOSFET
- Model developed for lateral (signal level) MOSFETs

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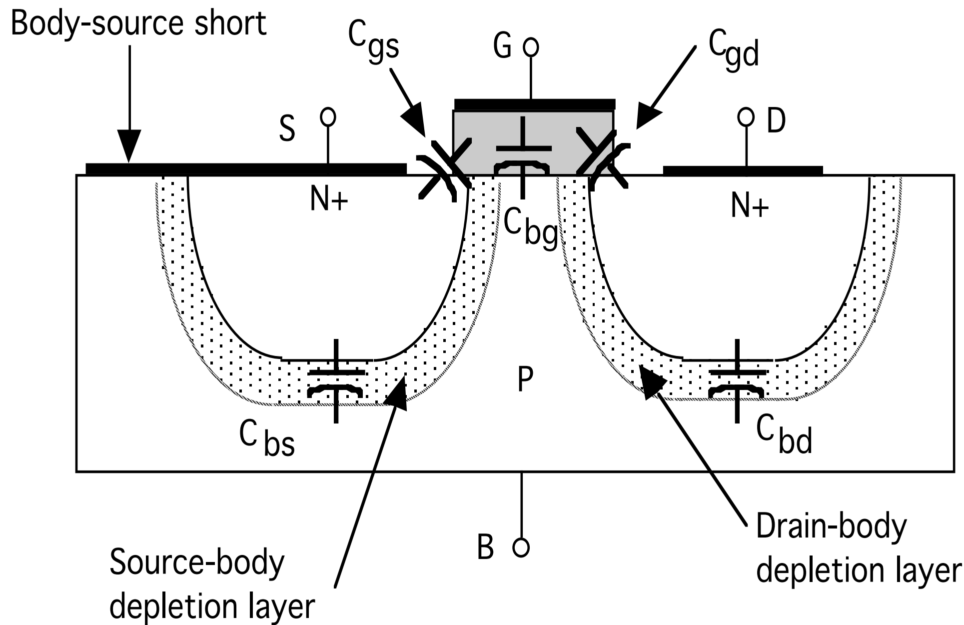
Lateral (Signal level) MOSFET



- C_{gs}, C_{bg}, C_{gd} due to electrostatic capacitance of gate oxide. Independent of applied voltage
- C_{bs} and C_{bd} due to depletion layers. Capacitance varies with junction voltage.

- Body-source short keeps C_{bs} constant.
- Body-source short puts C_{bd} between drain and source.
- Variations in drain-source voltage relatively small, so changes in C_{bd} also relatively small.
- Capacitances relatively independent of terminal voltages
- Consequently PSPICE MOSFET model has voltage-independent capacitances.

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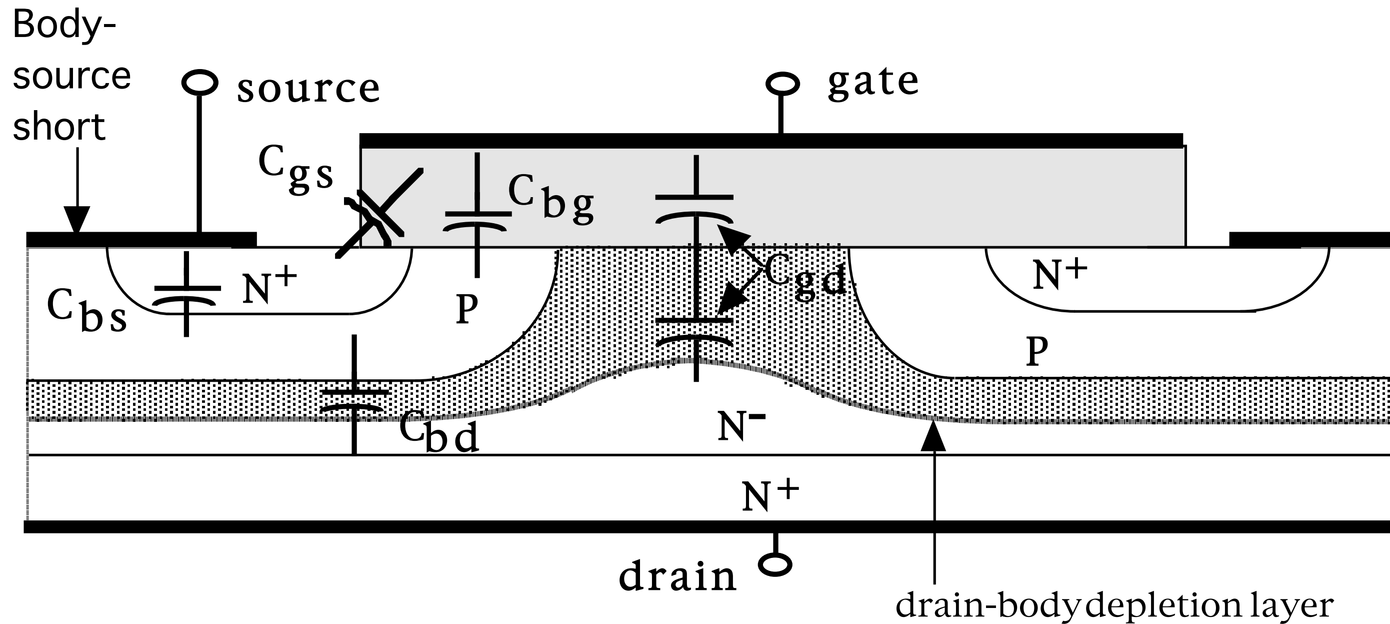
Vertical Power MOSFET



- Drain-drift region and large drain-source voltage variations cause large variations in drain-body depletion layer thickness
  - Large changes in C_{gd} with changes in drain-source voltage. 10 to 100:1 changes in C_{gd} measured in high voltage MOSFETs.
  - Moderate changes in C_{gb} and C_{bs}.

- MOSFET circuit simulation models must take this variation into account.

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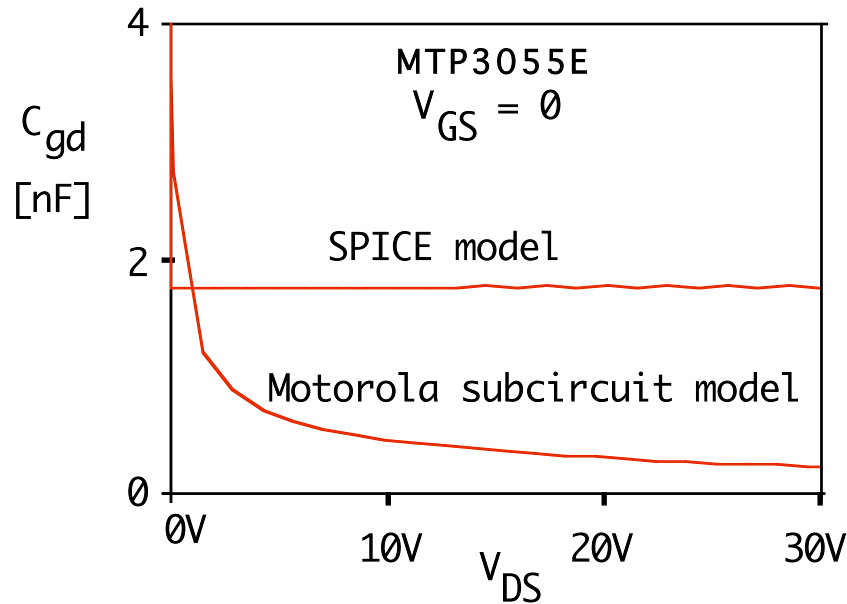
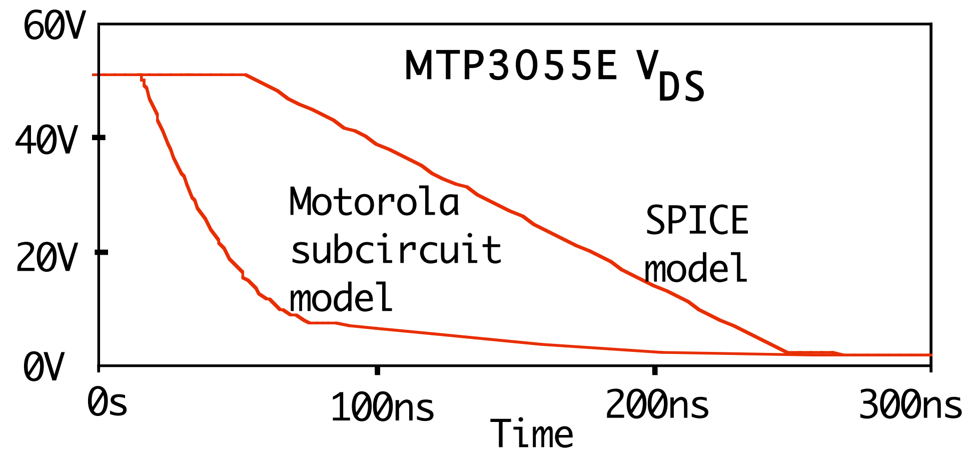
Inadequacies of PSPICE MOSFET Model



- C_{gs} and C_{gd} in PSPICE model are constant independent of terminal voltages
- In vertical power MOSFETs, C_{gd} varies substantially with terminal voltages.



- Comparison of transient response of drain-source voltage using PSPICE model and an improved subcircuit model. Both models used in same step-down converter circuit.

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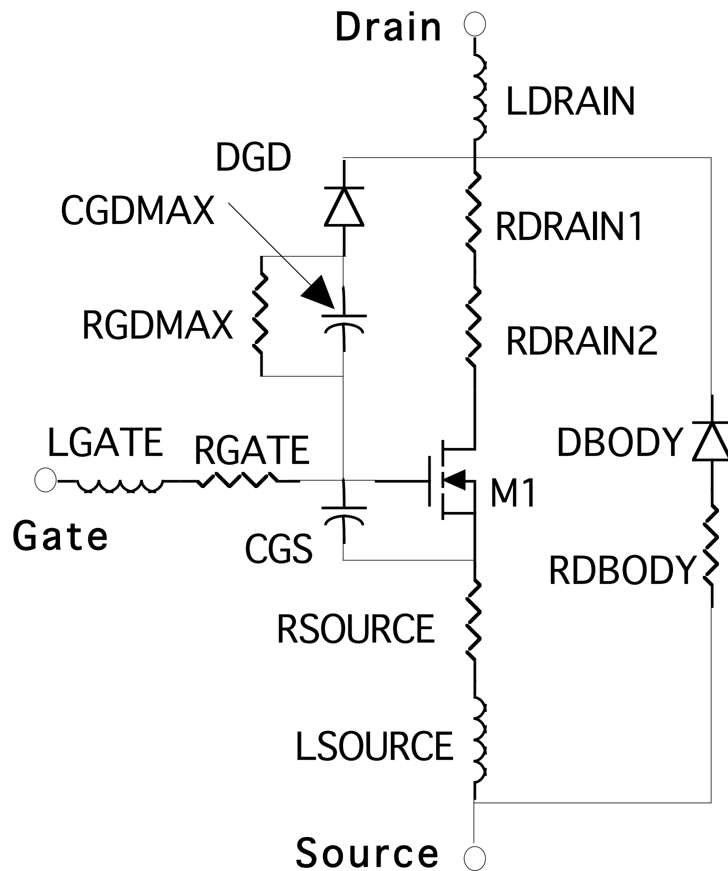
Example of an Improved MOSFET Model



- Developed by Motorola for their TMOS line of power MOSFETs
- M1 uses built-in PSPICE models to describe dc MOSFET characteristics. Space charge capacitances of intrinsic model set to zero.
- Space charge capacitance of DGD models voltage-dependent gate-drain capacitance.
- CGDMAX insures that gate-drain capacitance does not get unrealistically large at very low drain voltages.
- DBODY models built-in anti-parallel diode inherent in the MOSFET structure.
- CGS models gate-source capacitance of MOSFET. Voltage dependence of this capacitance ignored in this model.
- Resistances and inductances model parasitic components due to packaging.
- Many other models described in literature. Too numerous to list here.

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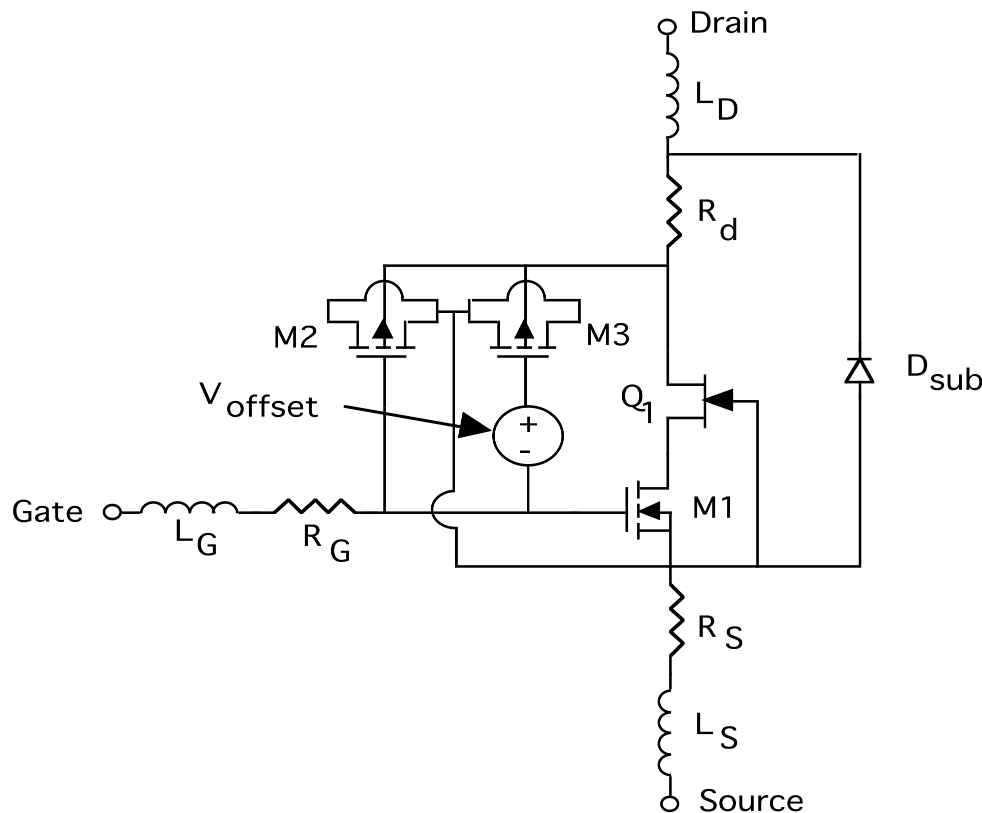
Another Improved MOSFET Simulation Model



- L_G, R_G, L_S R_S, L_D, R_D - parasitic inductances and resistances
- M1= intrinsic SPICE level 2 MOSFET with no parasitic resistances or capacitances.

- M2 and M3 are SPICE level 2 MOSFETs used along with V_{offset} to model voltage dependent behavior of C_{gd}.
- JFET Q_1 and R_d account for voltage drop in N^- drain drift region
- D_{sub} is built-in SPICE diode model used to account for parasitic anti-parallel diode in MOSFET structure.
- Reference - "An Accurate Model for Power DMOSFETs Including Inter-electrode Capacitances", Robert Scott, Gerhard A. Frantz, and Jennifer L. Johnson, IEEE Trans. on Power Electronics, Vol. 6, No. 2, pp. 192-198, (April, 1991)

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Lecture Notes

Thyristors (SCRs)

OUTLINE

- SCR construction and I-V characteristics.
- Physical operation of SCRs.
- Switching behavior of SCRs
- dv/dt and di/dt limitations and methods of improving them.
- SCR drive circuit considerations.

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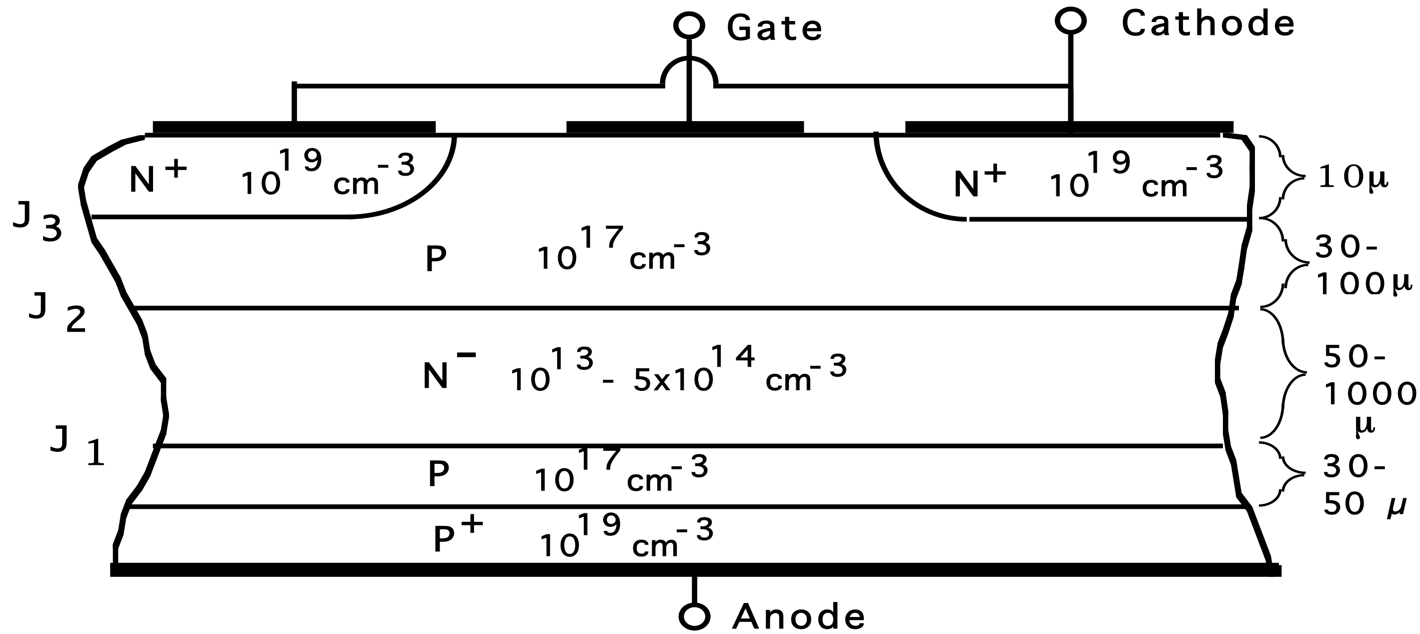
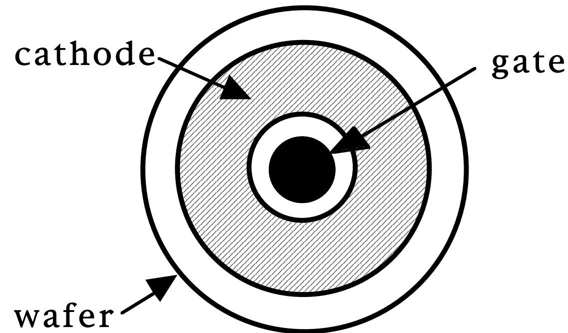
Thyristor (SCR) Geometry

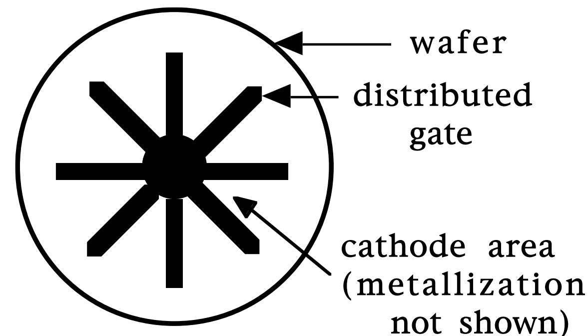


- Cross-sectional view showing vertical orientation of SCR.
- SCRs with kiloamp ratings have diameters of 10 cm or greater.

Gate and cathode metallization for slow (phase control) thyristor.



Gate and cathode metallization for fast (inverter grade) SCR



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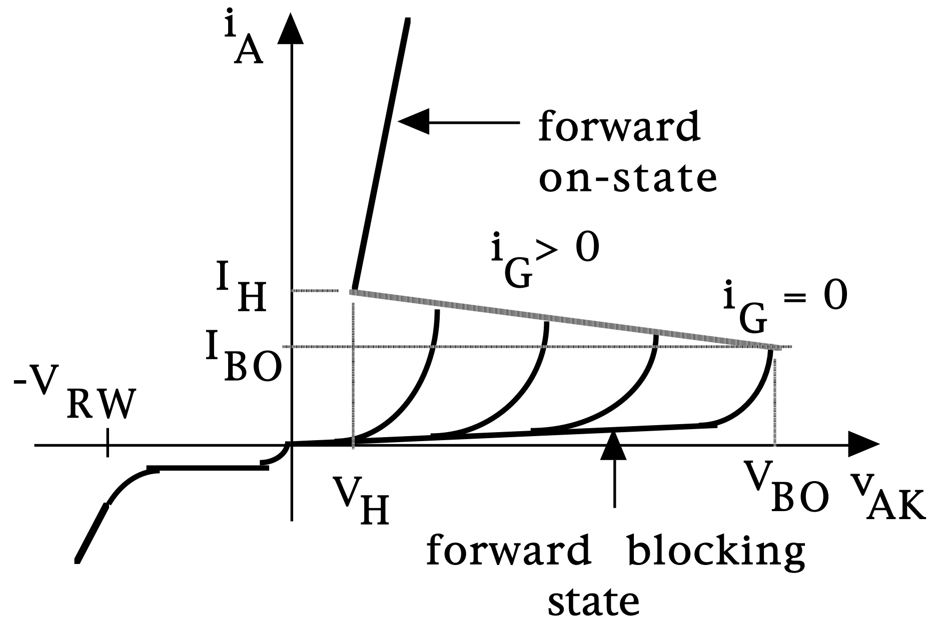
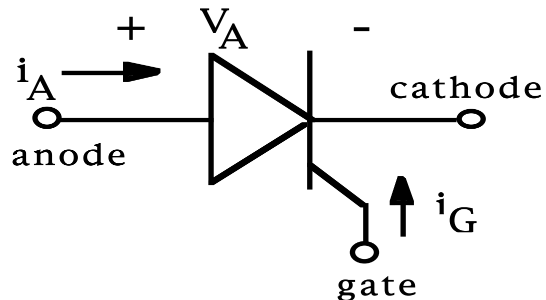
Thyristor I-V Characteristics



Thyristor circuit symbol.



- SCR triggerable from forward blocking state to on-state by a gate current pulse.
- Thyristor latches on and gate cannot turn it off. External circuit must force SCR off.
- Current to several kiloamps for V(on) of 2-4 volts.
- Blocking voltages to 5-8 kilovolts.
- V_{BO} = breakover voltage ; I_{BO} = breakover current
- V_H = holding voltage I_H = holding current
- Maximum junction temperature = 125 C - limited by temperature dependence of V_{BO}.

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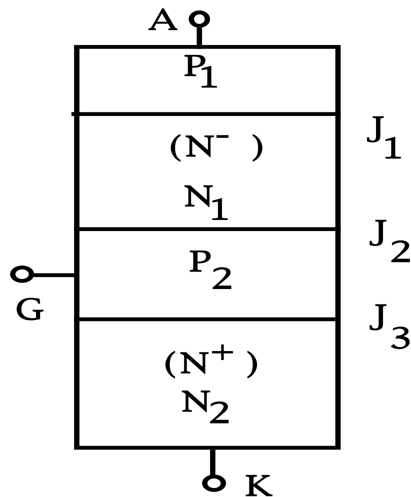
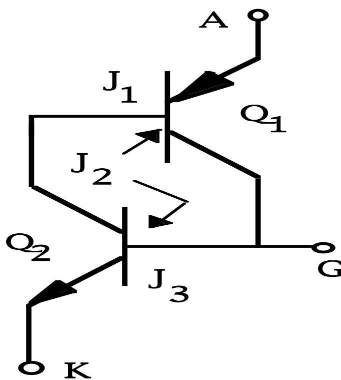
SCR Model and Equivalent Circuit

One dimensional SCR model.



Two transistor equivalent circuit



- BJTs in equivalent circuit in active region.
- Use Ebers-Moll equations for BJTs
- $I_{C1} = -\alpha_1 I_{E1} + I_{CO1}$; $I_{C2} = -\alpha_2 I_{E2} + I_{CO}$
- $I_A = I_{E1}$; $I_K = -I_{E2} = I_A + I_G$
- $I_{C1} + I_{B1} + I_{E1} = 0$
- $I_A = \dfrac{\alpha I_G + I_{CO1} + I_{CO2}}{1 - \alpha_1 - \alpha_2}$
- Blocking state $\alpha_1 + \alpha_2 << 1$
- At breakover $\alpha_1 + \alpha_2 \approx 1$

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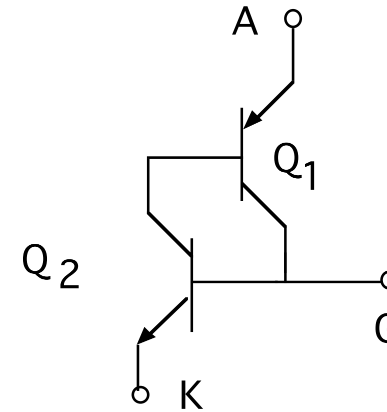
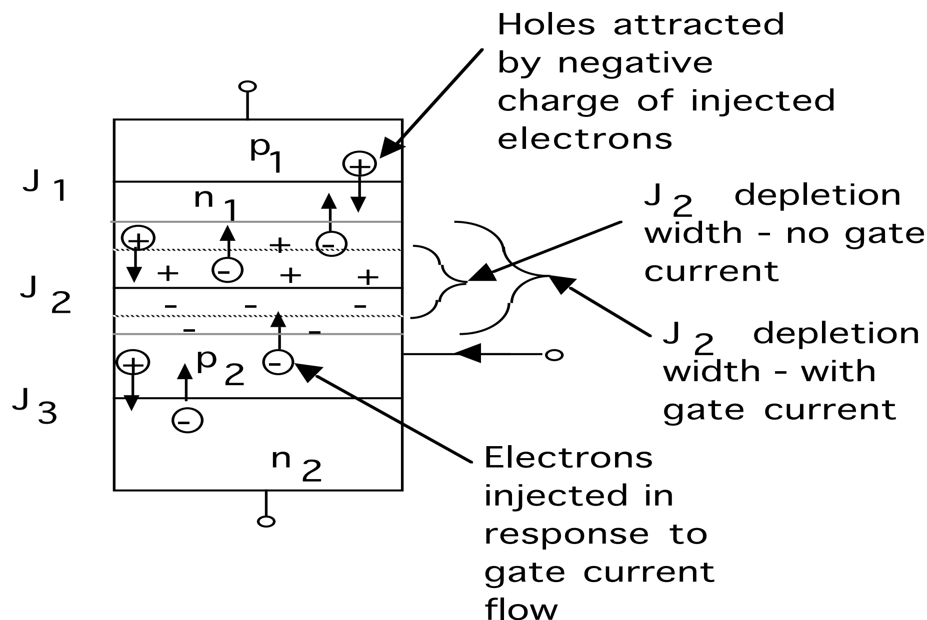
Thyristor Turn-on Process

- In forward blocking state, both BJTs active.
- If $\alpha_1 + \alpha_2 < 1$, connection is stable.
- If $V_{AK} = V_{BO}$ or if positive gate current pulse is applied $\alpha_1 + \alpha_2$ becomes equal to unity and circuit connection becomes unstable and SCR switches on.





- Negative charge of electrons swept into n_1 layer partially compensate positive charge of ionized donors exposed by growth of depletion of junction J_2.
- Growth of depletion reduces width of bases of Q_{npn} and Q_{pnp} and thus increases α_1 and α_2.
- Holes attracted by first wave of injected elctrons attract additional electrons and so on - regenerative action.

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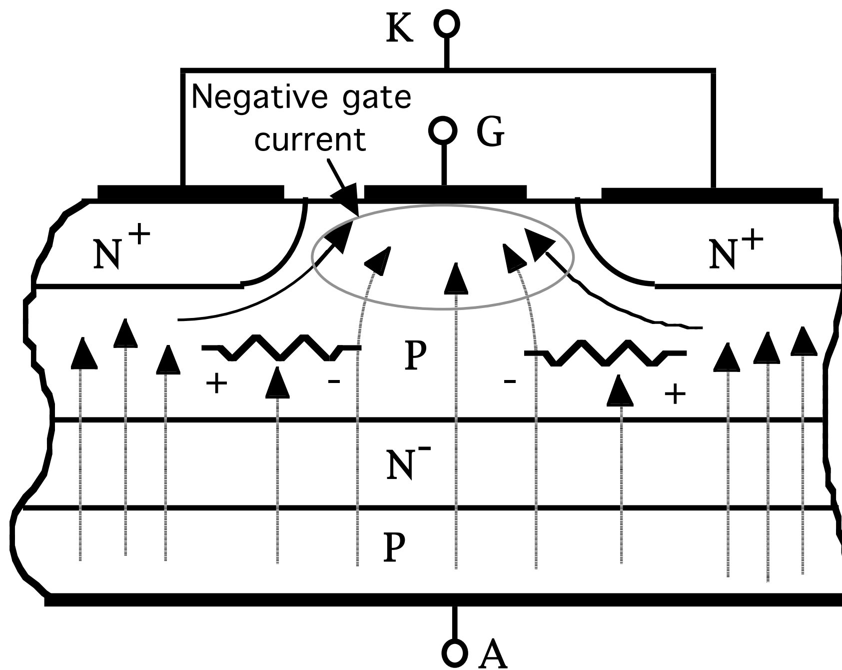
Thyristor On-state Latchup

SCR with negative gate current



- Negative gate current causes lateral voltage drops as indicated which lead to current crowding in center of cathode.
- Conventional SCRs (phase control) have large area cathodes - negative gate current cannot remove stored charge from center of large cathode area.
- SCR stays latched on in spite of negative gate current.
- External circuit must force anode current to negative values in order that enough stored charge be removed from SCR so that it can turn off.

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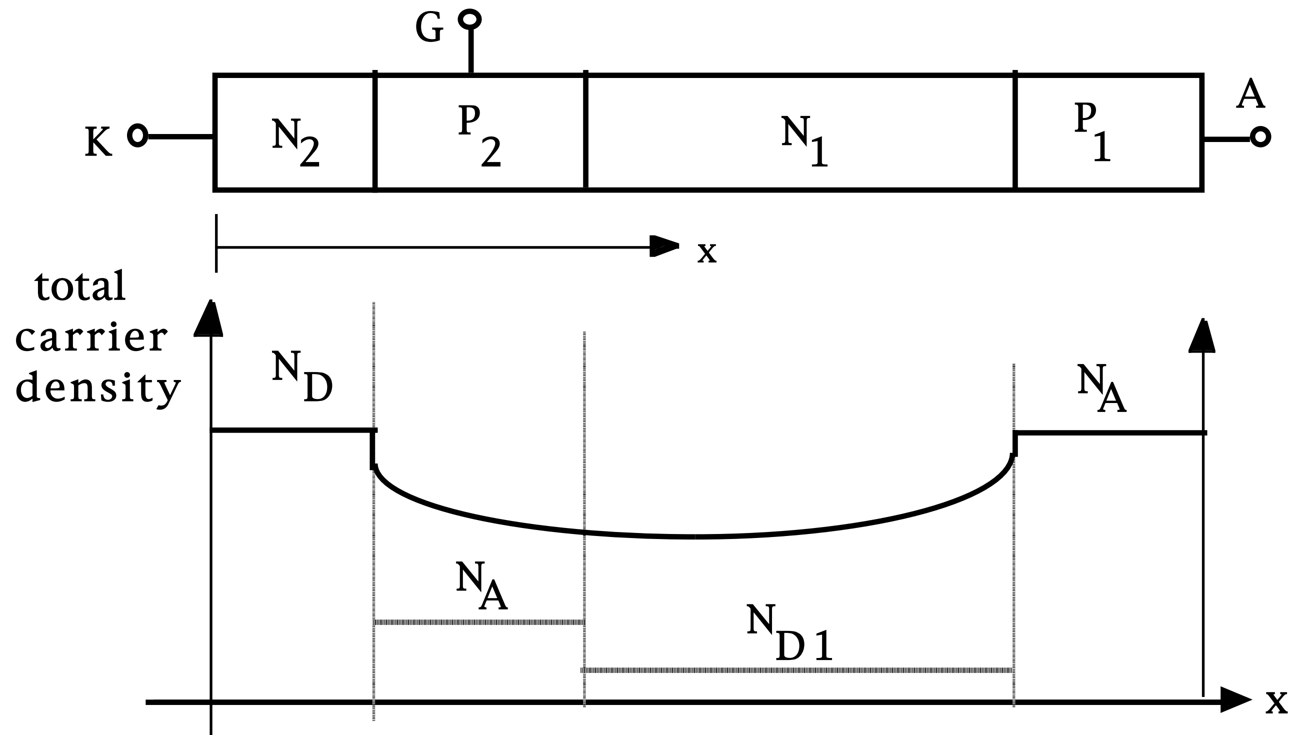
Thyristor On-state Operation



- On-state: all three junctions forward biased and BJTs in equivalent circuit saturated.

- On-state stable because saturated BJTs have $\alpha_1 + \alpha_2 << 1$.

- On-state voltage $V_{AK(on)} = V_{j1} - V_{j2} + V_{j3} + V_n$

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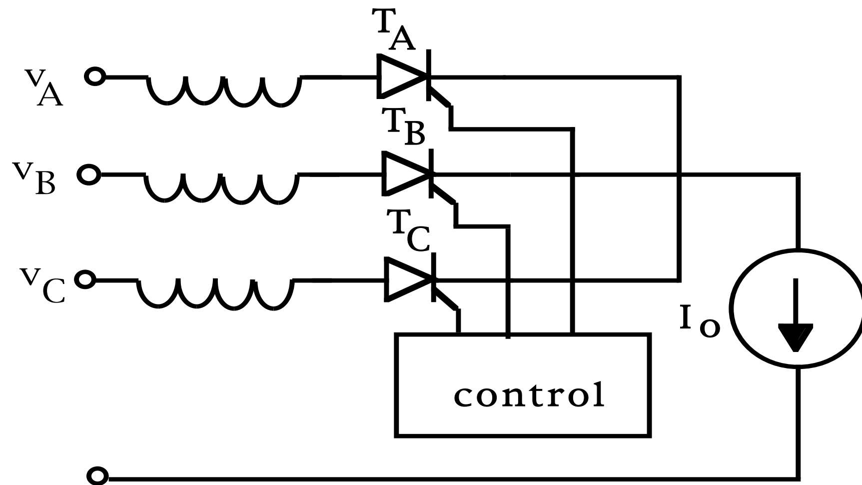
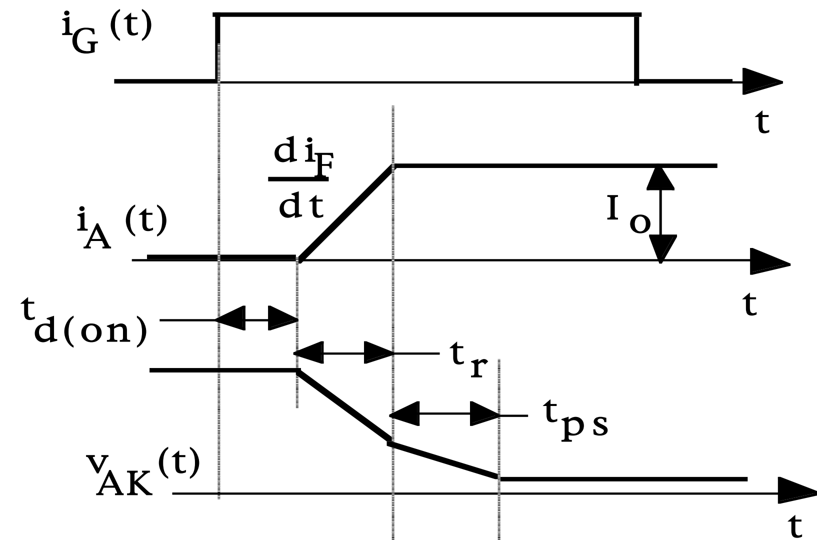
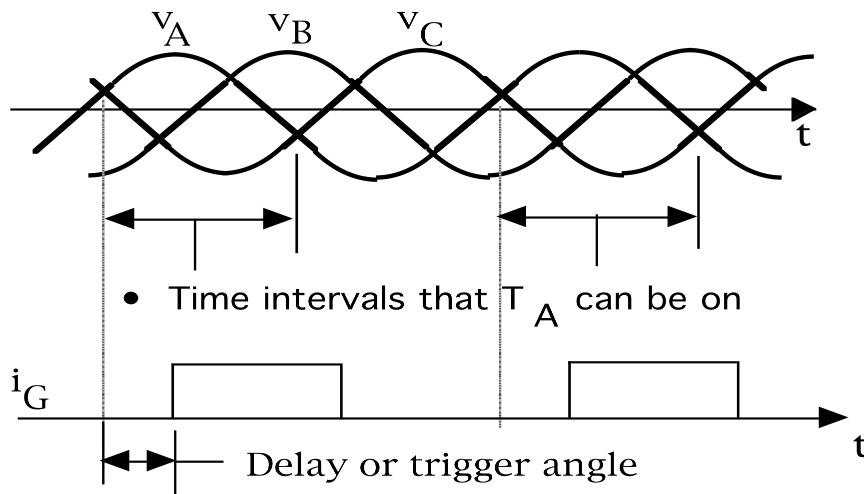
Thyristor Turn-on Behavior







- $t_{d(on)}$ = turn-on delay time; time required for charge injection by gate current to make $\alpha_1 + \alpha_2 = 1$.
- t_r = time required for anode current to reach on-state value. Anode current rate-of-rise di_F/dt limited by external inductance.
- t_{ps} = time required for plasma to spread over whole cathode area from cathode periphery near gate.
- V_{AK} does not attain on-state value until complete area of cathode is conducting.

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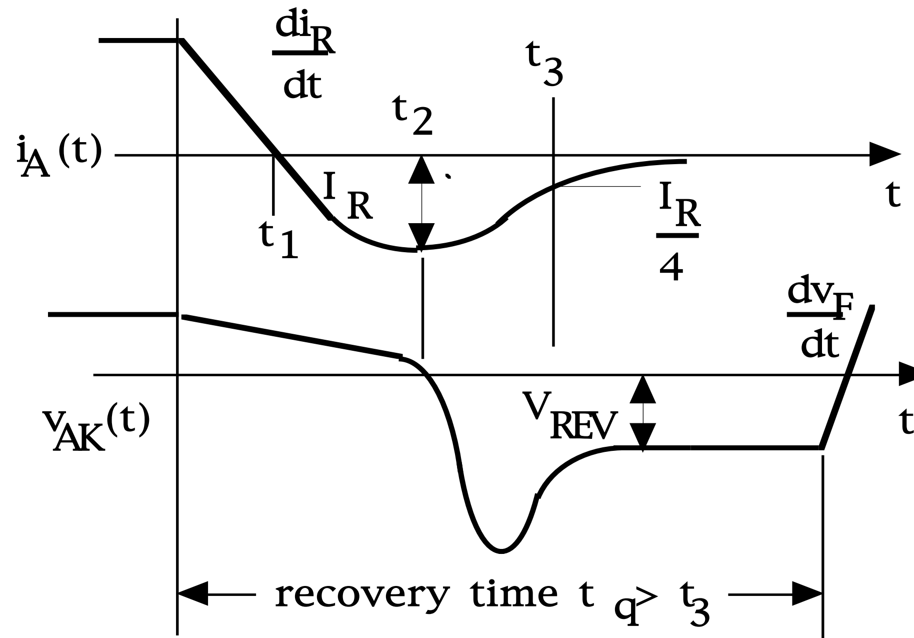
Thyristor Turn-off Behavior



Turn-off waveforms

- SCR turn-off quite similar to power diode turn-off.
- Anode current rate-of-fall controlled by external inductance.
- Reverse voltage overshoot caused by external inductance.
- Junction J_1 is blocking junction in reverse bias. J_3 has low breakdown voltage (20-40 volts) because of the heavy doping on both sides of the junction.

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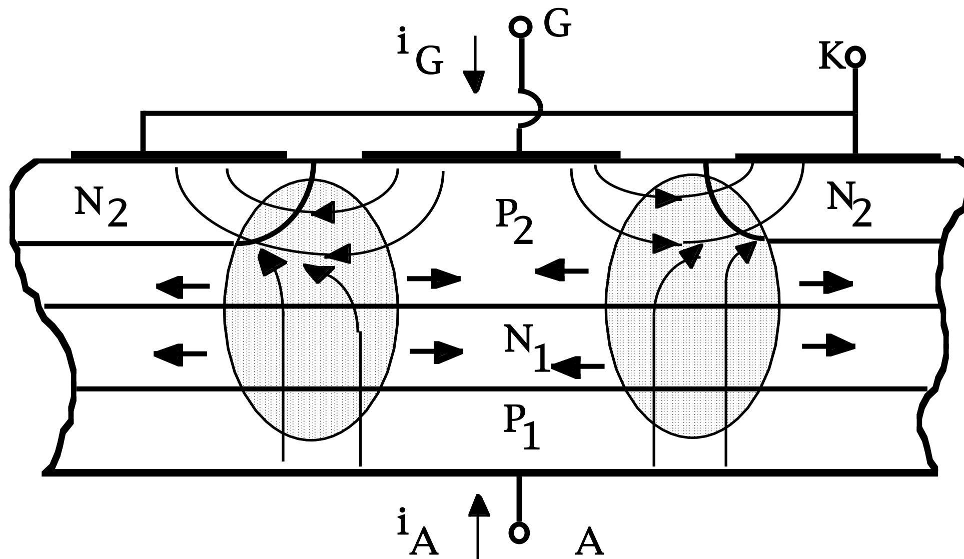
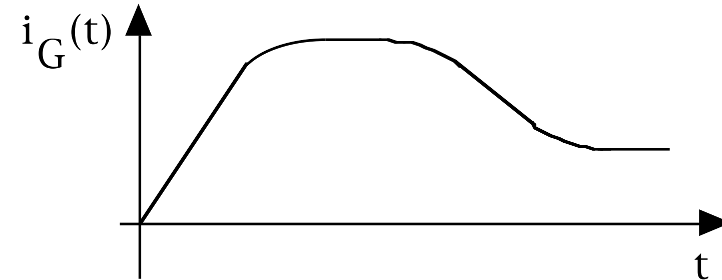
Thyristor di/dt Limit at Turn-on





- SCR first turns on at cathode periphery nearest gate.
- Current constricted to small areas during initial phases of turn-on, $t_{d(on)}$ and t_r.
- If anode current rate-of-rise, di_F/dt, not kept less than some specified maximum, current density in constricted area will be too large.
- Localized power dissipation too high and thermal runaway likely.

- Use shaped gate current pulse for rapid turn-on.

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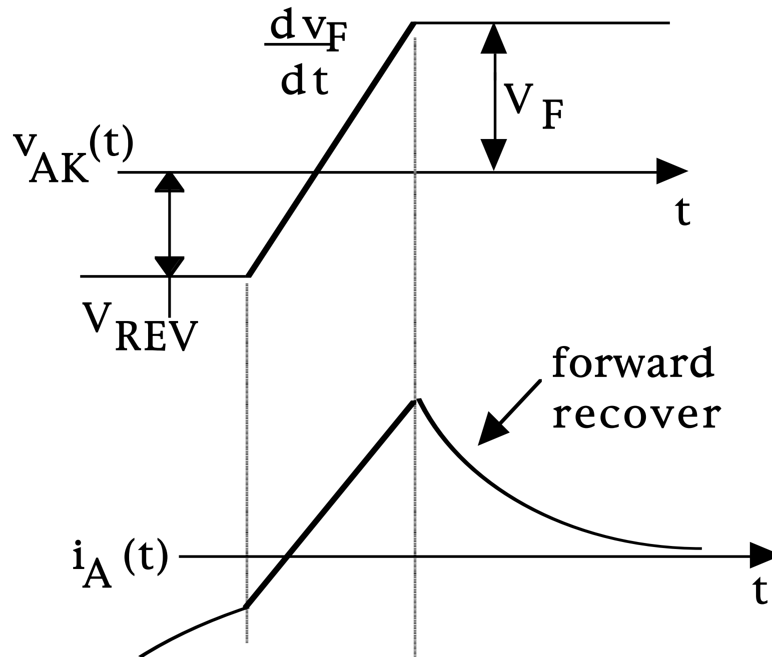
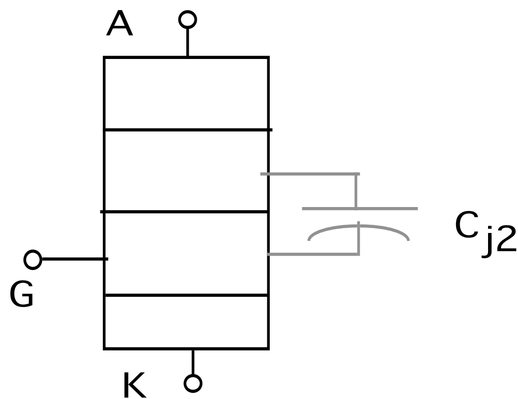
Thyristor Re-applied dv/dt Limits



- Removal of all stored charge in SCR requires a minimum time t_q.
- Application of positive dV_F/dt larger than a specified value before t_q results in a pulse of positive anode current which may produce unintentioned turn-on of the SCR.
- Avoidance of unintentioned turn-on requires $dV_F/dt < dV_{F,max}/dt$ and remaining in reverse bias for a minimum time t_q.



$$\left.\frac{dv_F}{dt}\right|_{max} < \frac{I_{BO}}{C_{j2}}$$

Rate effect

$$100\ \text{V}/\mu\text{s} < \left.\frac{dv_F}{dt}\right|_{max} < 2000\ \text{V}/\mu\text{s}$$

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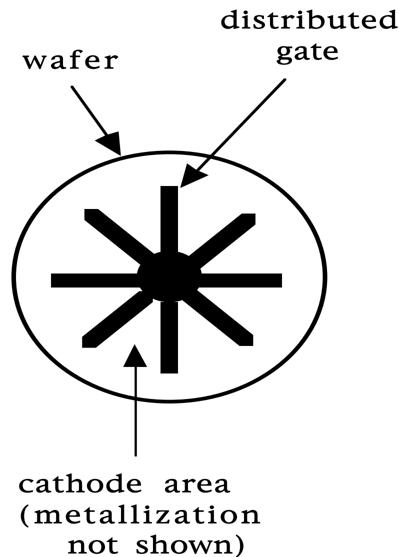
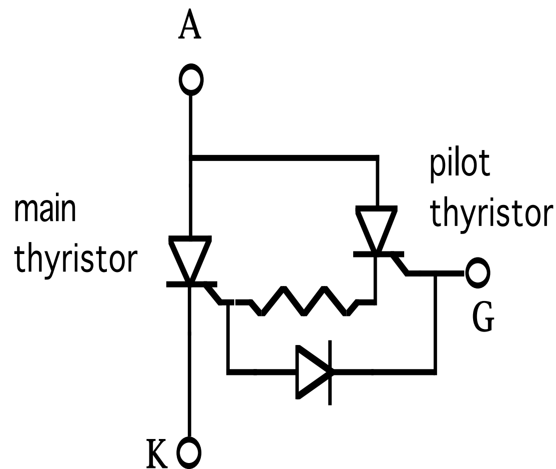
Methods of Improving Thyristor di/dt Rating





- Interdigitated gate-cathode structure used to greatly increase gate-cathode periphery.
- Distance from periphery to center of any cathode region significantly shortened.
- Ability of negative gate current to break latching condition in on-state increased.
- Combination of pilot thyristor, diode, and iterdigitated gate-cathode geometry tgermed a gate-assisted turn-off thyristor or GATT

- Use of pilot thyristor to increase turn-on gate current to main thyristor.
- Larger gate current increases amount of initial conducting area of cathode and thus improves di_F/dt capabiities.
- Diode allowes negative gate current to flow from main SCR.

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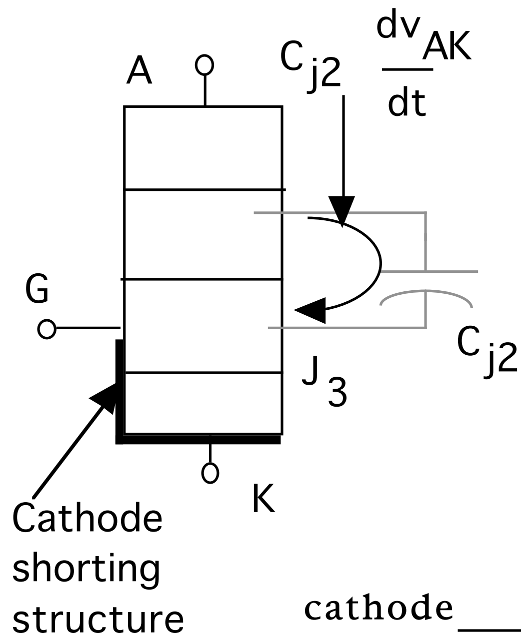
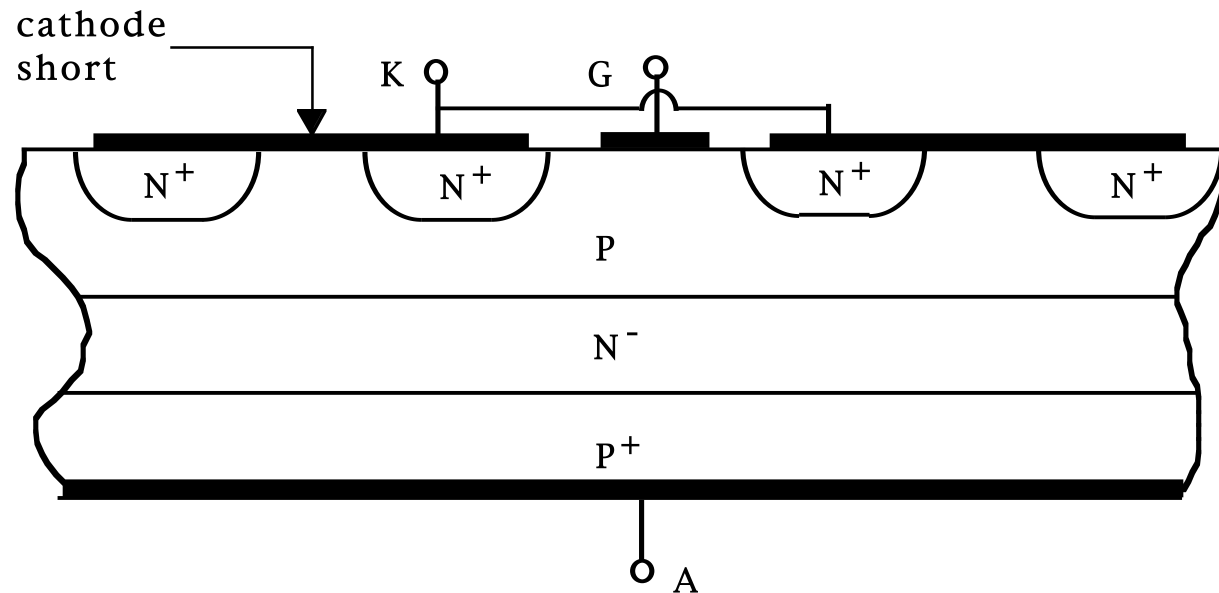
Improvement in dv/dt Rating Via Cathode Shorts



- Current thru C_{j2} indistinguishable from positive gate current with respect to turn-on of SCR.
- If current thru C_{j2} bypasses junction J_3, then SCR will not be turned on by the large displacement currents.
- Cathode shorts provide this desirable bypass. Most effective with interdigitaated gate-cathode geometry.
- $\left.\frac{dV_F}{dt}\right|_{max}$ significantly increased.



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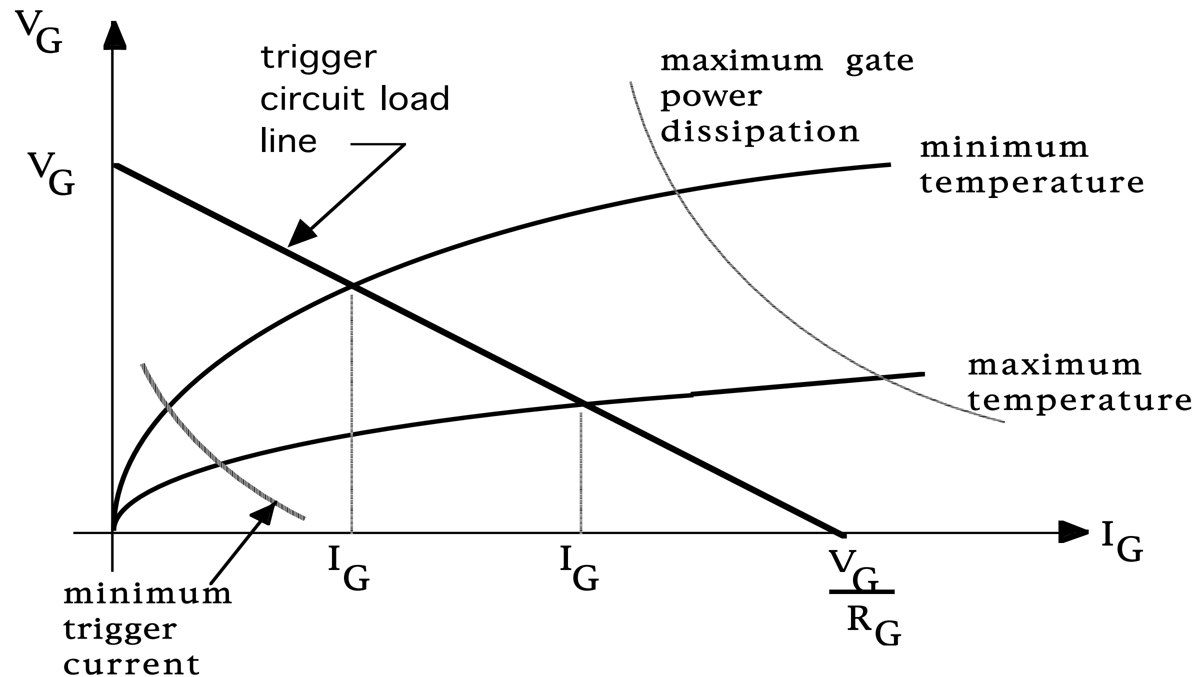
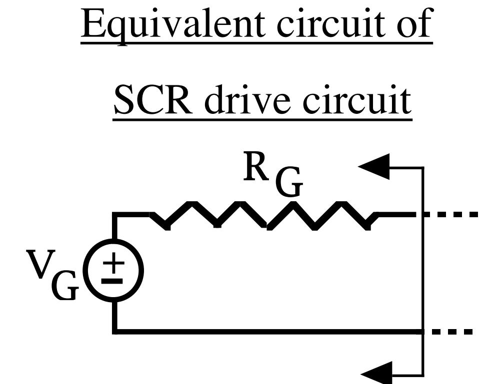
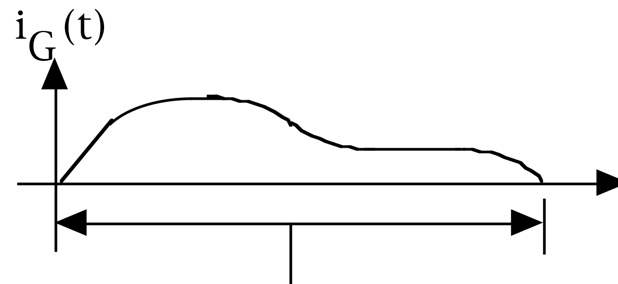
Thyristor Gate Trigger Requirements







Gate current must be on for a specified minimum time interval (few tens of microseconds) to guarantee SCR turn-on

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Lecture Notes

Gate Turn-off Thyristors (GTOS)

OUTLINE

- GTO construction and I-V characteristics.
- Physical operation of GTOs.
- Switching behavior of GTOS

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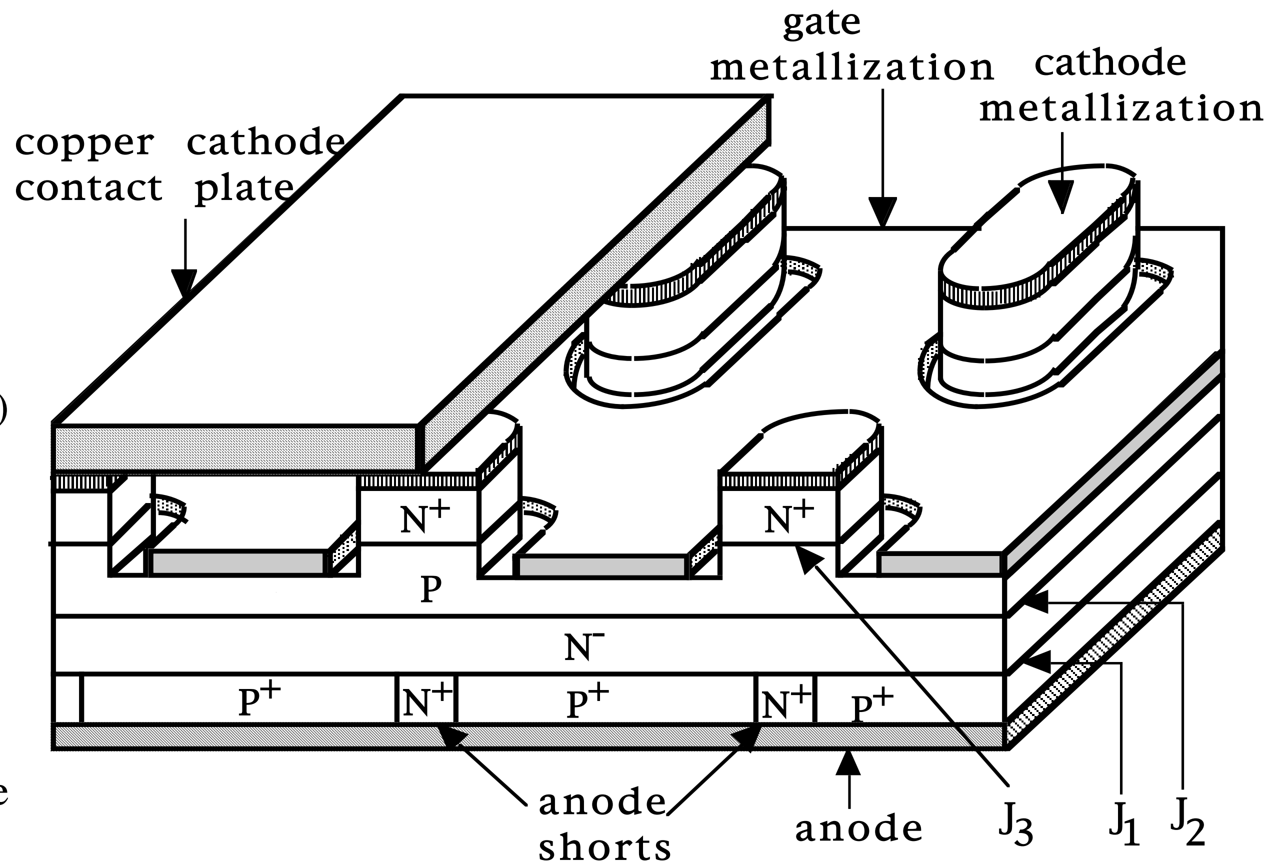
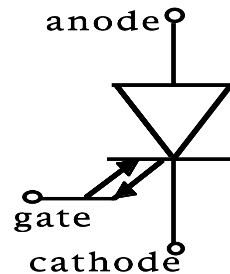
GTO (Gate Turn-off Thyristor) Construction

- Unique features of the GTO.
  - Highly interdigitated gate-cathode structure (faster switching)
  - Etched cathode islands (simplify electrical contacts)
  - Anode shorts (speed up turn-off)
- GTO has no reverse blocking capability because of anode shorts
- Otherwise i-v characteristic the same as for standard SCR



GTO circuit symbol



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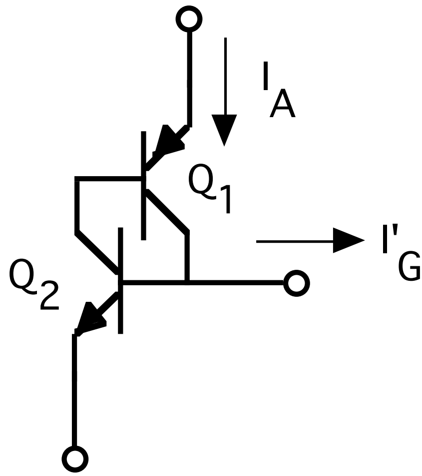
GTO Turn-off Gain



- Turn off GTO by pulling one or both of the BJTs out of saturation and into active region.
- Force Q_2 active by using negative base current I_G' to make $I_{B2} < \frac{I_{C2}}{\beta_2}$
- $I_{B2} = \alpha_1 I_A - I'_G$; $I_{C2} = (1 - \alpha_1) I_A$
- $\alpha_1 I_A - I'_G < \frac{(1 - \alpha_1) I_A}{\beta_2} = \frac{(1 - \alpha_1)(1 - \alpha_2) I_A}{\alpha_2}$
- $I'_G < \frac{I_A}{\beta_{off}}$; $\beta_{off} = \frac{\alpha_2}{(1 - \alpha_1 - \alpha_2)}$ = turn-off gain

- Large turn-off gain requires $\alpha_2 \approx 1$, $\alpha_1 << 1$
- Make α_1 small by
  1. Wide n_1 region (base of Q_1) - also needed for large blocking voltage
  2. Short lifetime in n_1 region to remove excess carriers rapidly so Q_1 can turn off
- Short lifetime causes higher on-state losses
- Anode shorts helps resolve lifetime delimma
  1. Reduce lifetime only moderately to keep on-state losses reasonable
  2. N^+ anode regions provide a sink for excess holes - reduces turn-off time
- Make $\alpha_2 \approx$ unity by making p_2 layer relatively thin and doping in n_2 region heavily (same basic steps used in making beta large in BJTs).
- Use highly interdigitated gate-cathode geometry to minimize cathode current crowding and di/dt limitations.

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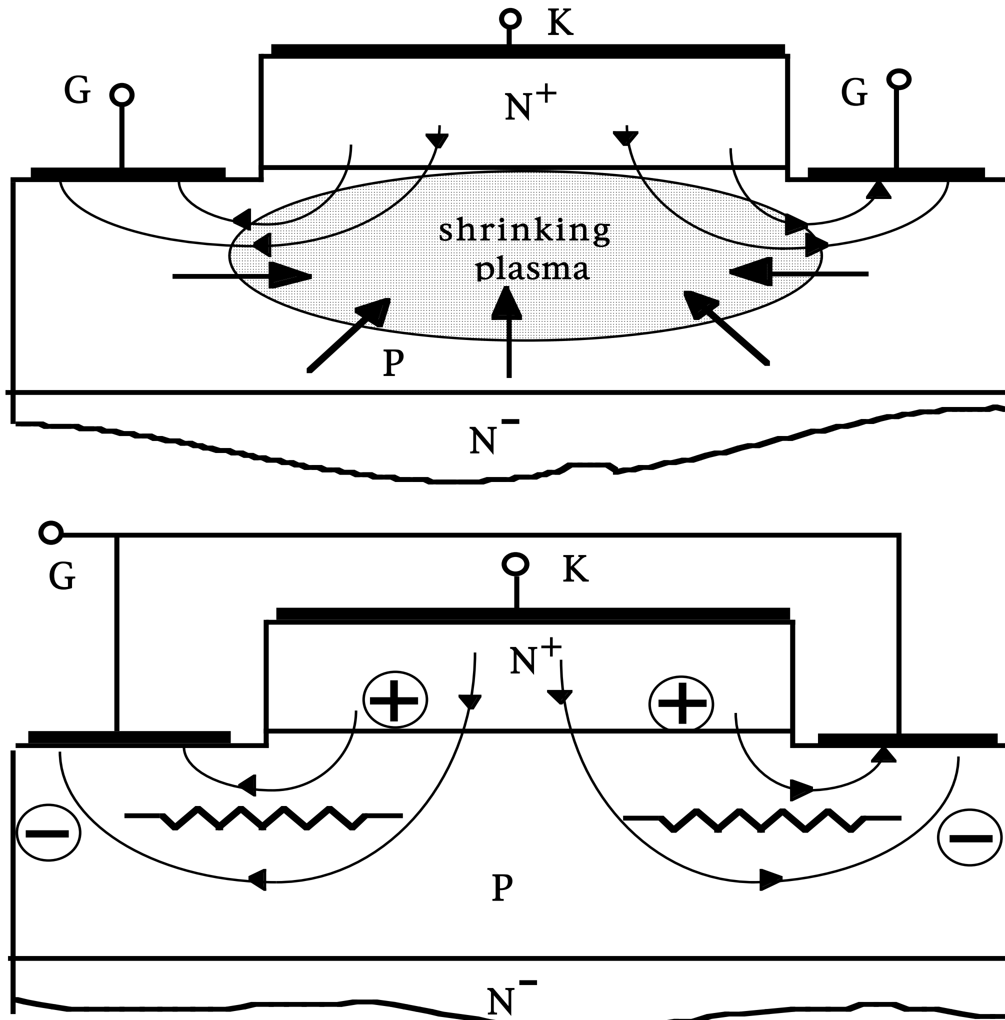
Maximum Controllable Anode Current



- Large negative gate current creates lateral voltage drops which must be kept smaller than breakdown voltage of J_3.

- If J_3 breaks down, it will happen at gate-cathode periphery and all gate current will flow there and not sweep out any excess carriers as required to turn-off GTO.

- Thus keep gate current less than $I_{G,max}$ and so anode current restricted by $I_A < \dfrac{I_{G,max}}{\beta_{off}}$

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GTO Step-down Converter

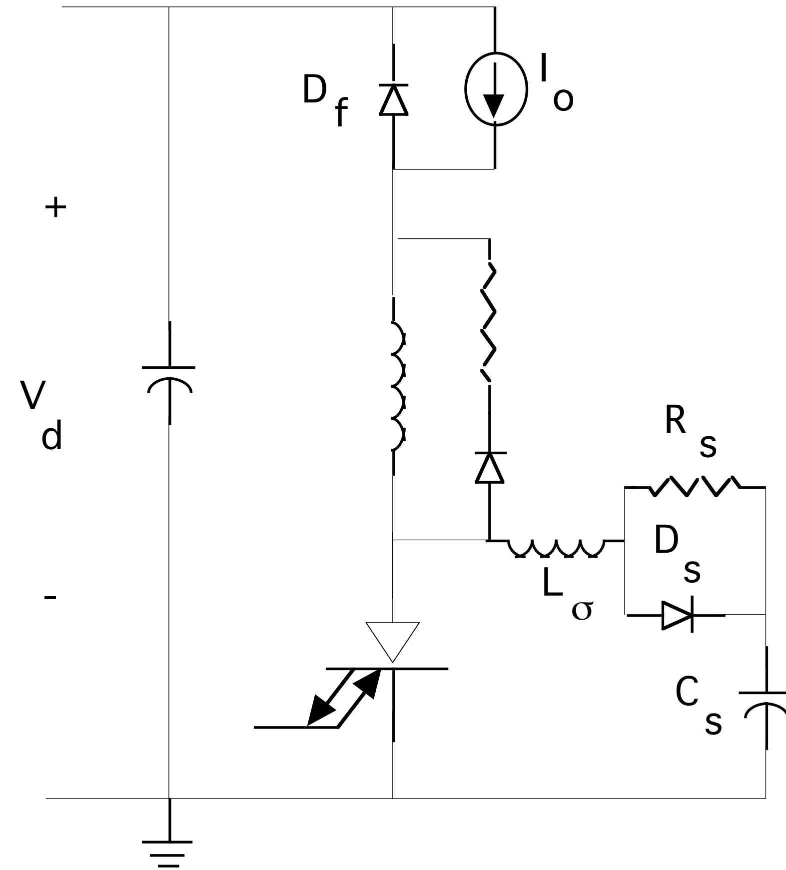
- GTO used in medium-to-high power applications where electrical stresses are large and where other solid state devices used with GTOs are slow e.g. free-wheeling diode D_F.

- GTO almost always used with turn-on and turn-off snubbers.

  1. Turn-on snubber to limit overcurrent from D_F reverse recovery.

  2. Turn-off snubber to limit rate-of-rise of voltage to avoid retriggering the GTO into the on-state.

- Hence should describe transient behavior of GTO in circuit with snubbers.



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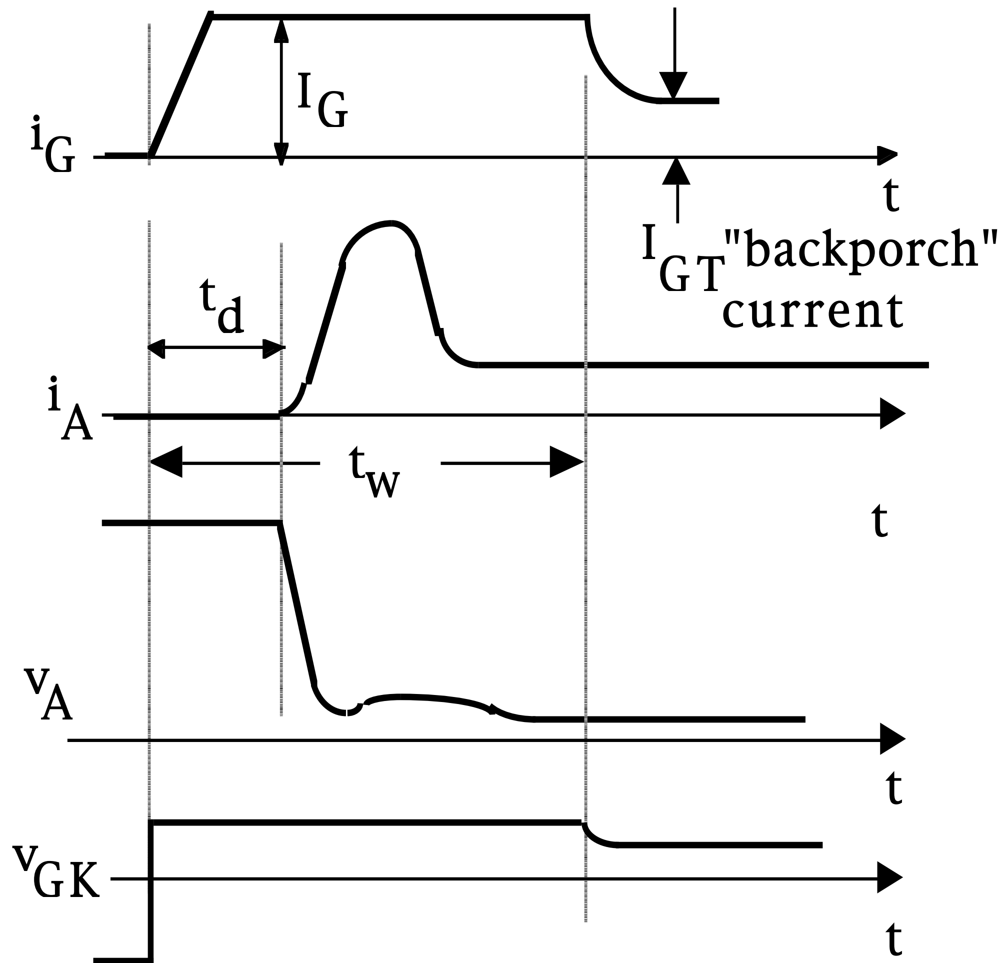
GTO Turn-on Waveforms



- GTO turn on essentially the same as for a standard thyristor
- Large I_{GM} and large rate-of-rise insure all cathode islands turn on together and have good current sharing.
- Backporch current I_{GT} needed to insure all cathode islands stay in conduction during entire on-time interval.
- Anode current overshoot caused by free-wheeling diode reverse recovery current.
- Anode-cathode voltage drops precipitiously because of turn-on snubber

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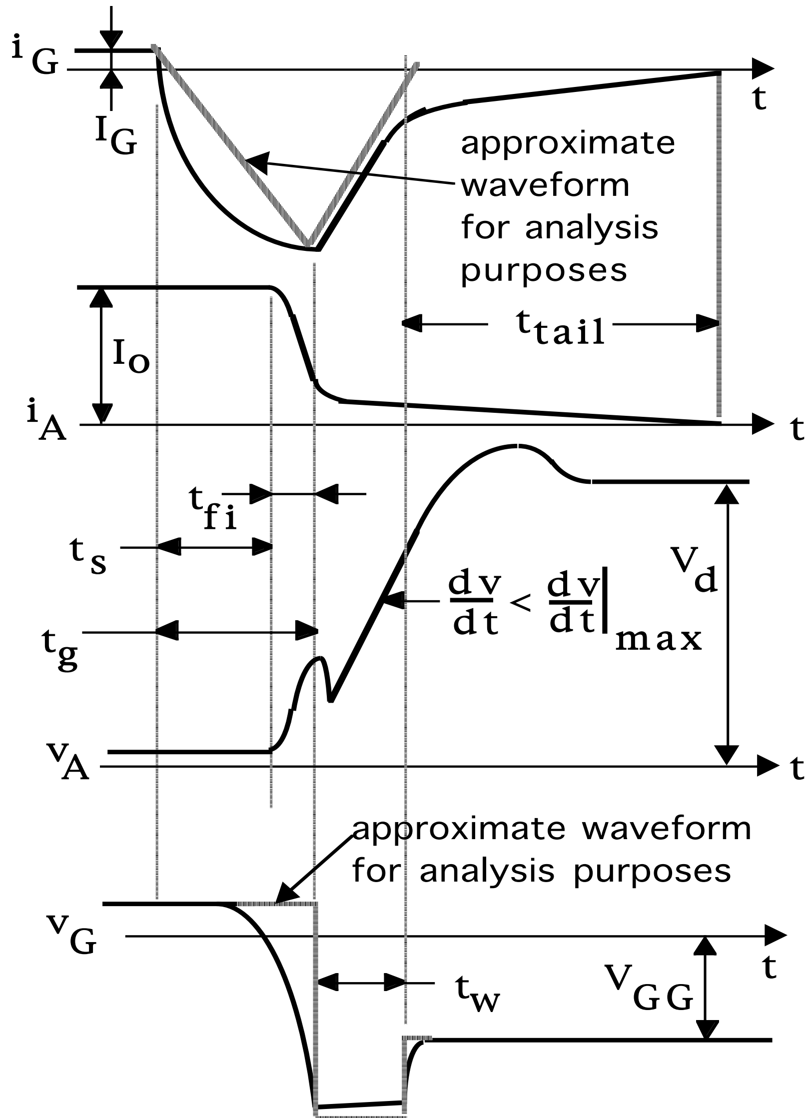
GTO Turn-off Waveforms



- t_s interval

  Time required to remove sufficient stored charge to bring BJTs into active region and break latch condition

- t_{fi} interval

  1. Anode current falls rapidly as load current commutates to turn-off snubber capacitor
  2. Rapid rise in anode-cathode voltage due to stray inductance in turn-off snubber circuit

- t_{w2} interval

  1. Junction J_3 goes into avalanche breakdown because of inductance in trigger circuit. Permits negative gate current to continuing flowing and sweeping out charge from p_2 layer.
  2. Reduction in gate current with time means rate of anode current commutation to snubber capacitor slows. Start of anode current tail.

- t_{tail} interval

  1. Junction J_3 blocking, so anode current = negative gate current. Long tailing time required to remove remaining stored charge.
  2. Anode-cathode voltage growth governed by turn-off snubber.
  3. Most power dissipation occurs during tailing time.

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Lecture Notes

Insulated Gate Bipolar Transistors (IGBTs)

Outline

- Construction and I-V characteristics
- Physical operation
- Switching characteristics
- Limitations and safe operating area
- PSPICE simulation models

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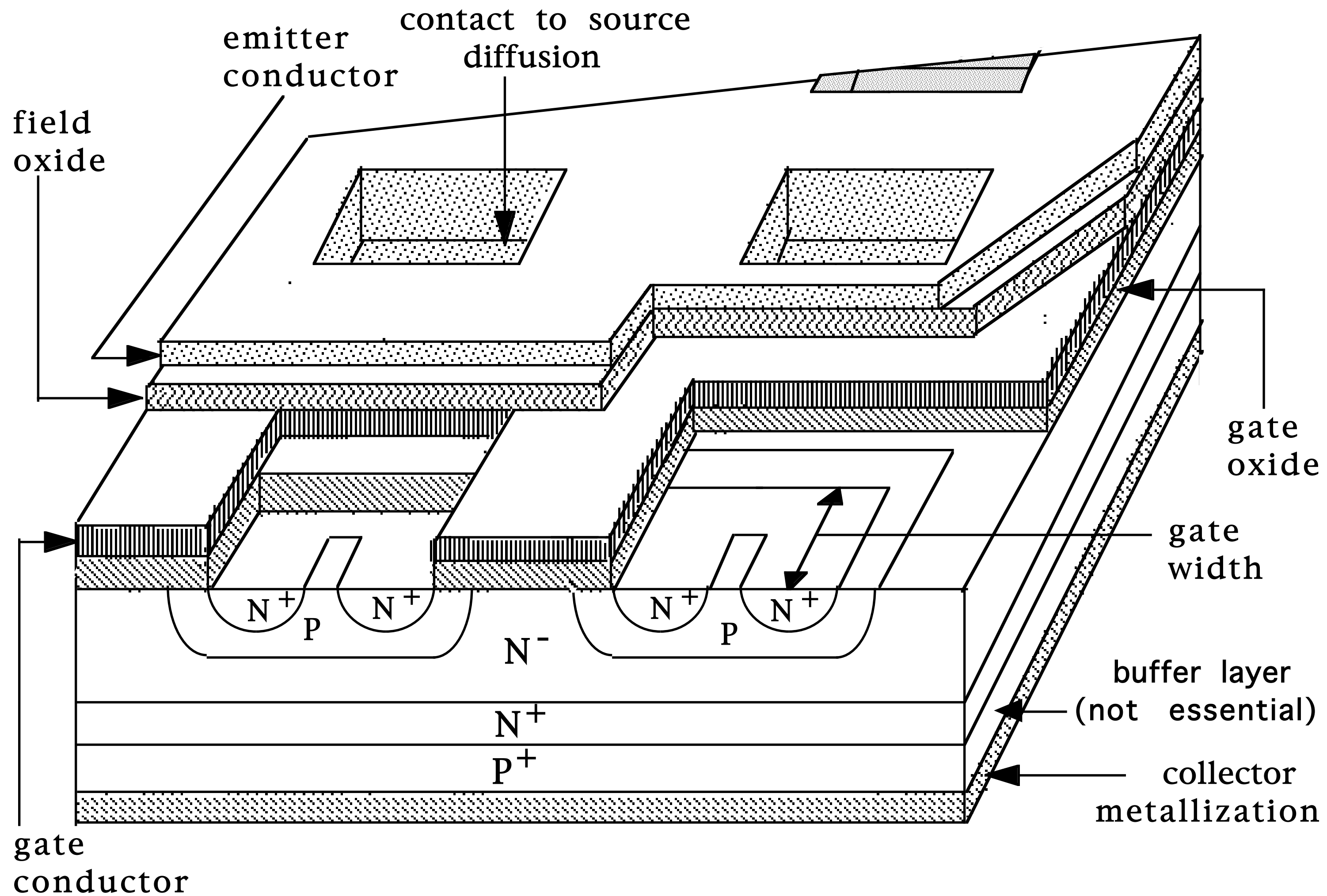
Multi-cell Structure of IGBT

- IGBT = insulated gate bipolar transistor.



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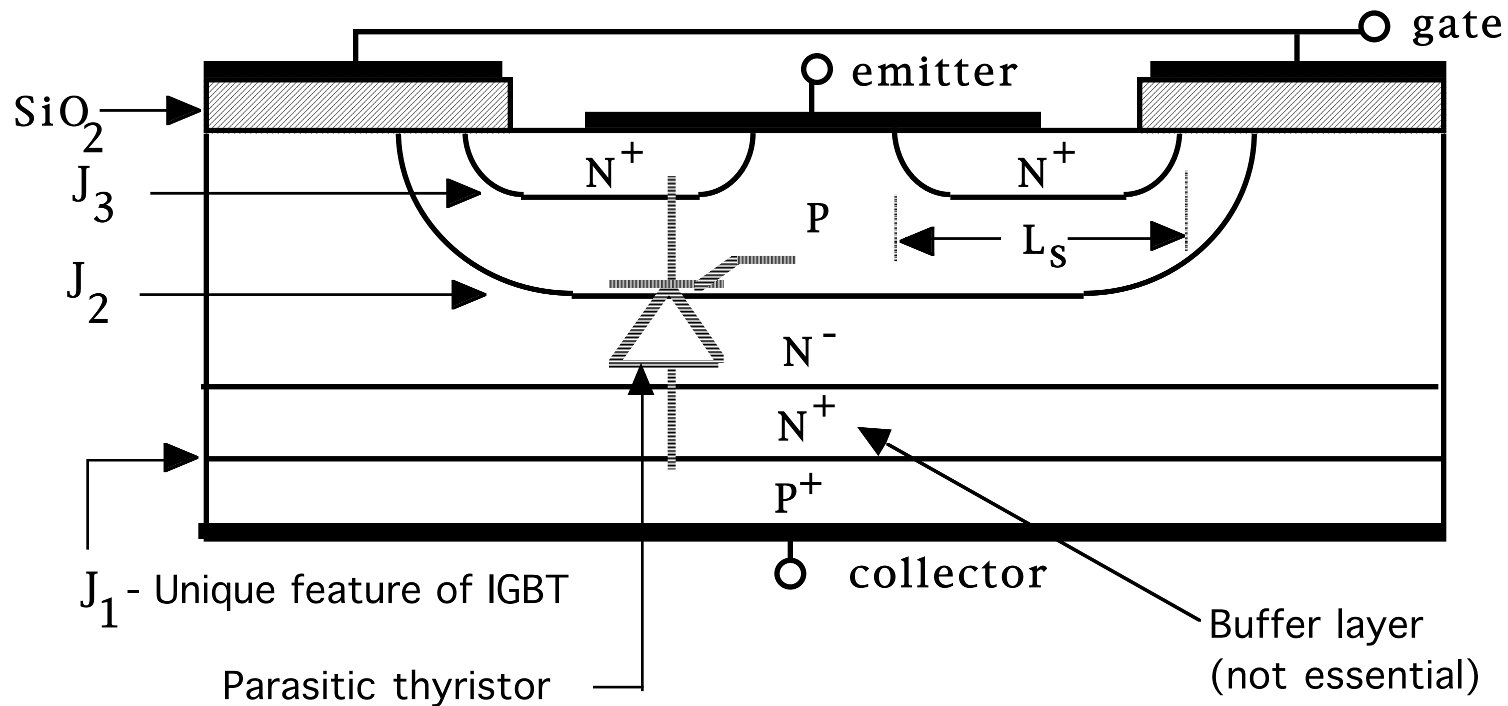
Cross-section of IGBT Cell



- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at collector end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N^+ buffer layer present.
- Non-punch-through (NPT) IGBT - N^+ buffer layer absent.

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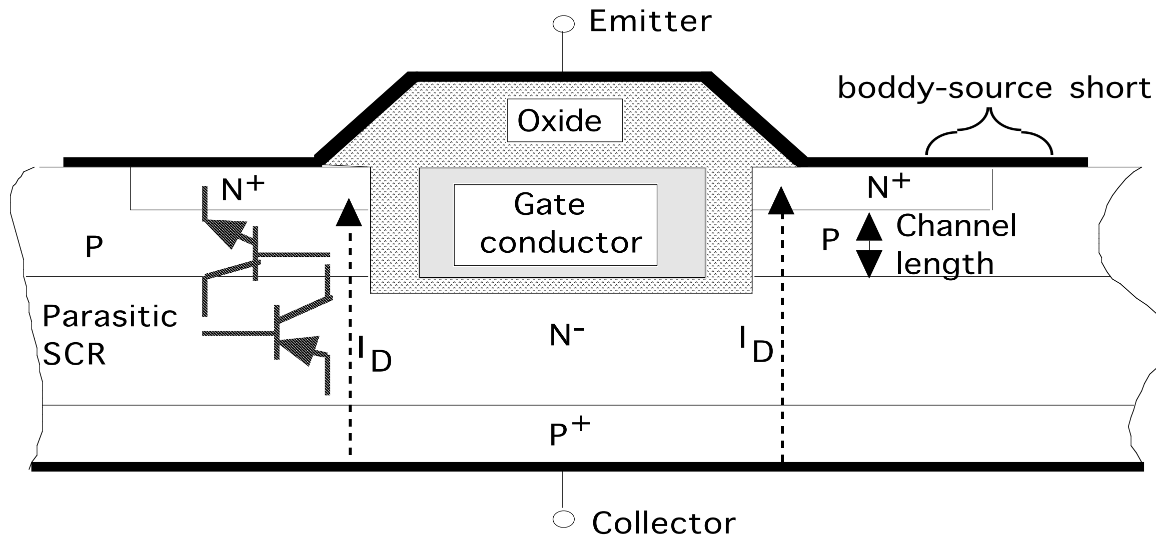
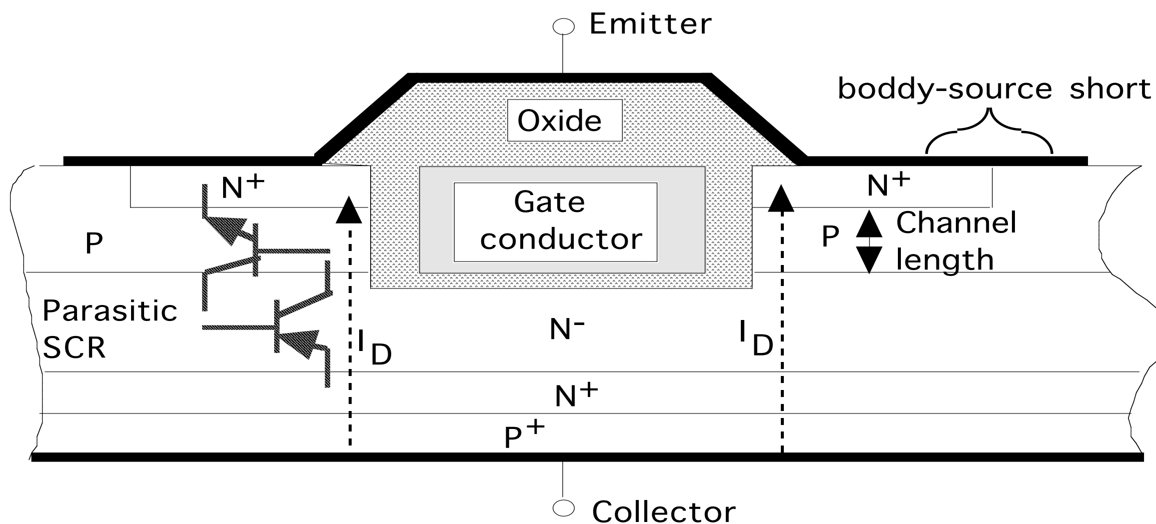
Cross-section of Trench-Gate IGBT Unit Cell



- Non-punch-thru IGBT



- Punch-thru IGBT

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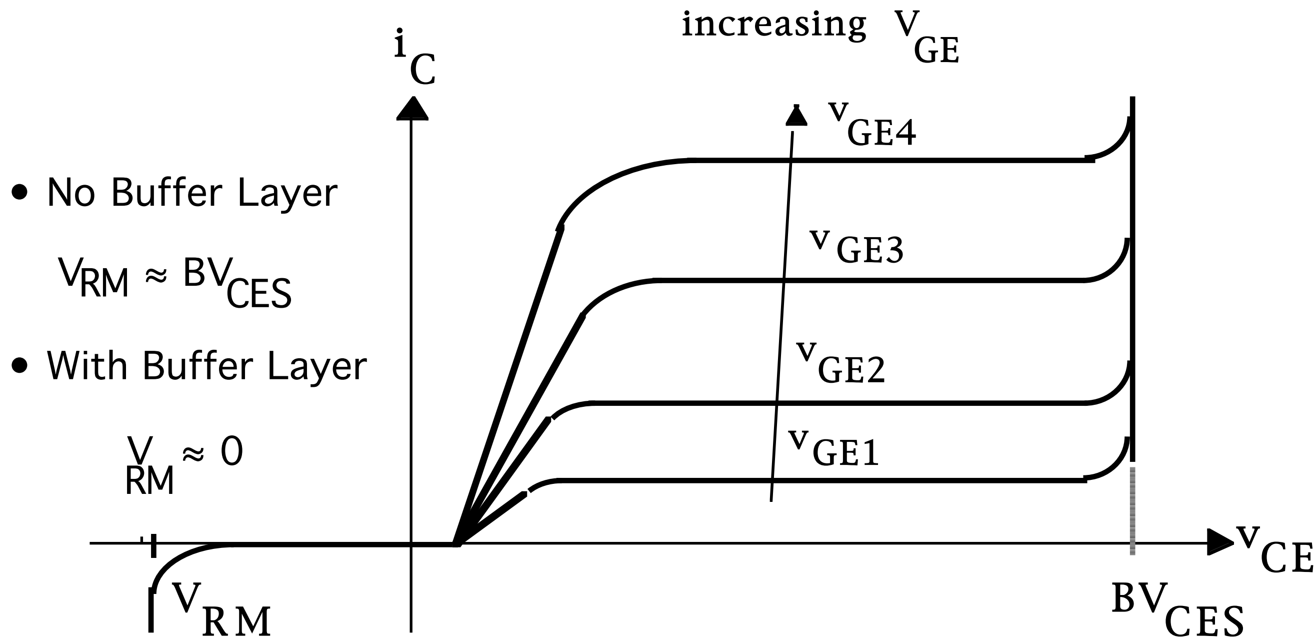
IGBT I-V Characteristics and Circuit Symbols

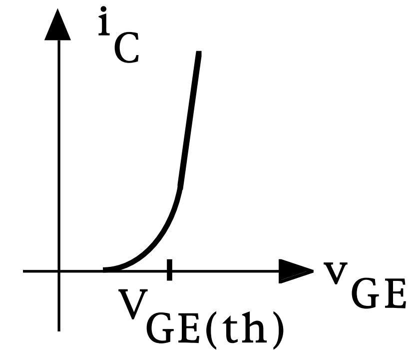


- No Buffer Layer

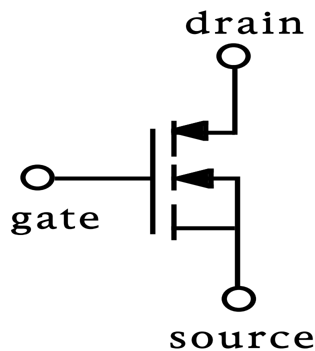
  $V_{RM} \approx BV_{CES}$

- With Buffer Layer

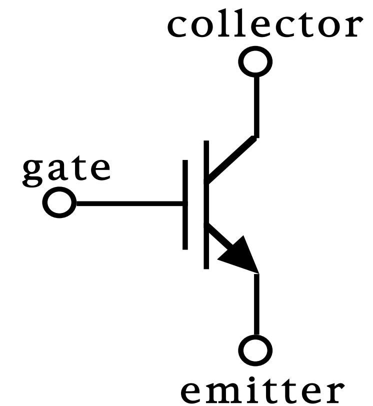
  $V_{RM} \approx 0$



- Transfer curve



- N-channel IGBT circuit symbols



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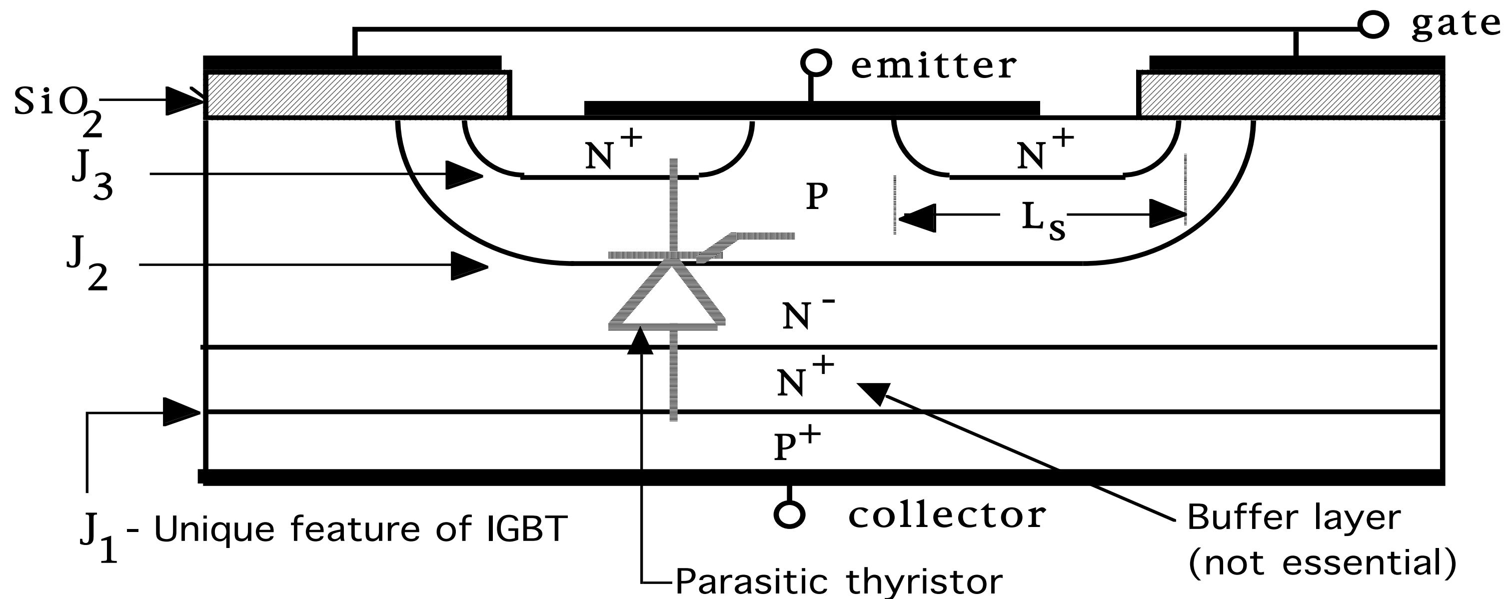
Blocking (Off) State Operation of IGBT



- Blocking state operation - $V_{GE} < V_{GE(th)}$
- Junction J_2 is blocking junction - n^+ drift region holds depletion layer of blocking junction.
- Without N^+ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With N^+ buffer layer, junction J_1 has small breakdownvoltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

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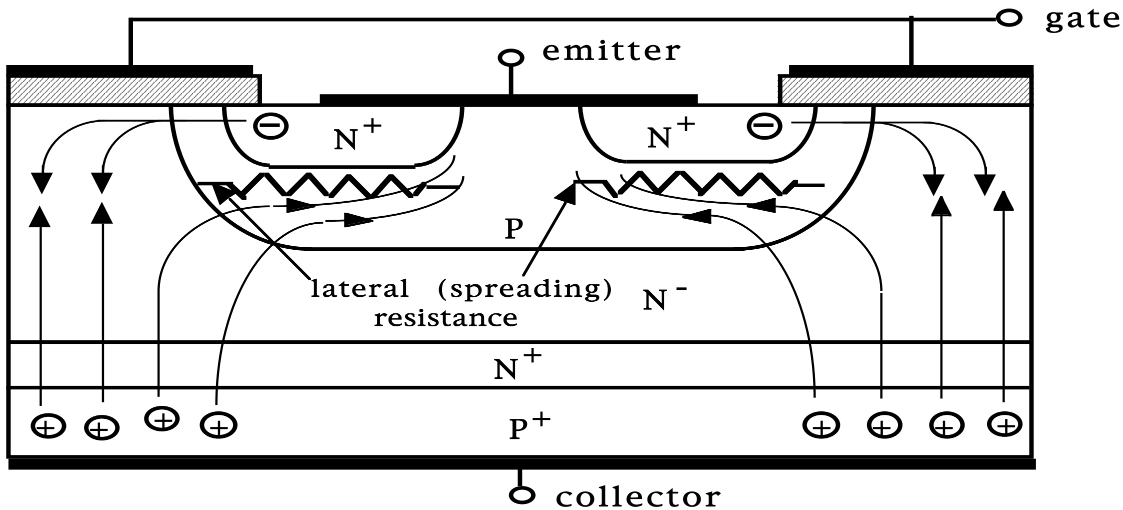
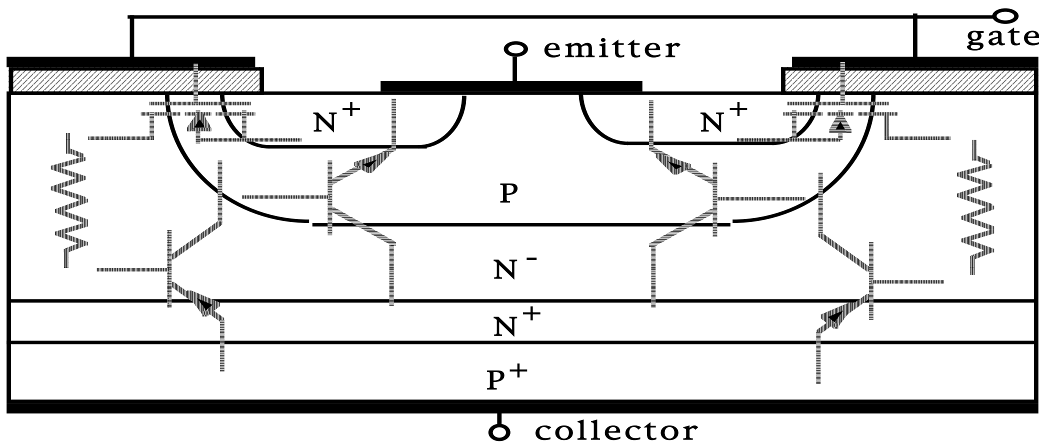
IGBT On-state Operation





- MOSFET section designed to carry most of the IGBT collector current
- On-state $V_{CE(on)}$ = $V_{J1} + V_{drift} + I_C R_{channel}$
- Hole injection into drift region from J_1 minimizes V_{drift}.

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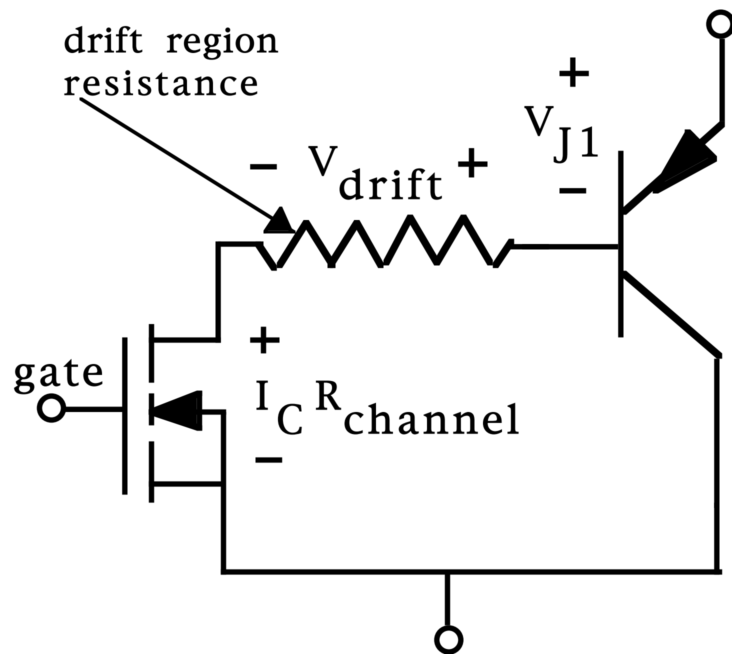
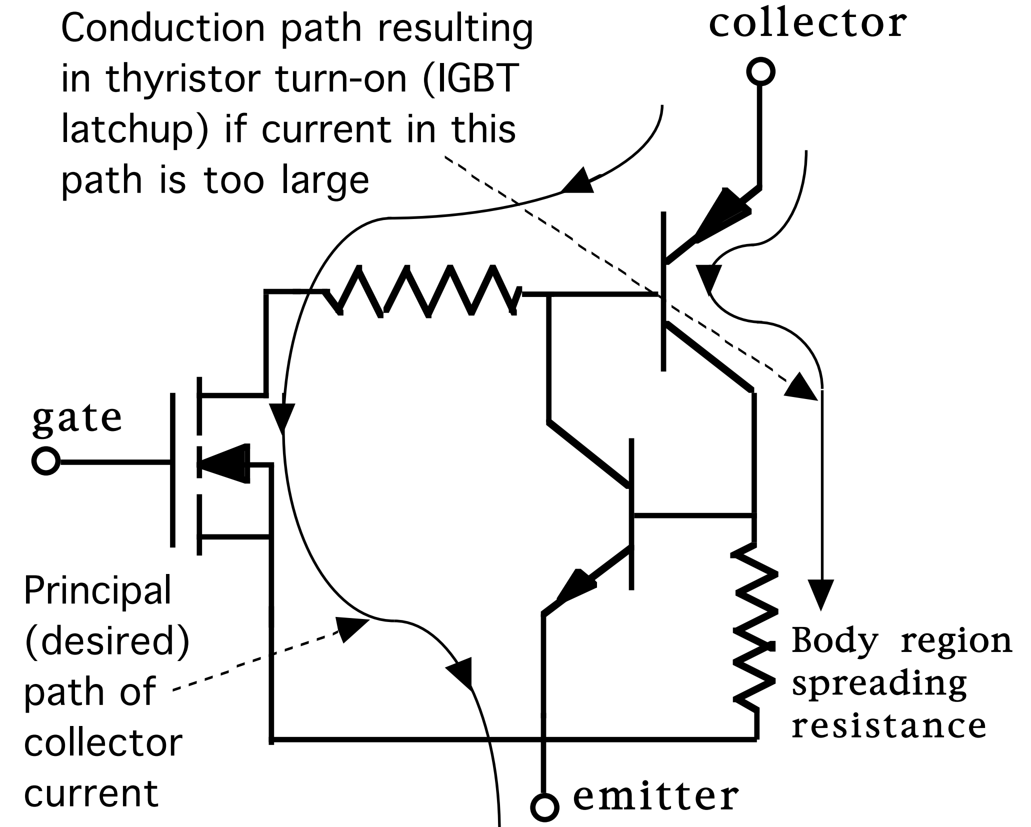
Approximate Equivalent Circuits for IGBTs





- Approximate equivalent circuit for IGBT valid for normal operating conditions.

- $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$

- IGBT equivalent circuit showing transistors comprising the parasitic thyristor.

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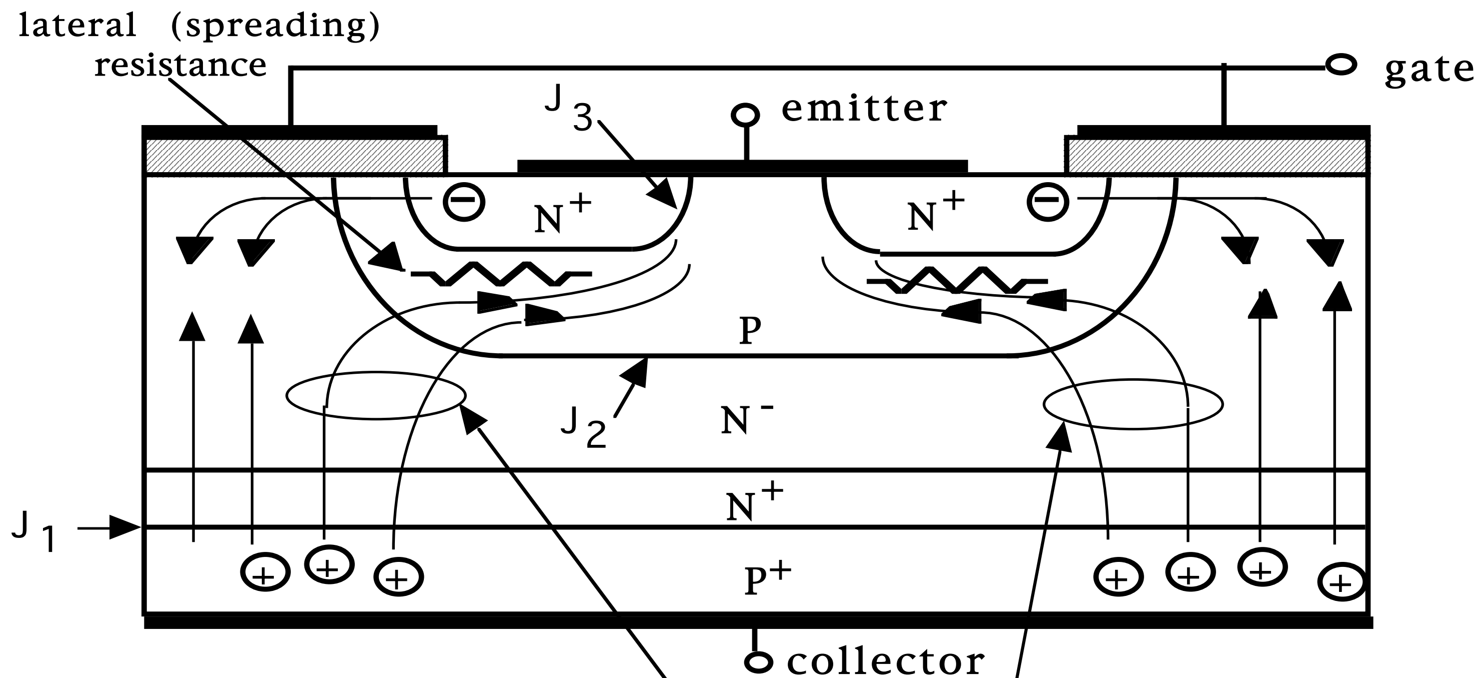
Static Latchup of IGBTs



Conduction paths causing lateral voltage drops and turn-on of parasitic thyristor if current in this path is too large

- Lateral voltage drops, if too large, will forward bias junction J3.
- Parasitic npn BJT will be turned on, thus completing turn-on of parasitic thyristor.
- Large power dissipation in latchup will destroy IGBT unless terminated quickly. External circuit must terminate latchup - no gate control in latchup.

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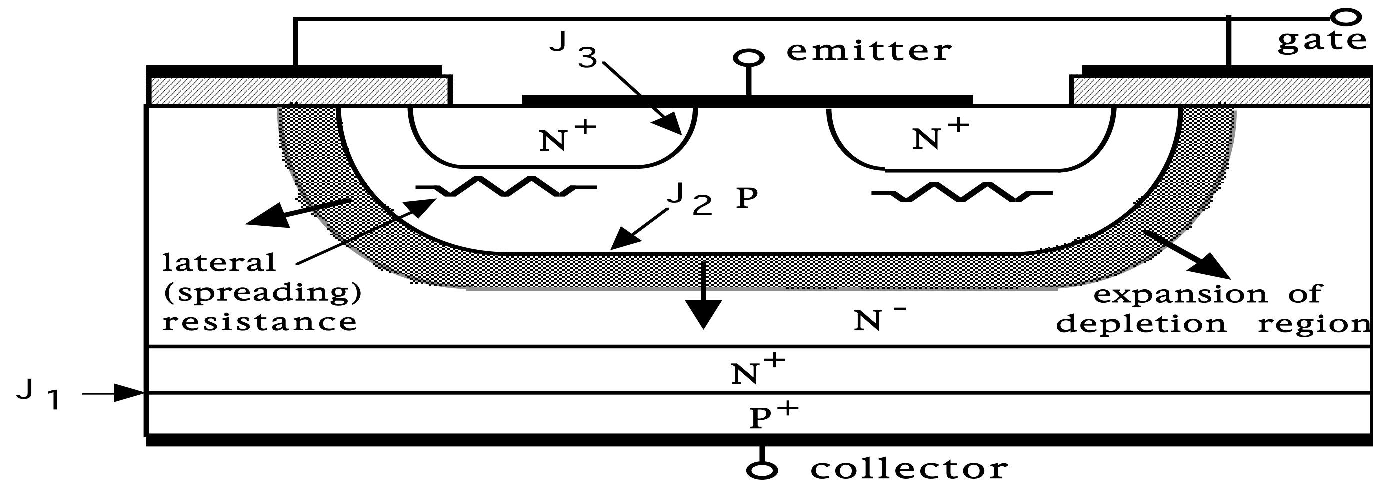
Dynamic Latchup Mechanism in IGBTs



- MOSFET section turns off rapidly and depletion layer of junction J2 expands rapidly into N^- layer, the base region of the pnp BJT.
- Expansion of depletion layer reduces base width of pnp BJT and its a increases.
- More injected holes survive traversal of drift region and become "collected" at junction J2.
- Increased pnp BJT collector current increases lateral voltage drop in p-base of npn BJT and latchup soon occurs.
- Manufacturers usually specify maximum allowable drain current on basis of dynamic latchup.

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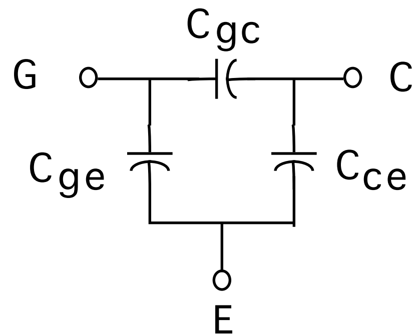
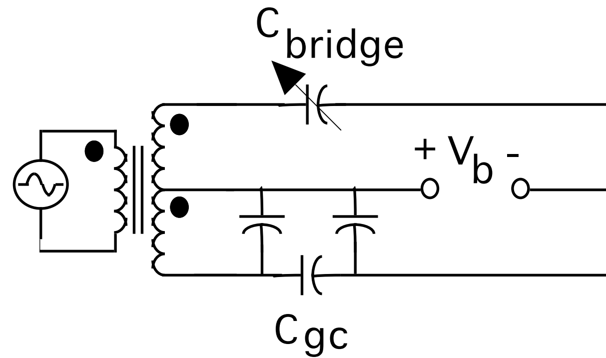
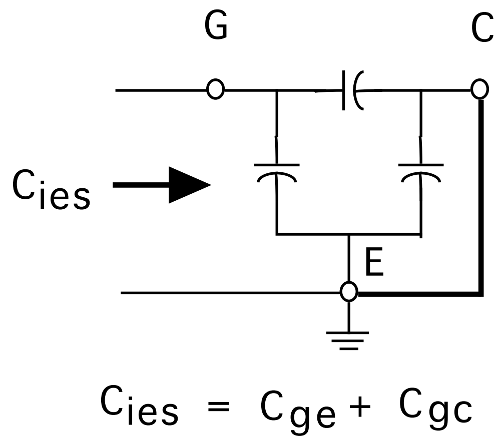
Internal Capacitances Vs Spec Sheet Capacitances

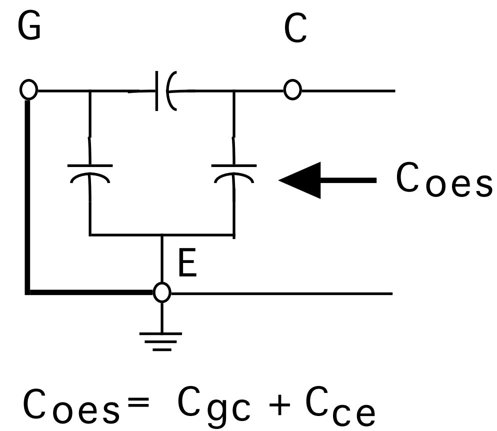




Bridge balanced (Vb=0) Cbridge = $C_{gc} = C_{res}$



$C_{ies} = C_{ge} + C_{gc}$



$C_{oes} = C_{gc} + C_{ce}$

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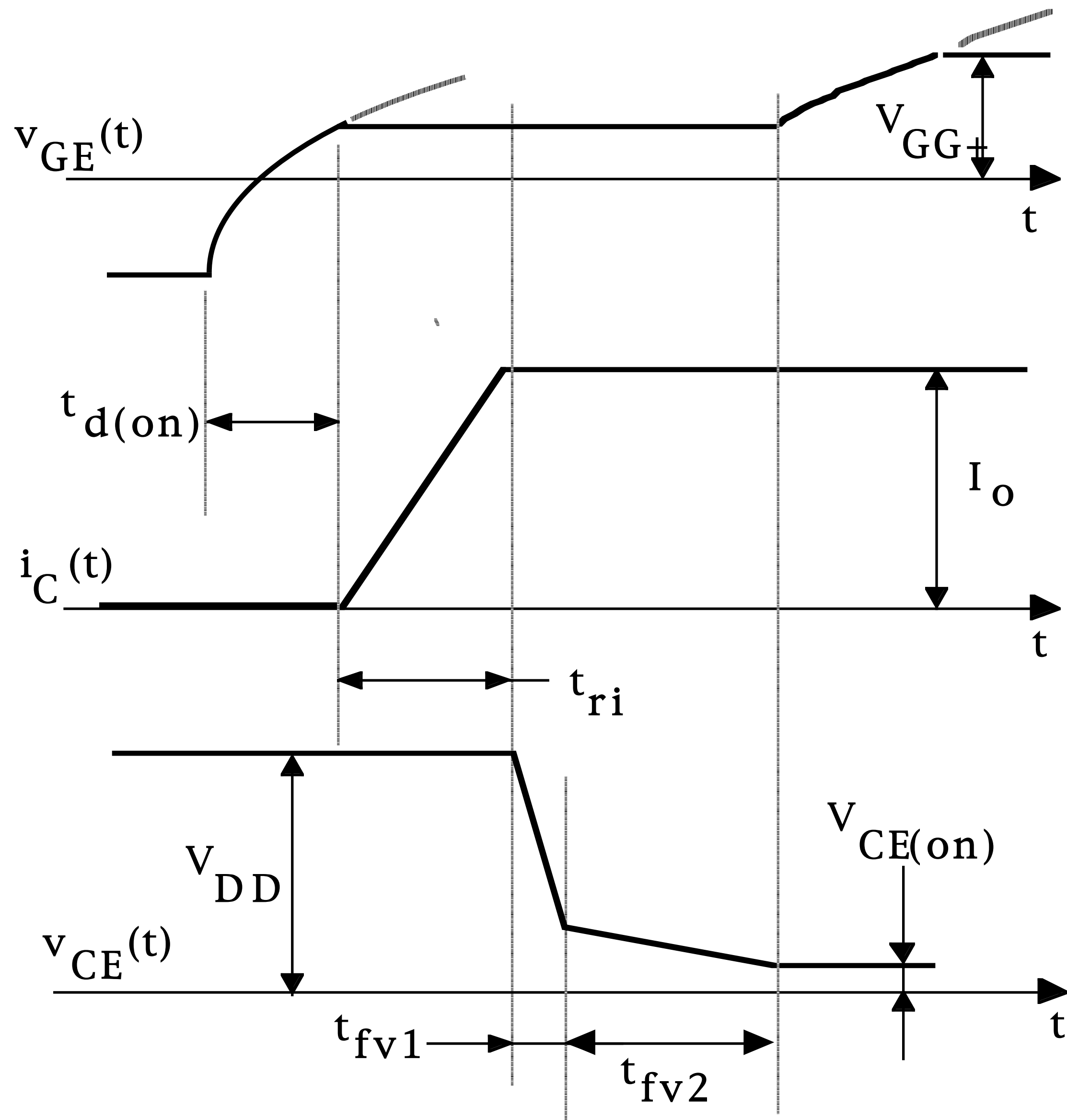
IGBT Turn-on Waveforms

- Turn-on waveforms for IGBT embedded in a stepdown converter.
- Very similar to turn-on waveforms of MOSFETs.
- Contributions to t_{vf2}.
  - Increase in C_{ge} of MOSFET section at low collector-emitter voltages.
  - Slower turn-on of pnp BJT section.



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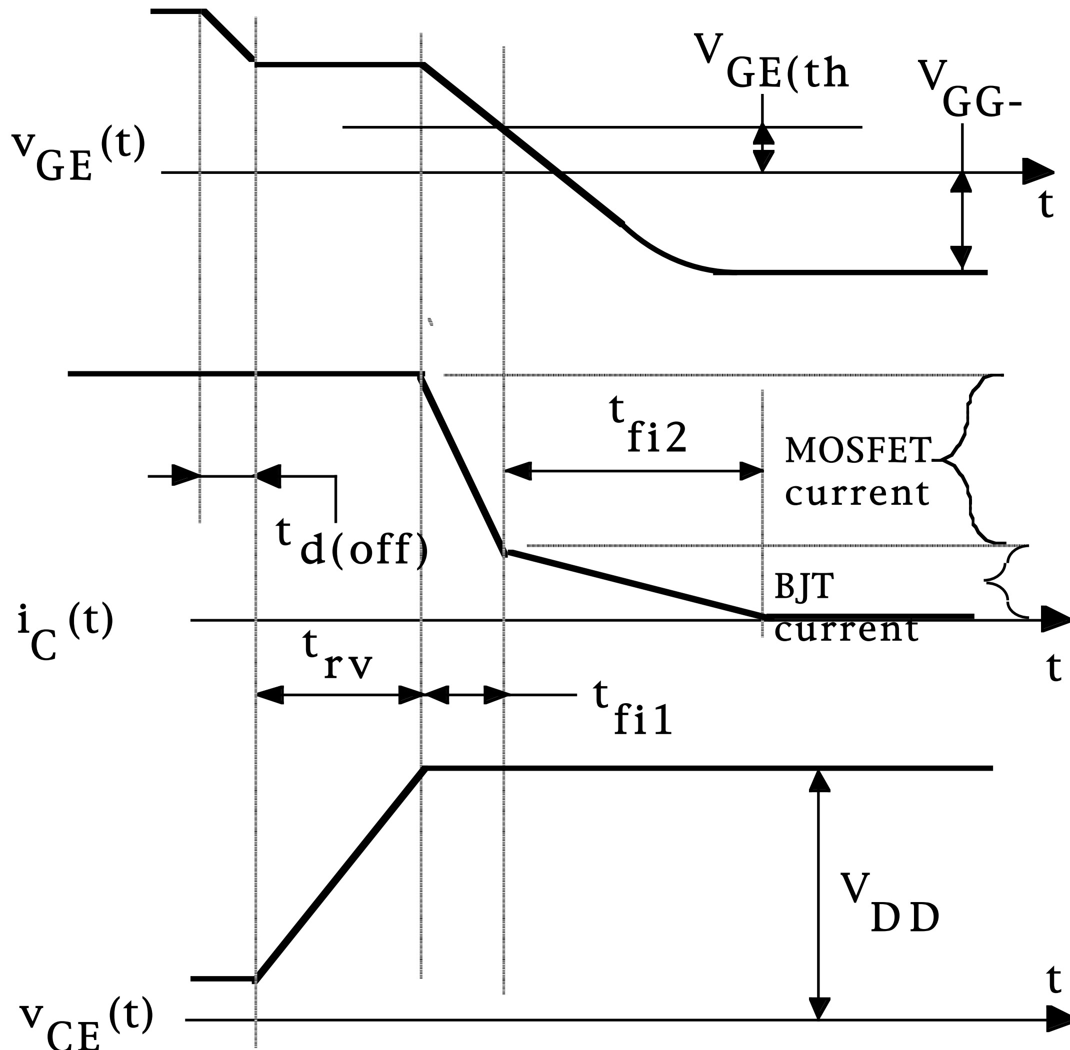
IGBT Turn-off Waveforms



- Turn-off waveforms for IGBT embedded in a stepdown converter.
- Current "tailing" (t_{fi2}) due to stored charge trapped in drift region (base of pnp BJT) by rapid turn-off of MOSFET section.
- Shorten tailing interval by either reducing carrier lifetime or by putting N^+ buffer layer adjacent to injecting P^+ layer at drain.
- Buffer layer acts as a sink for excess holes otherwise trapped in drift region becasue lifetime in buffer layer can be made small without effecting on-state losses - buffer layer thin compared to drift region.

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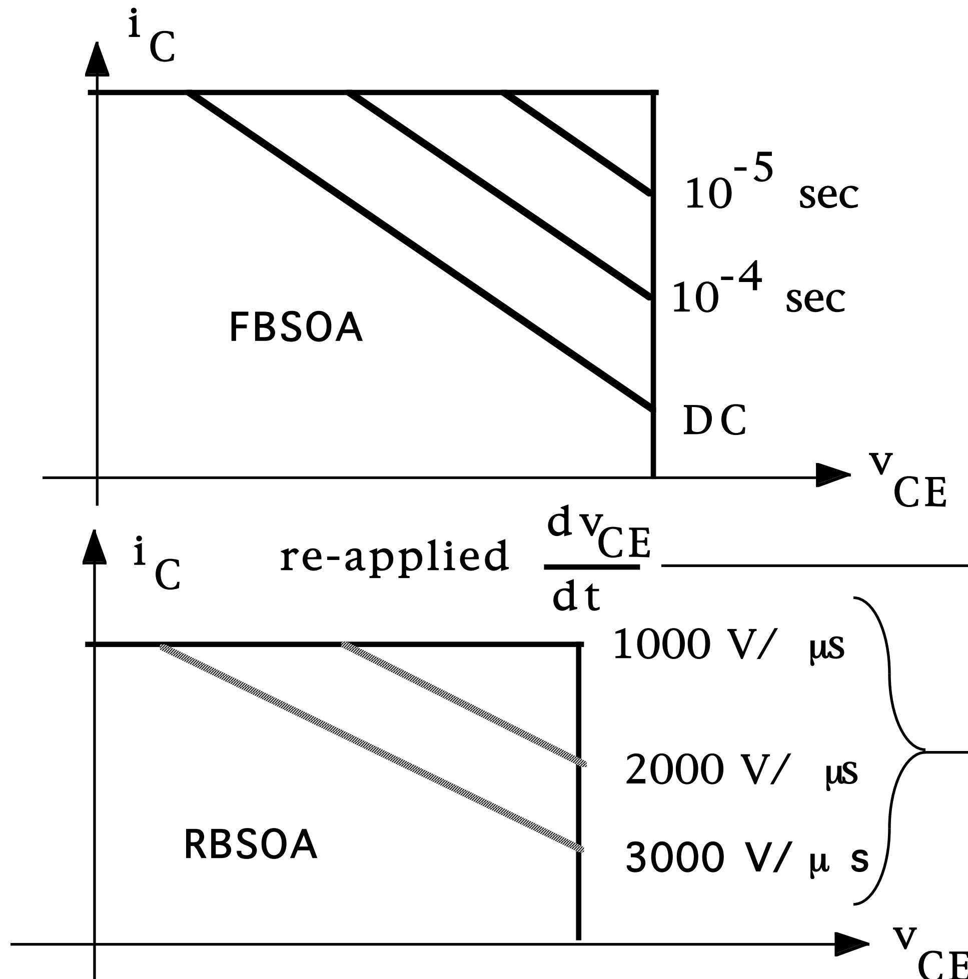
IGBT Safe Operating Area



- Maximum collector-emitter voltages set by breakdown voltage of pnp transistor - 2500 v devices available.
- Maximum collector current set by latchup considerations - 100 A devices can conduct 1000 A for 10 µsec and still turn-off via gate control.
- Maximum junction temp. = 150 C.
- Manufacturer specifies a maximum rate of increase of re-applied collector-emitter voltage in order to avoid latchup.

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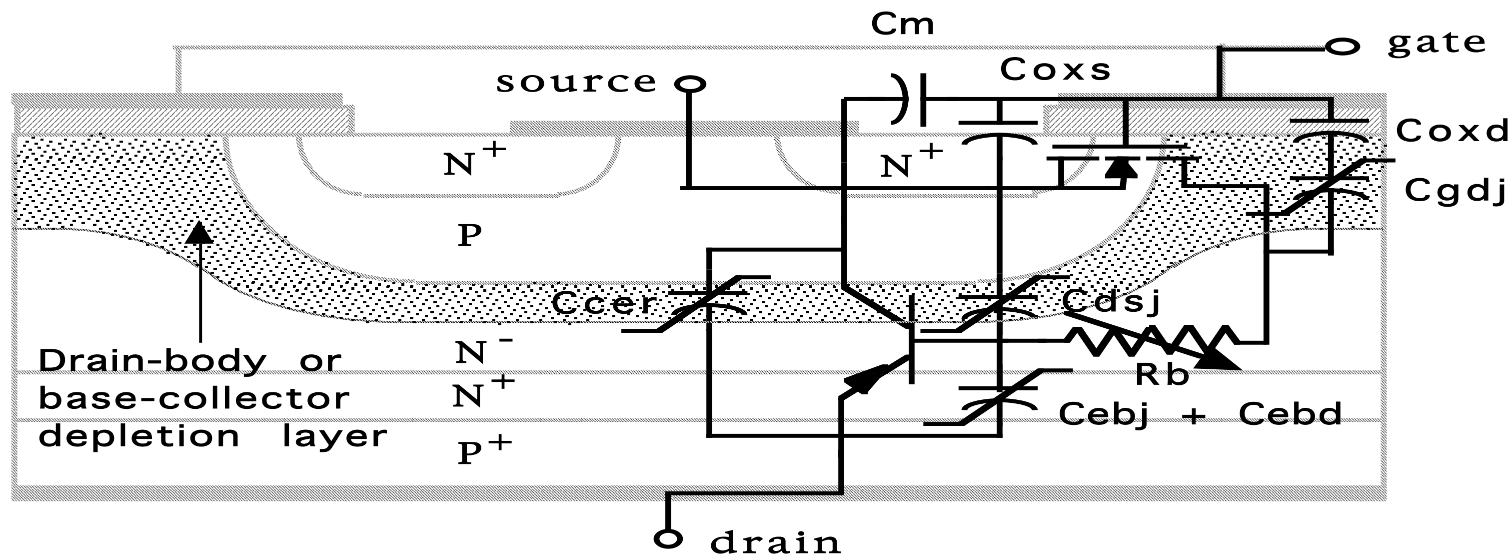
Development of PSpice IGBT Model



- Nonlinear capacitors Cdsj and Ccer due to N^-P junction depletion layer.
- Nonlinear capacitor Cebj + Cebd due to P^+N^+ junction
- MOSFET and PNP BJT are intrinsic (no parasitics) devices
- Nonlinear resistor Rb due to conductivity modulation of N^- drain drift region of MOSFET portion.
- Nonlinear capacitor Cgdj due to depletion region of drain-body junction (N^-P junction).
- Circuit model assumes that latchup does not occur and parasitic thyristor does not turn.

- Reference - "An Experimentally Verified IGBT Model Implemented in the SABER Circuit Simulator", Allen R. Hefner, Jr. and Daniel M. Diebolt, IEEE Trans. on Power Electronics, Vol. 9, No. 5, pp. 532-542, (Sept., 1994)

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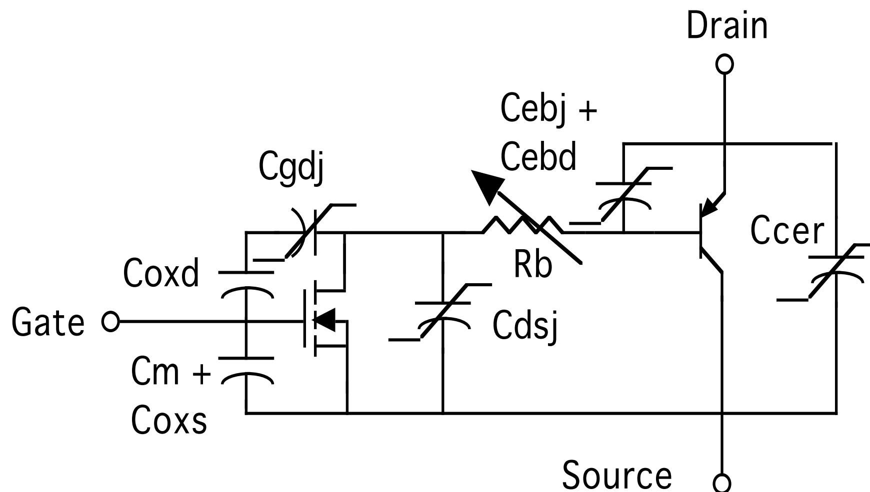
Parameter Estimation for PSpice IGBT Model

- Built-in IGBT model requires nine parameter values.
  - Parameters described in Help files of Parts utility program.

- Parts utility program guides users through parameter estimation process.
  - IGBT specification sheets provided by manufacturer provide sufficient informaiton for general purpose simulations.
  - Detailed accurate simulations, for example device dissipation studies, may require the user to carefully characterize the selected IGBTs.



- Built-in model does not model ultrafast IGBTs with buffer layers (punch-through IGBTs) or reverse free-wheeling diodes

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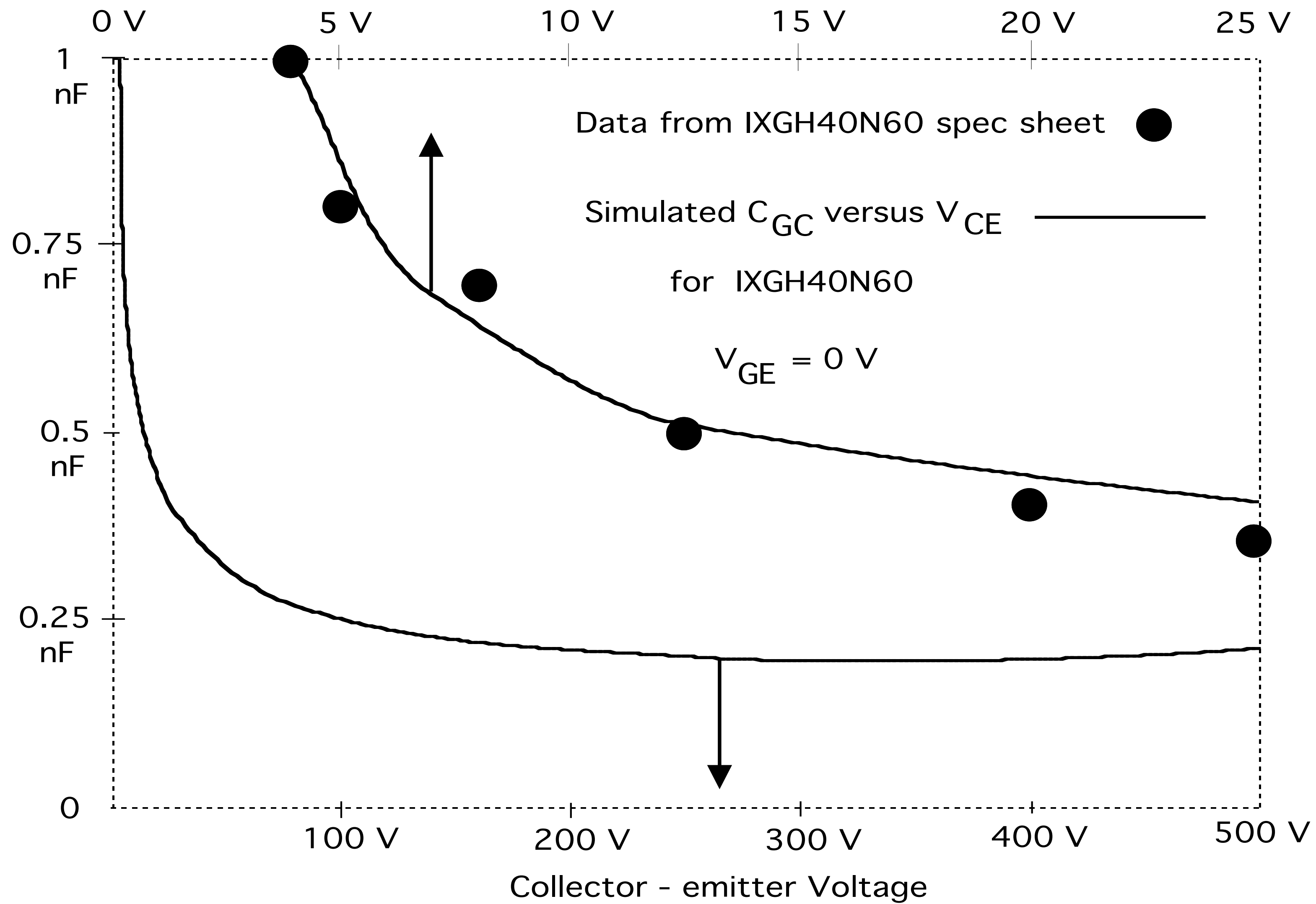
PSpice IGBT - Simulation Vs Experiment



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Lecture Notes

Emerging Devices

Outline

- Power JFET Devices
- Field-Controlled Thyristor
- MOS-Controlled Thyristor
- High Voltage Integrated Circuits/ Discrete Modules
- New Semiconductor Materials

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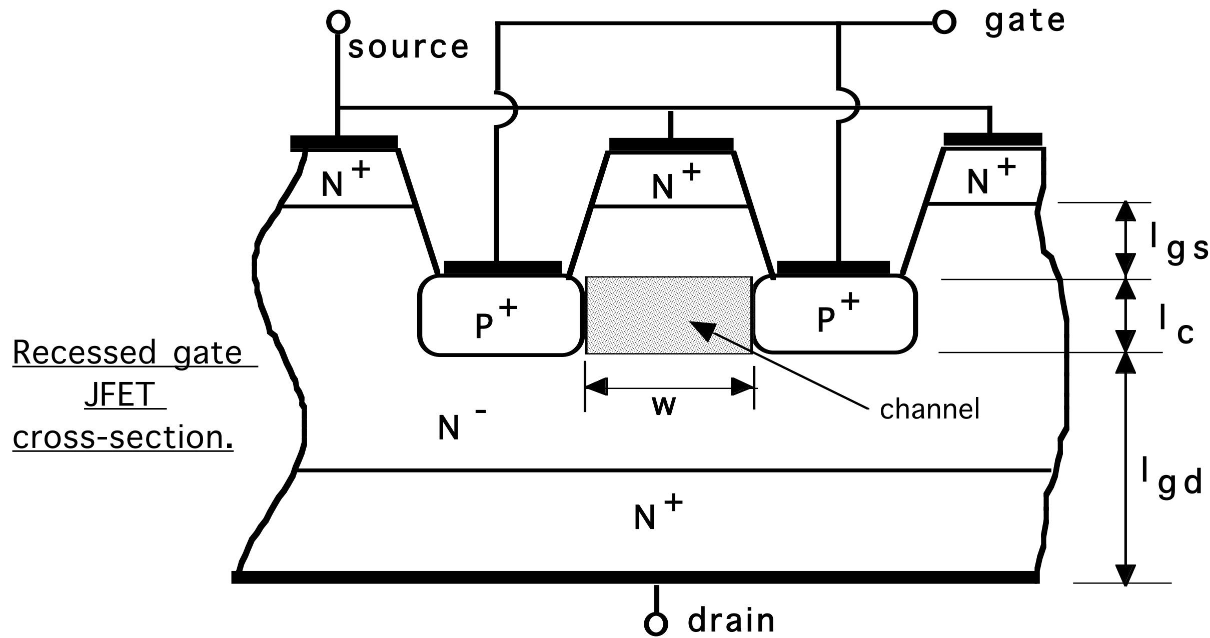
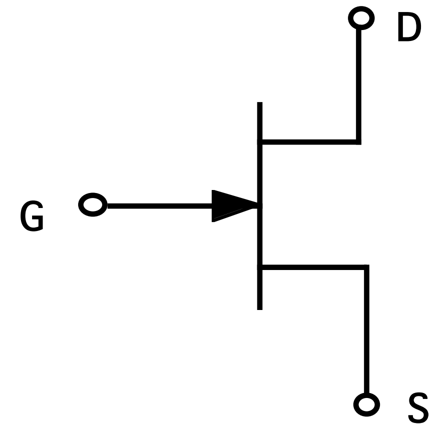
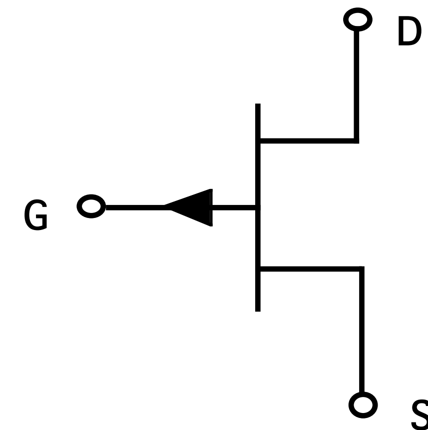
Power JFET Geometry







- Gate-source geometry highly interdigitated as in MOSFETs.
- Width w = μms to a few tens of μms ; $l_c < w$; l_{gs} minimized.
- l_{gd} set by blocking voltage considerations.

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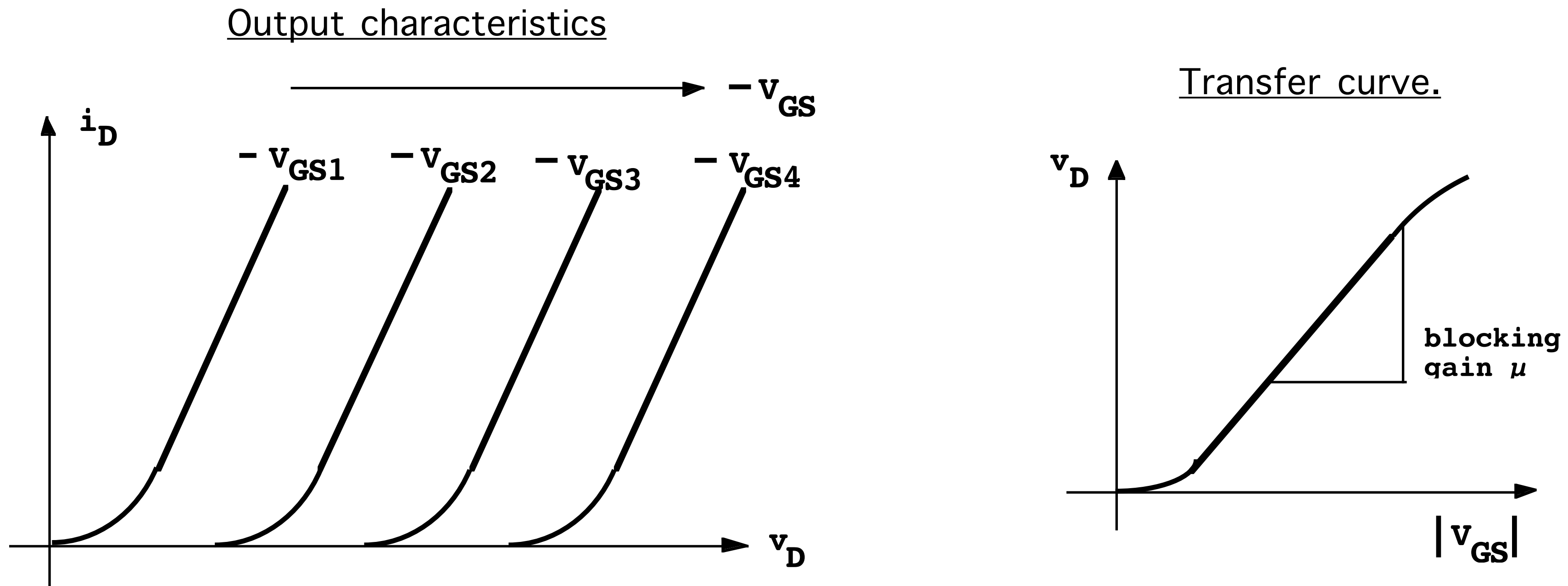
Power JFET I-V Characteristics



- Power JFET is a normally-on device. Substantial current flows when gate-source voltage is equal to zero.
- Opposite to BJTs, MOSFETs, and IGBTs which are normally-off devices.

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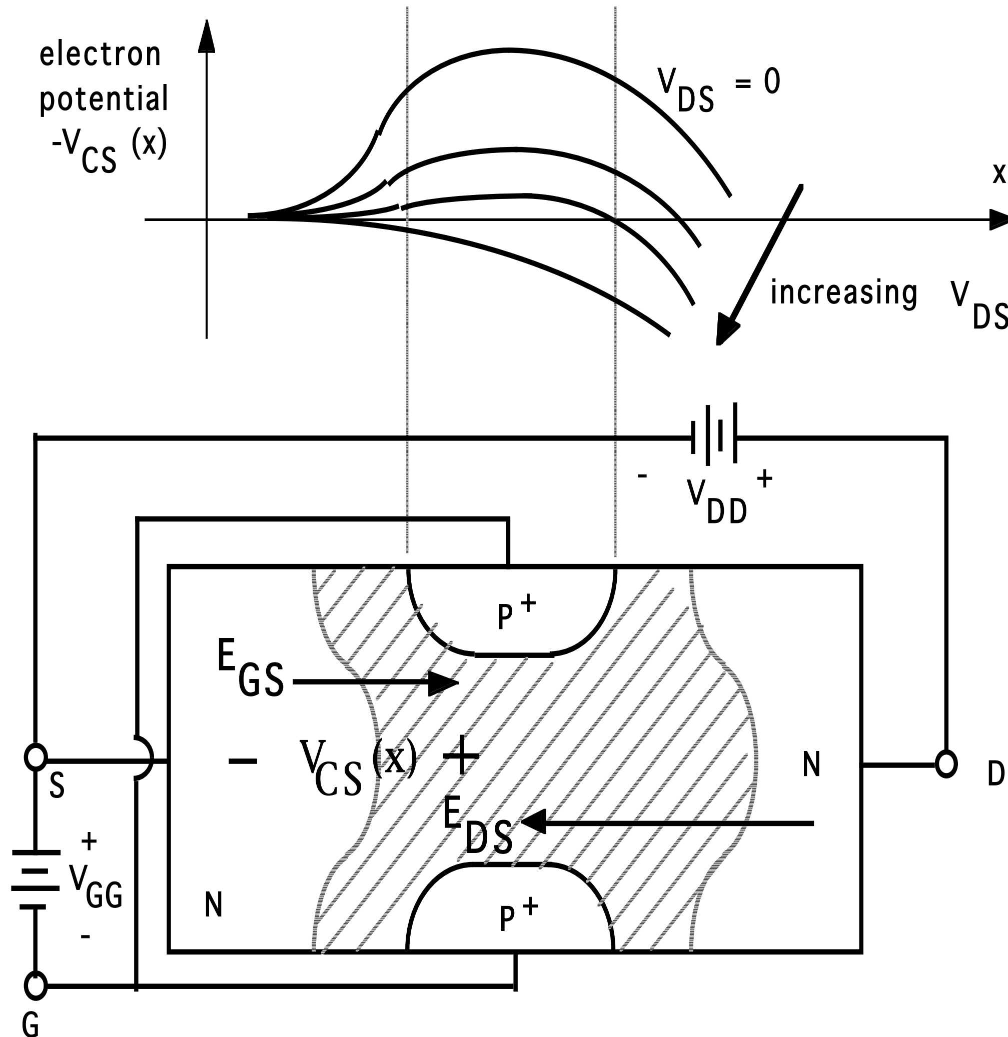
Controlling Potential Barrier in JFETs



- $|V_{GS}| > |V_p|$ (pinchoff voltage) potential barrier to electron flow from source to drain created. No drain current can flow.
- Suppress potential barrier by increasing V_{DS} at fixed V_{GS}. When $V_{DS} > \mu\, |V_{GS}|$ substantial drain currents flow.
- Blocking capability limited by magnitude of electric field in drift region. Longer drift regions have larger blocking voltage capability.
- Normally-off JFET created by having narrow enough channel width so that the channel is pinched off at zero gate-source voltage.

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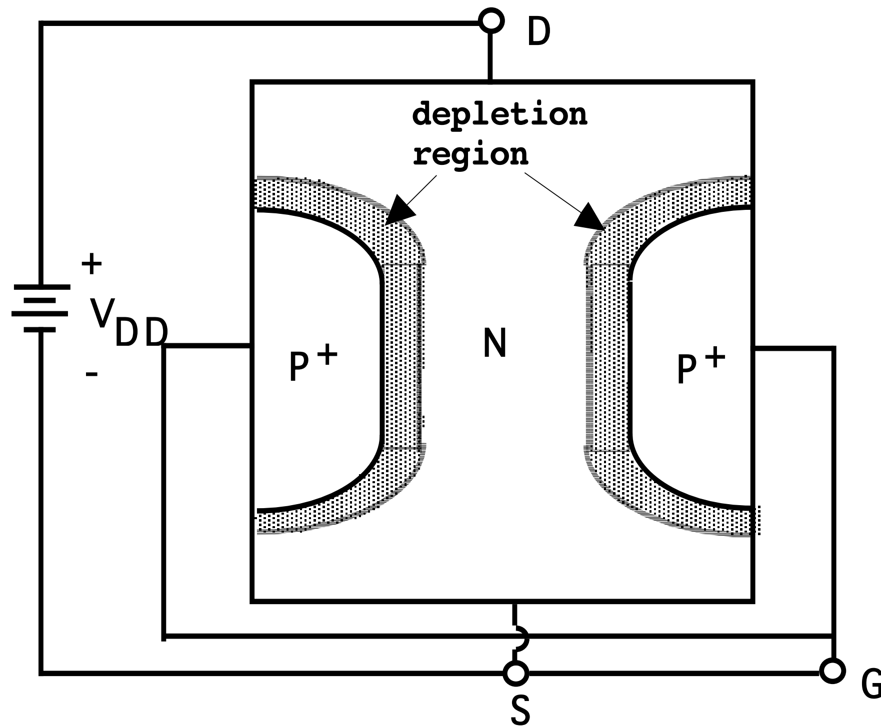
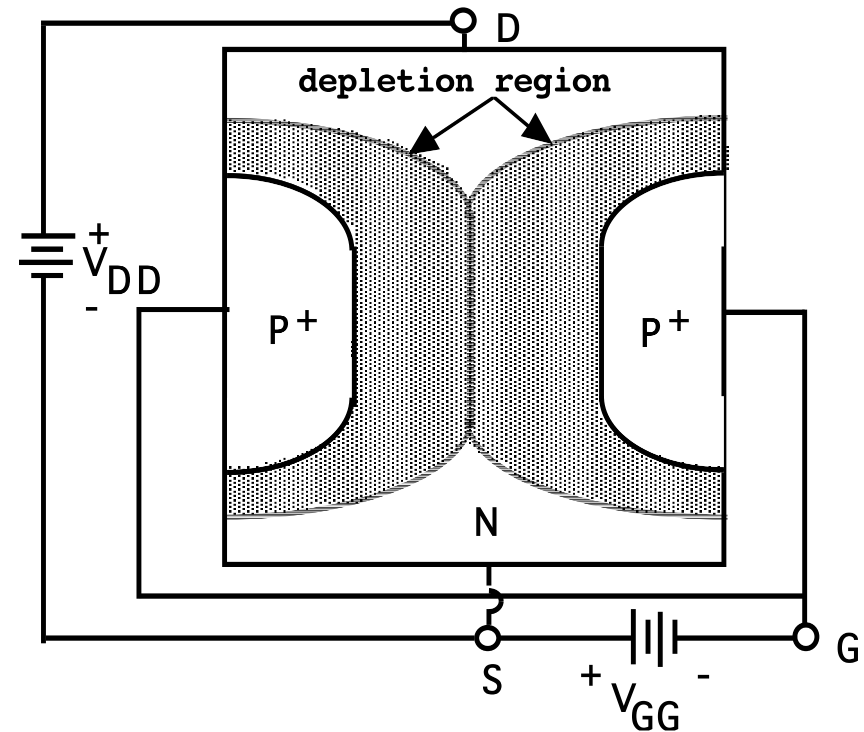
JFET On and Off States



- **Channel open between drain and source.**



- **Channel pinched-off (closed) between drain and source.**

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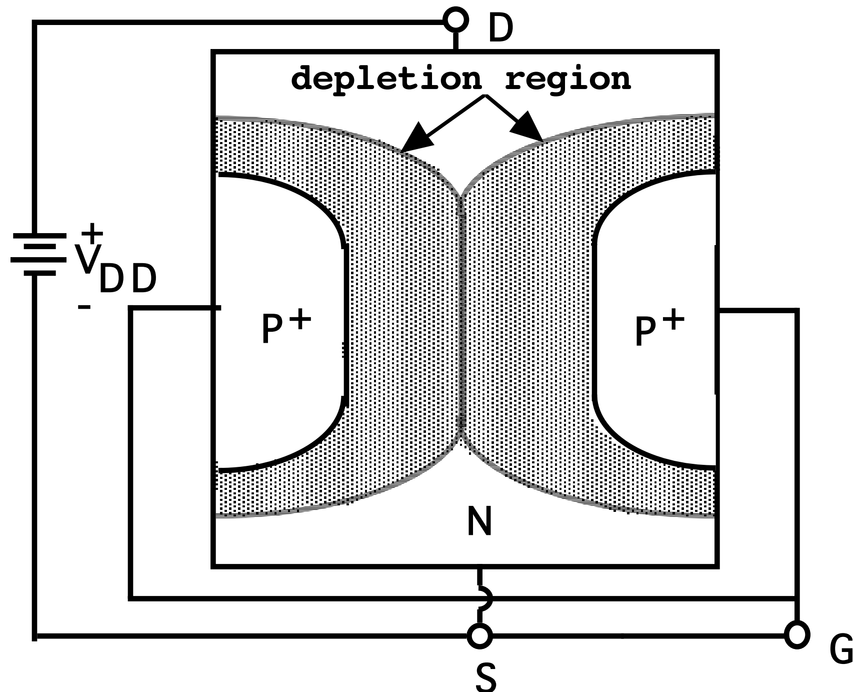
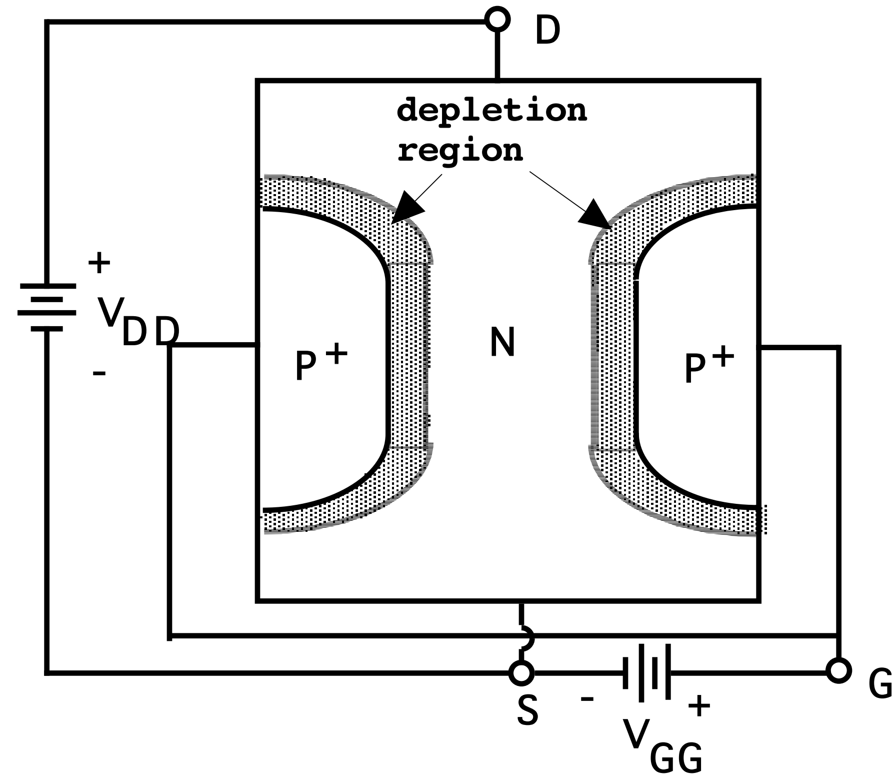
Bipolar Static Induction Transistor (BSIT)

BSIT in blocking state



- Channel width and channel doping chosen so that at zero gate-source voltage, depletion layers of gate-channel junction pinch-off the channel.
- Narrower channel than normally-on JFET.

JFET in on-state



- Forward bias gate-channel junction to reduce depletion region width and open up channel.
- Substantial current flow into gate.

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JFET Switching Characteristics

- Equivalent circuits of JFETS nearly identical to those of MOSFETs
- Switching waveforms nearly identical to those of MOSFETs including values of various switching time intervals
- JFET V_{GS} starts at negative values and steps to zero at turn-on while MOSFET V_{GS} starts at zero and steps to positive value at turn-on
- FET on-state losses somewhat higher than for MOSFET - technology related not fundamental
- Normally-off JFET (Bipolar static induction transistor or BSIT) switching characteristics more similar to those of BJT
- Differences between BSIT and BJT observable mainly at turn-off

1. BSIT has no quasi-saturation region and thus only one current fall time (no current tailing) at turn-off.
2. Overall turn-off times of BSIT shorter than for BJT
3. Differences due to fact that BSIT has no in-line pn junction that can block sweep-out of excess carriers as does BJT

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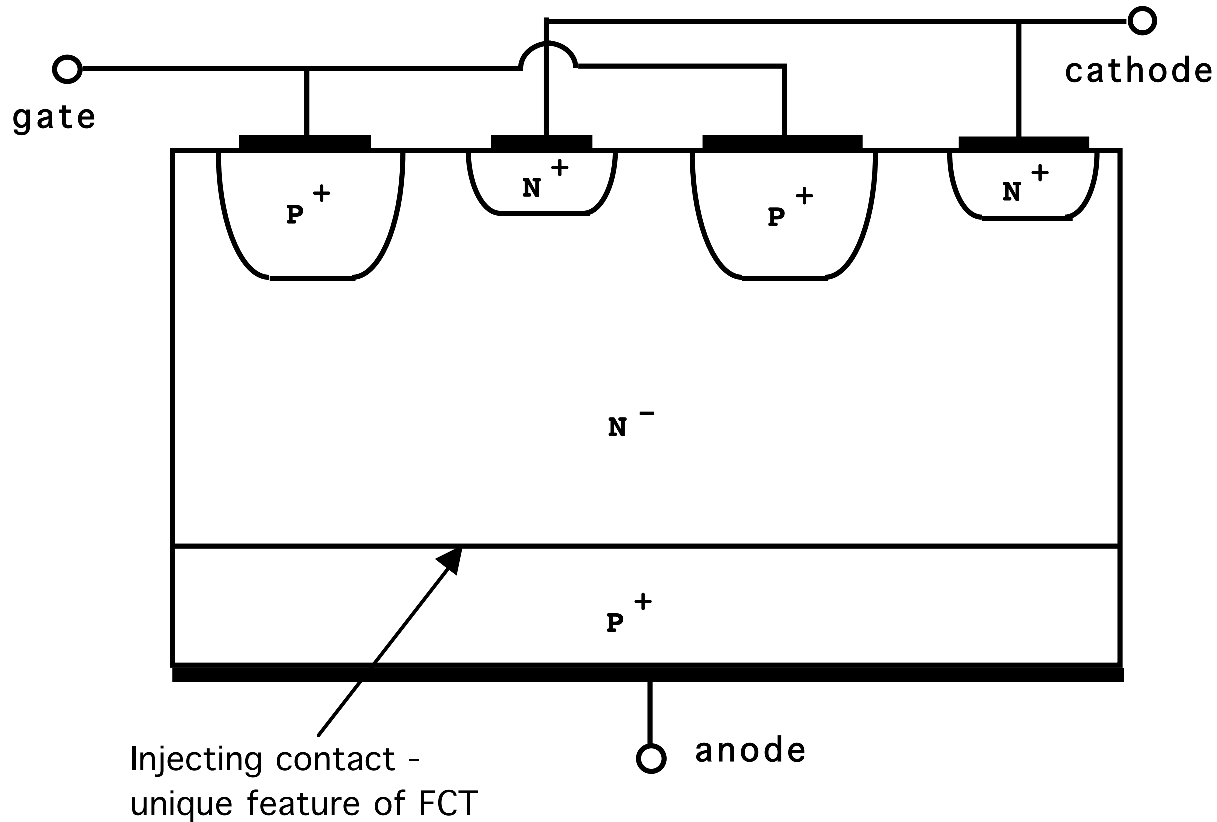
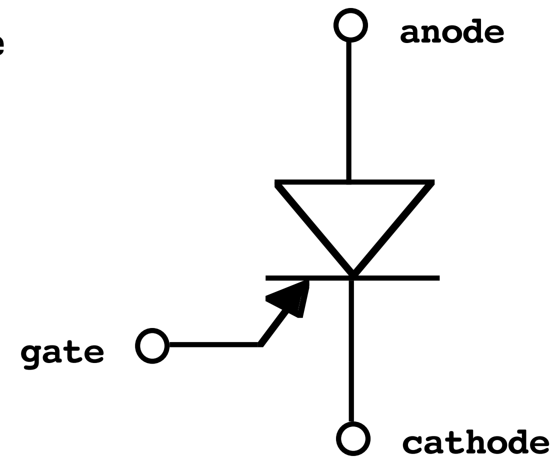
Field-Controlled Thyristor (FCT)

Vertical Cross-section



Circuit symbol



- Sometimes termed a bipolar static induction thyristor (BSIThy).

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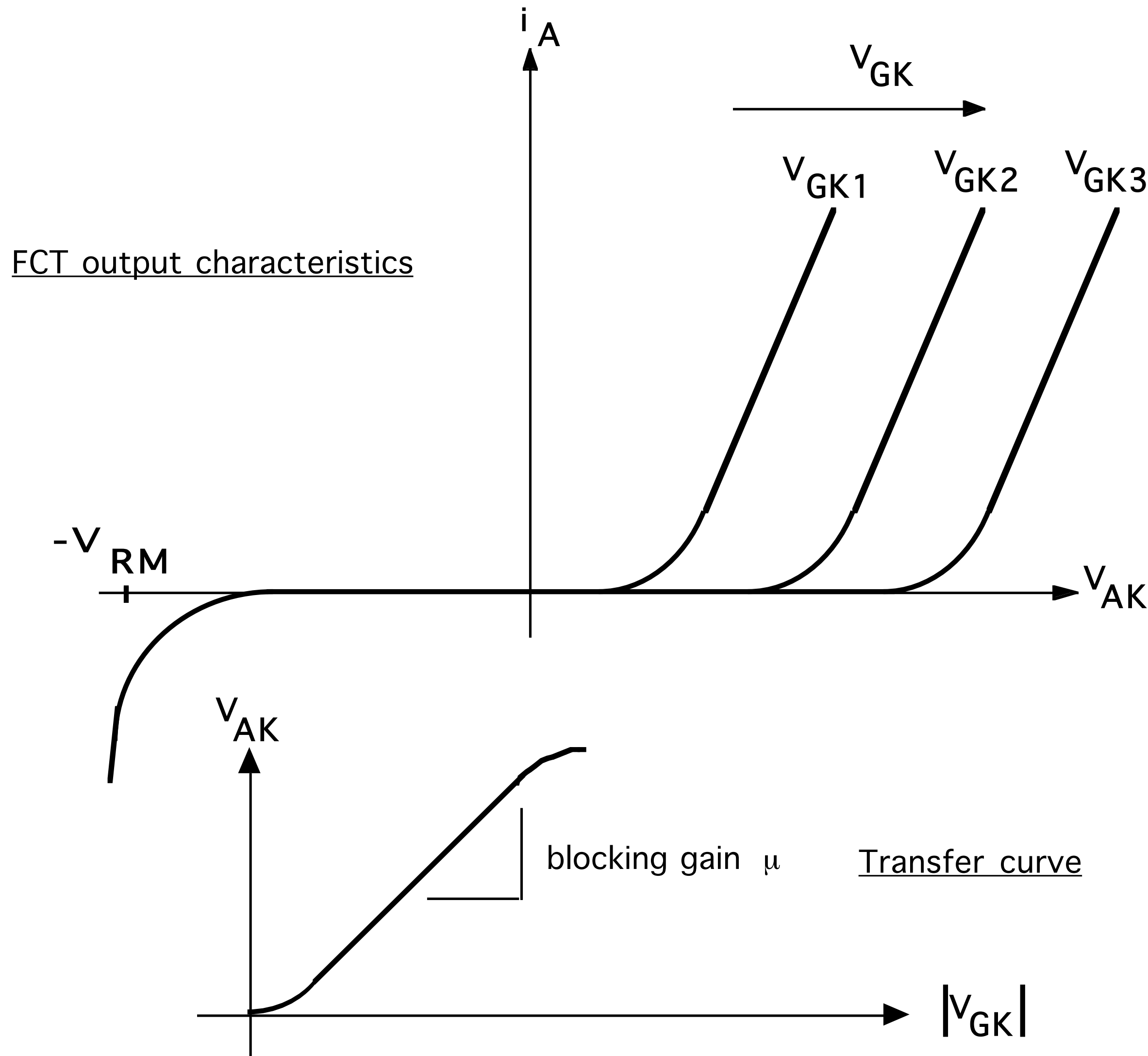
FCT I-V Characteristics



- FCT has a normally-on characteristic.
- Can be made to have a normally-off characteristic.

  1. Reduce channel width so that zero-bias depletion layer width of gate-channel junction pinches off channel

  2. Then termed a bipolar static induction thyristor (BSIThy).

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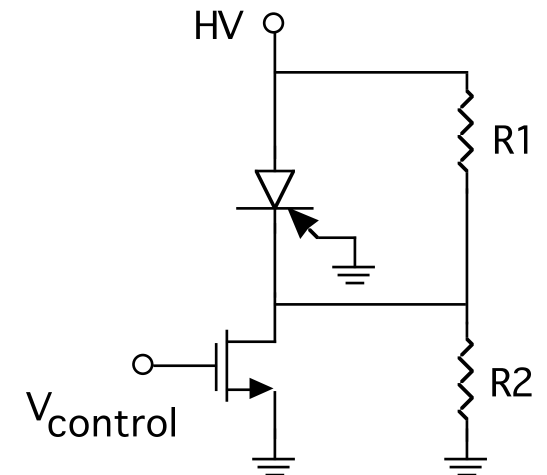
Physical Operation of FCT

- FCT essentially a power JFET with an injecting contact at the drain
- Injecting contact causes conductivity modulation of drain drift region and results in much lower on-state losses
- At turn-off, gate draws large negative current similar to a GTO because of stored charge in drift region
- FCT not a latching switch as is a GTO. FCT has no regenerative action.
- FCT can be made a normally-off device by using narrow channel widths so that zero-bias width gate depletion layer pinchs off channel.

- Cascode switching circuit.
- Implement a normally-off composite switch.
- R1 and R2 insure that voltage across MOSFET not overly large. Permits use of low voltage-high current device.



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FCT Switching Characteristics

- FCT switching waveforms qualitatively similar to thyristor or GTO including large negative gate current at turn-off.

- FCT has gate-controlled turn-on and turn-off capabilities similar to GTO.

- FCT switching times somewhat shorter than GTO.

- Gate drive must be continuously applied to FCT because FCT has no latching characteristic.

- FCT has much larger re-applied dv/dt rating than GTO because of lack of latching action.

- FCT hasdi/dt limits because of localized turn-on and then expansion of turned-on region across entire device cross-section.

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JFET-Based Devices Vs Other Power Devices

- Blocking voltage capability of JFETs comparable to BJTs and MOSFETs.

- JFET on-state losses higher than MOSFETs - technology limitation.

- Switching speeds of normally-on JFET somewhat slower than those of MOSFET - technology limitation.

- BSIT switching times comparable to BJTs - in principle should be faster because of lack of in-line pn junction trapping stored charge at turn-off.

- No second breakdown in normally-on JFETs, similar to MOSFETs.

- BSITs and BSIThy have and possibly limitations.

- JFET-based power devices much less widely used because of normally-on characteristic. This has also slowed research and development efforts in these devices compared to other devices.

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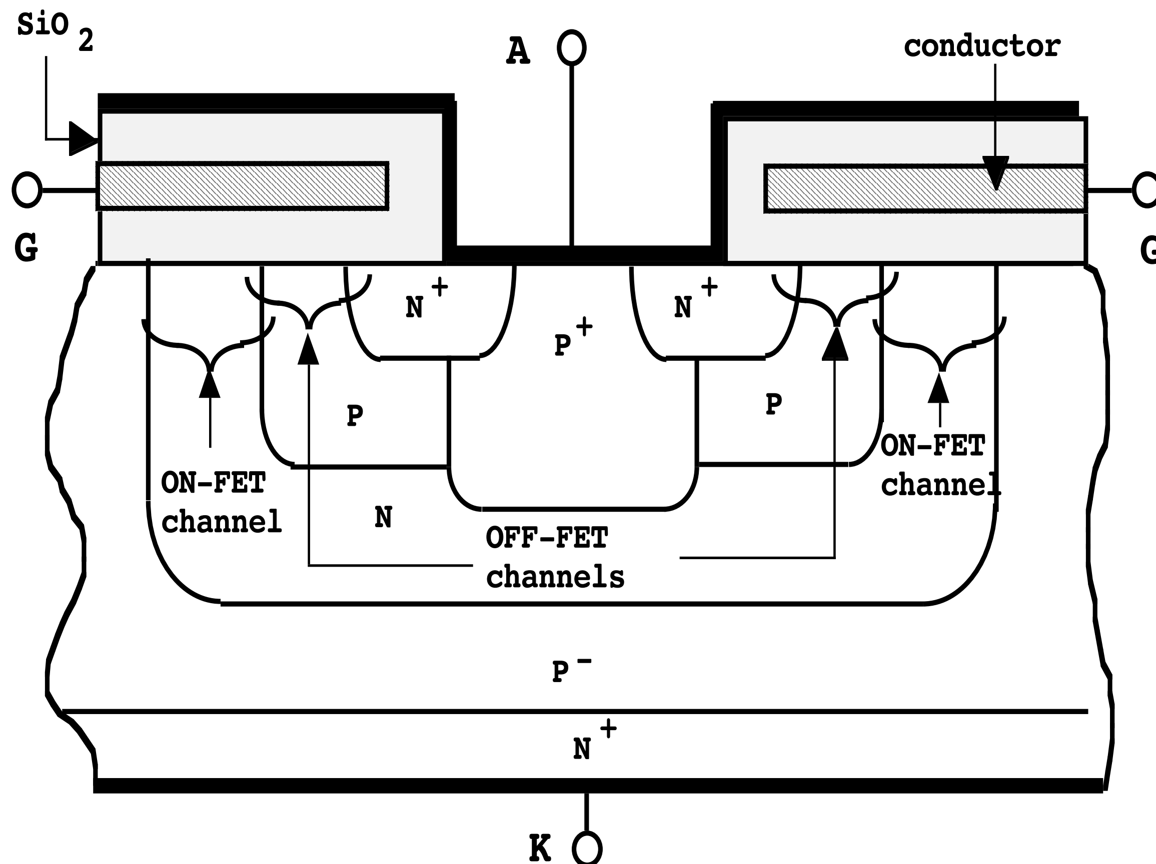
P-MCT (P-type MOS-controlled Thyristor

Unit cell vertical cross-section



- Complete MCT composed of tens of thousands of identical cells connected in parallel.
- P-designation refers to doping of the lightly-doped P^- layer which contains the depletion layer of the blocking junction.
- Note that ON and OFF FETs are positioned at the anode end of the device.

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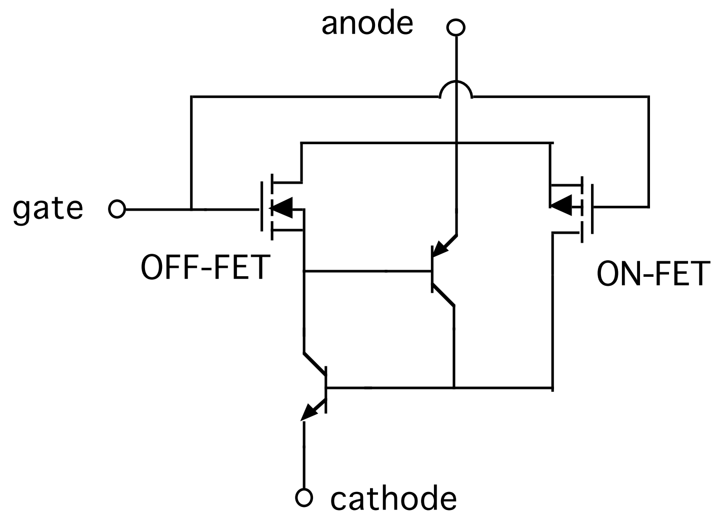
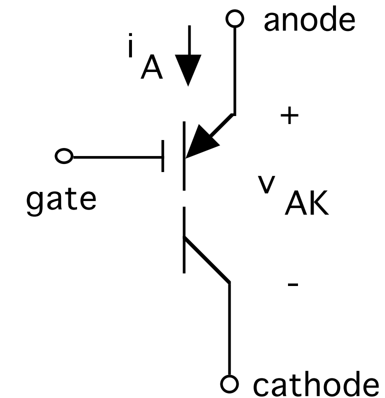
P-MCT Equivalent Circuit & Circuit Symbol

P-MCT equivalent circuit



P-MCT circuit symbol



- P-MCT used with anode grounded.
- Gate-anode voltage is input drive voltage.
- Use P-MCT in circuits with negative voltages.

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N-MCT (N-type MOS-controlled Thyristor

Vertical cross-section of N-MCT unit cell

- N-MCT composed of thousands of cells connected electrically in parallel.
- N-designation refers to the N^- layer which contains the depletion layer of the blocking junction.
- Note that the ON and OFF FETs are positioned at the cathode end of the device.

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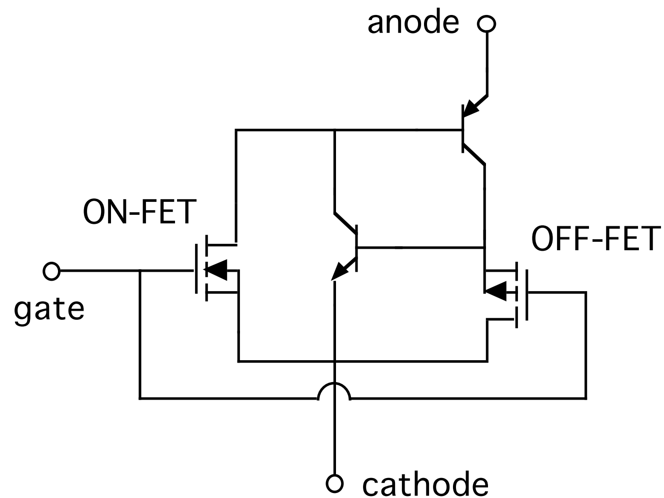
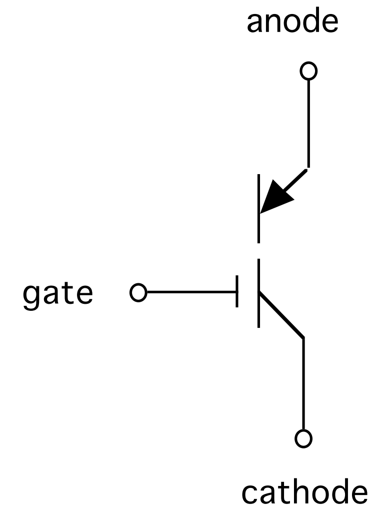
N-MCT Equivalent Circuit & Circuit Symbol

N-MCT equivalent circuit



N-MCT circuit symbol



- N-MCT used with cathode grounded.
- Gate-cathode voltage is input drive voltage.
- Use N-MCT in circuits with positive voltages.

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Gate-controlled Turn-on of MCTs

- Turn on MCT by turning on the ON-FET
  - Positive gate-cathode voltage for N-MCT
  - Negative gate-anode voltage for P-MCT
  - These polarities of gate voltage automatically keep the OFF-FET in cutoff.

- ON-FET delivers base current to the low-gain BJT in the thyristor equivalent circuit and activates that BJT.
  - PNP transistor in the N-MCT
  - NPN transistor in the P-MCT

- Low-gain transistor activates the higher gain transistor and thyristor latches on.

- Once higher gain transistor, which is in parallel with ON-FET is activated, current is shunted from ON-FET to the BJT and the ON-FET carries very little current in the MCT on-state.
  - Only 5-10% of the cells have an ON-FET.
  - Cells are close-packed. Within one excess carreier diffusion length of each other.
  - Adjacent cells without an ON-FET turned on via diffusion of excess carriers from turned-on cell.

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Gate-controlled Turn-off of MCTs

- Turn MCT off by turning on the OFF-FET
  - Negative gate-cathode for the N-MCT
  - Positive gate-anode voltage for the P-MCT
  - These gate voltage polarities automatically keep the ON-FET in cut-off.

- OFF-FET shunts base current away from the higher gain BJT in the thyristor equivalent circuit and forces it to cut-off.
  - NPN transistor in the N-MCT.
  - PNP transistor in the P-MCT.

- Cut-off of higher gain BJT then forces low-gain BJT into cut-off.

- Every MCT cell has an OFF-FET.

- OFF-FET kept activated during entire MCT off-state to insure no inadvertent activation of the thyristor.

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Maximum Controllable Anode Current

- If drain-source voltage of OFF-FET reaches approximately 0.7 V during turn-off, then MCT may remain latched in on-state.
- Higher-gain BJT remains on if OFF-FET voltage drop, which is the base-emitter voltage of the BJT reaches 0.7 volts.
- Thus maximum on-state current that can be turned off by means of gate control.
- P-MCT have approximately three times larger gate-controlled anode current rating than a similar (same size and voltage rating) N-MCT.
- OFF-FET of the P-MCT is an n-channel MOSFET which has three times larger channel mobility than the p-channel OFF-FET of the N-MCT.

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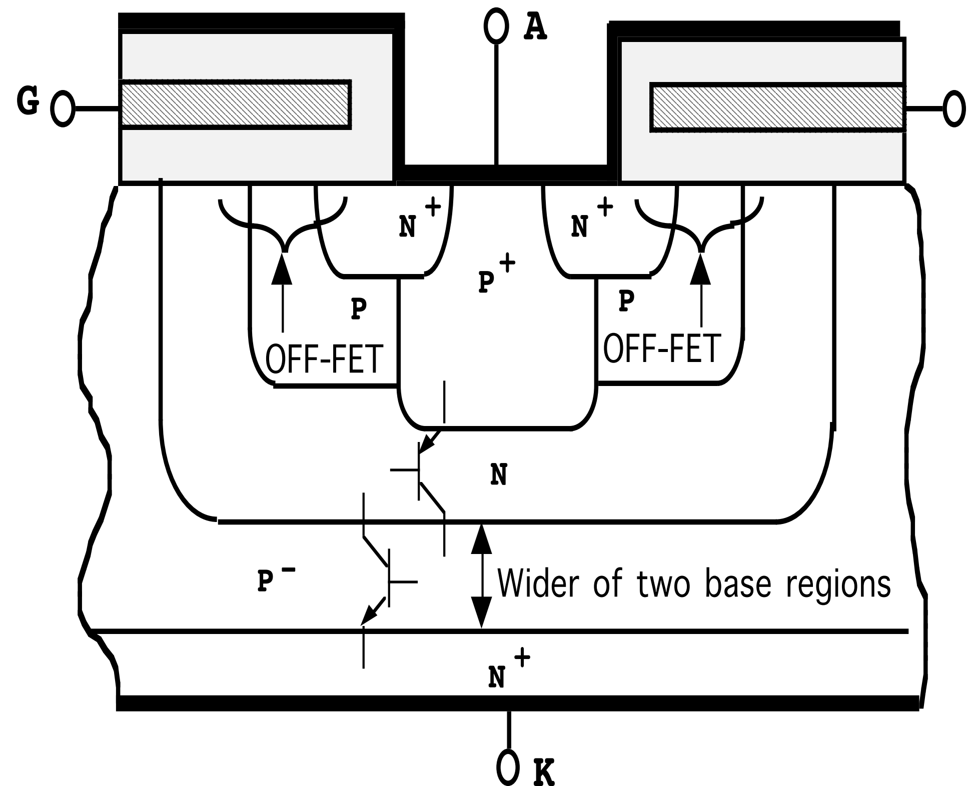
Rationale of OFF-FET Placement

- Turning off the BJT with the larger value of α most effective way to break the latching condition $\alpha_1 + \alpha_2 = 1$
- BJT with the smaller base width has the larger value of α.
  - P-MCT ; PNP BJT has smaller base width
  - N-MCT ; NPN BJT has smaller base width
- OFF-FET put in parallel with base-emitter of larger gain BJT so that OFF-FET shorts out base-emitter when the FET is activated.

P-MCT cross-section showing rationale for OFF-FET placement



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MCT Switching Waveforms

Gate-cathode voltage

V_{Tn}

V_{Tp}

t

Anode-cathode voltage

V_d

t_{fv1}

t_{fv2}

$t_{d,off}$

t_{rv1}

t_{rv2}

t

Anode current

I_o

$t_{d,on}$

t_{ri1}

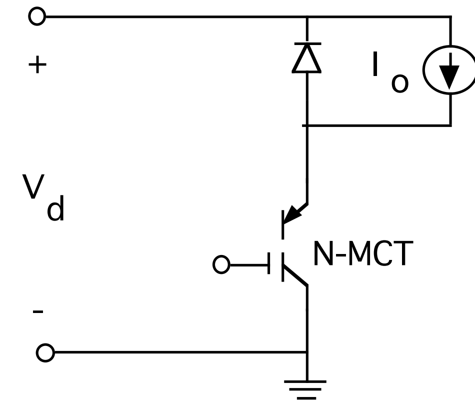
t_{ri2}

t_{fi1}

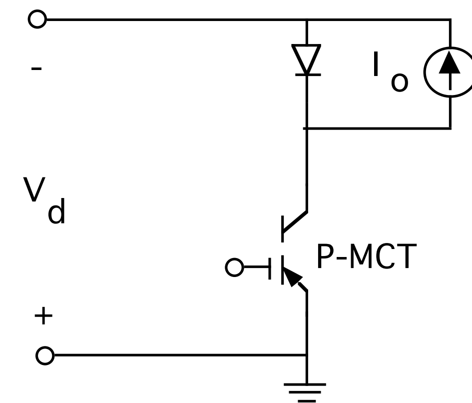
t_{fi2}

t

N-MCT Step-down Converter



P-MCT Step-down Converter



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MCT Turn-on Process

- Turn-on delay time $t_{d,on}$ - time required for gate voltage to reach ON-FET threshold starting from reverse-bias value of $V_{GG,off}$

- Current rise time t_{ri1} and t_{ri2}
  - t_{ri1} ; ON-FET turns on accepting all the current the gate drive voltage will permit. ON-FET in its active region.
  - t_{ri2} ; NPN and PNP BJTs turn on and current shunted away from ON-FET. BJTs and ON-FET in their active regions.

- Voltage fall time t_{fv1} and t_{fv2}
  - t_{fv1} ; BJTs in their active regions so voltage fall initially fast.
  - t_{fv2} ; BJTs in quasi-saturation, so their gain is reduced and rate of voltage fall decreases.
  - At end of voltage fall time interval, BJTs enter hard saturation and MCT is in the on-state.

- Gate-cathode voltage should reach final on-state value in times no longer than a specified maximum value (typically 200 nsec). Insure that all paralleled cells turn on at the same time to minimize current crowding problems.

- Keep gate-cathode at on-state value for the duration of the on-state to minimize likelyhood of inadvertant turn-off of some cells if current is substantially reduced during on-state.

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MCT Turn-off Process

- Turn-off delay time $t_{d,off}$ - time required to turn-off the ON-FET, activate the OFF-FET, and break the latching condition by pulling the BJTs out of hard saturation and into quasi-saturation.
  - Requires removal of substantial amount of stored charge, especially in the base regions of the two BJTs (n_1 and p_2 thyristor layers).

- Voltage rise times t_{rv1} and t_{rv2}
  - t_{rv1} ; time required to remove sufficient stored charge so that BJTs leave quasi-saturation and enter active region and blocking junction (J_2) becomes reverse-biased.
  - t_{rv2} ; BJTs in active region and their larger gain causes anode voltage to rapidly complete growth to power supply voltage V_d

- Current fall time t_{fi1} and t_{fi2}
  - t_{fi1} ; Initial rapid fall in current until high gain BJT (NPN BJT in the P-MCT equivalent circuit) goes into cutoff.
  - t_{fi2} ; stored charge still remaining in base (drift region of thyristor) of the low-gain BJT removed in this interval. The open-base nature of the turn-off casuses longer time interval giving a "tail" to the anode current decay.

- Gate-cathode voltage kept at off-state value during entire off-state interval to prevent accidental turn-on.

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MCT Operating Limitations

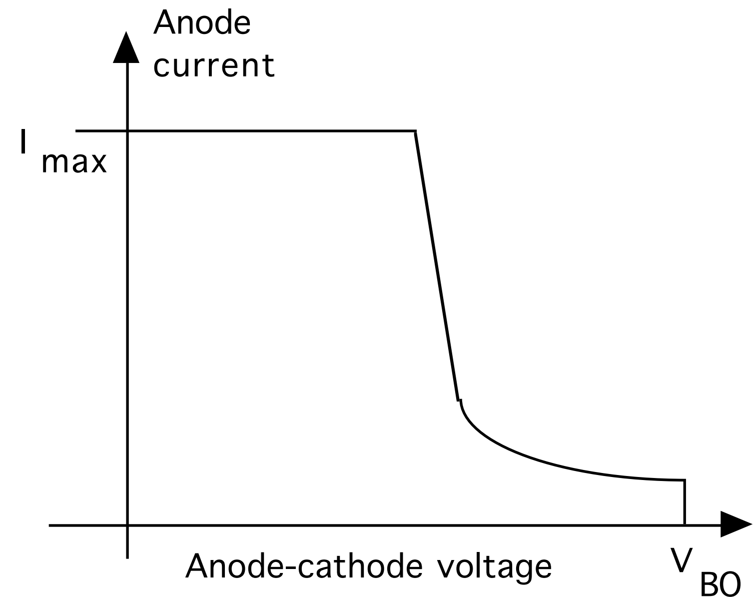
- I_{max} set by maximum controllable anode current. Presently available devices have 50-100 A ratings.

- V_{max} set by either breakover voltage of thyristor section or breakdown rating of the OFF-FET. Presently available devices rated at 600 V. 1000-2000 v devices prototyped.

- $\frac{dv_{DS}}{dt}$ limited by mechanisms identical to those in thyristors. Presently available devices rated at 500-1000 V/sec.

- $\frac{di_D}{dt}$ limited by potential current crowding problems. Presently available devices rated at 500 A/sec.

- MCT safe operating area. Very conservatively estimated.



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High Voltage (Power) Integrated Circuits

- Three classes of power ICs

  1. Smart power or smart/intelligent switches
     - Vertical power devices with on-chip sense and protective features and possibly drive and control circuits

  2. High voltage integrated circuits (HVICs)
     - Conventional ICs using low voltage devices for control and drive circuits and lateral high voltage power devices

  3. Discrete modules
     - Multiple chips mounted on a common substrate. Separate chips for drive, control, and power switch and possibly other functions.

- PIC rationale

  - Lower costs

  - Increased functionality

  - Higher reliability

  - Less circuit/system complexity

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Issues Facing PIC Commercialization

- Technical issues
  - Electrical isolation of high voltage devices from low voltage components
  - Thermal management - power devices generally operate at higher temperatures than low power devices/circuits.
  - On-chip interconnections with HV conductor runs over low voltage devices/regions.
  - Fabrication process should provide full range of devices and components - BJTs, MOSFETs, diodes, resistors, capacitors, etc.
- Economic issues
  - High up-front development costs
  - Relative cost of the three classes of PICs
  - Need for high volume applications to cover development expenses.

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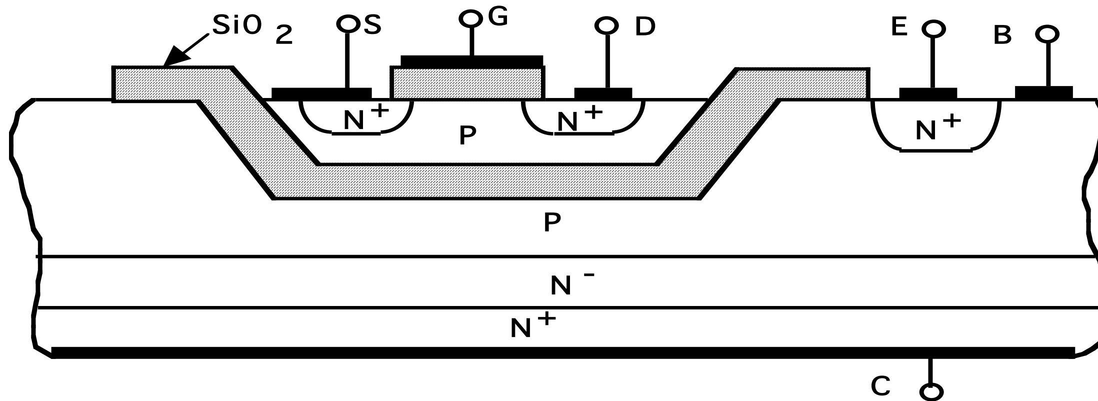
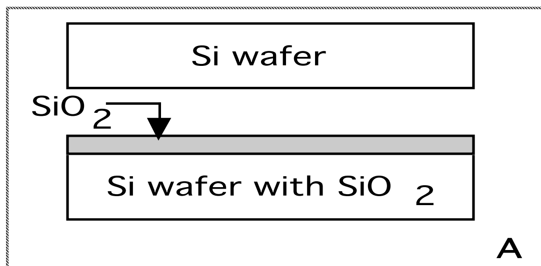
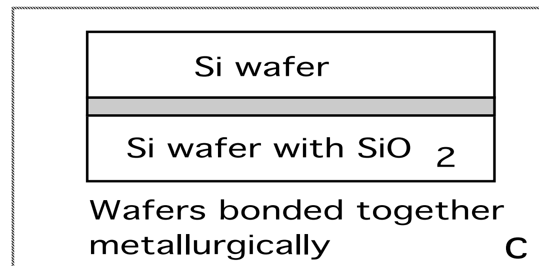
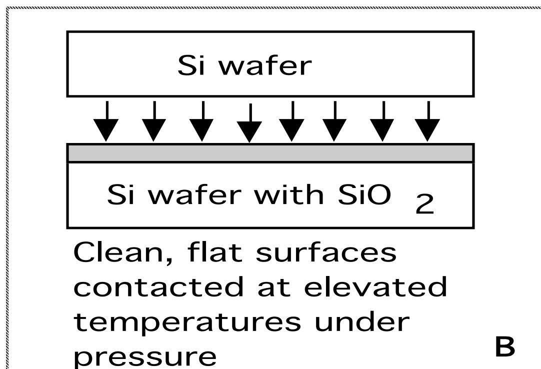
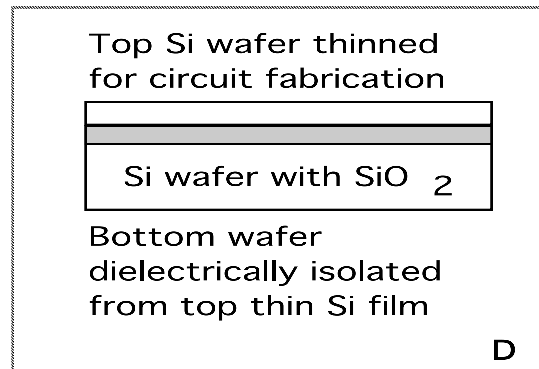
Dielectric Isolation











- Dielectrically isolated tubs - SiO_2 isolation and silicon thin film overgrowth.

- Wafer bonding and subsequent wafer thinning.

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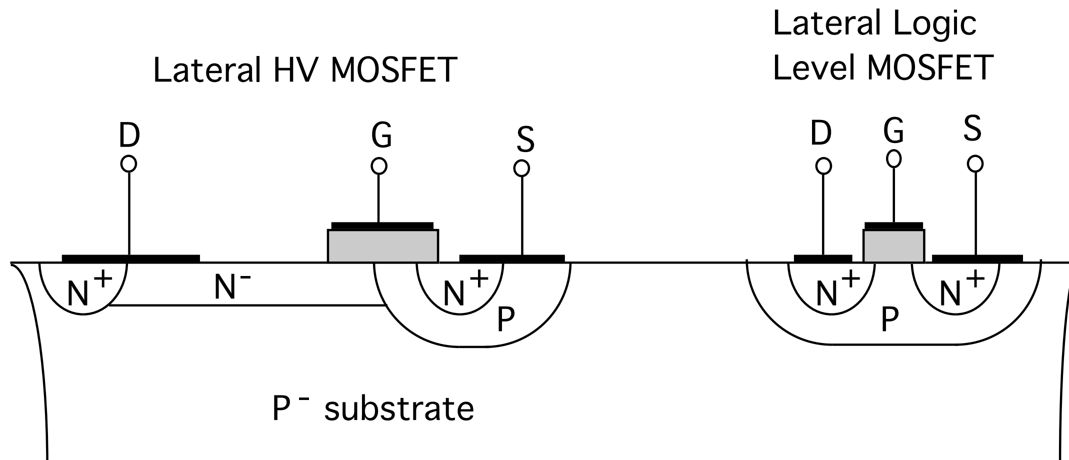
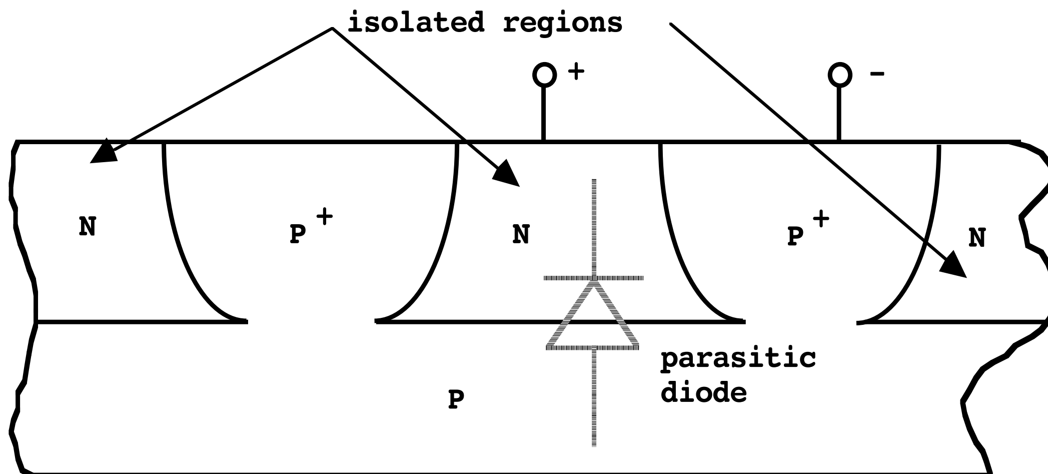
Self-Isolation and Junction Isolation



- Self-isolation - only feasible with MOSFET devices.



- Junction isolation.

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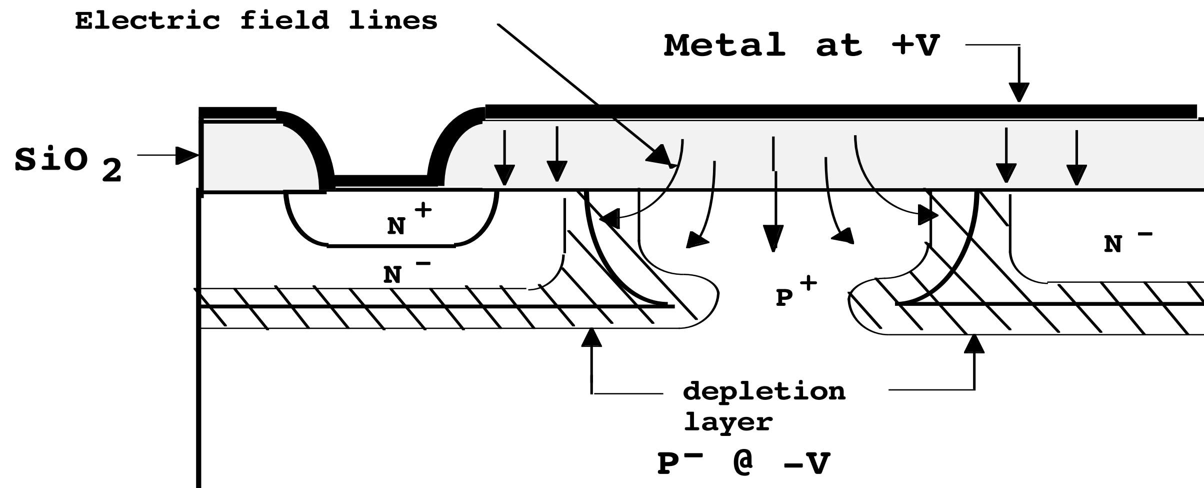
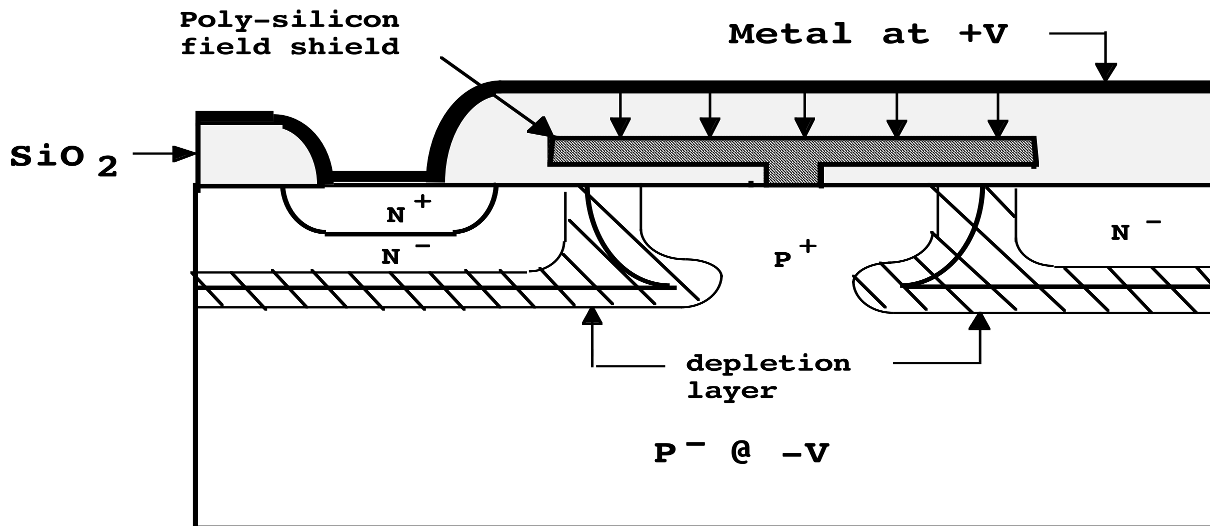
High-Voltage Low-Voltage Cross-overs



- Field-crowding and premature breakdown.



- Use of field shields to minimize field crowding problems at HV/LV cross-overs.

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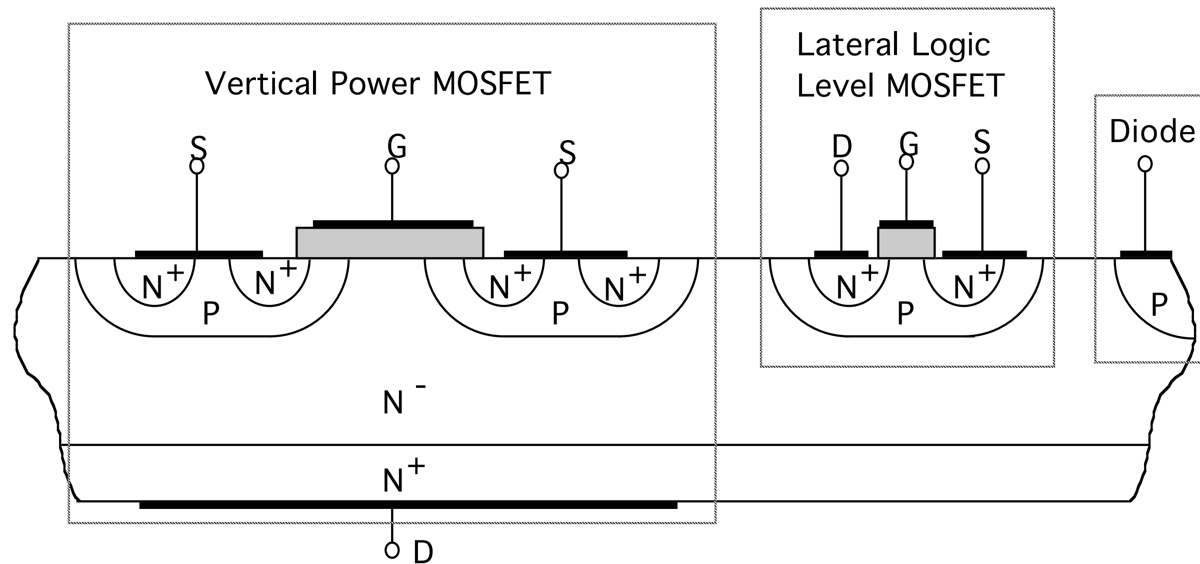
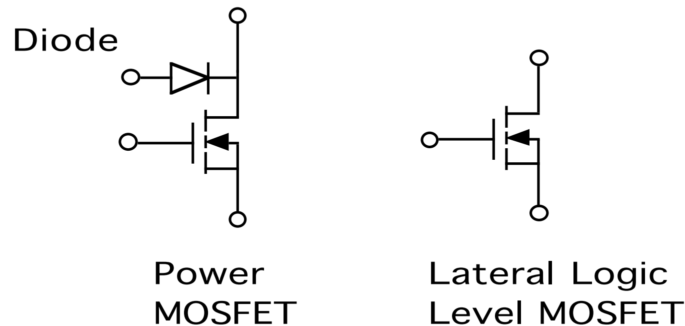
Smart or Intelligent Switch Using MOSFETs



- Cross-sectional diagram of switch.

- Circuit diagram



- Add additional components on vertical MOSFET wafer as long as no major process changes required.

- PN junction formed from N^- drift region and P-body region always reverse-biased if drain of power MOSFET positive respect to source. Provides electrical isolation of the two MOSFETs.

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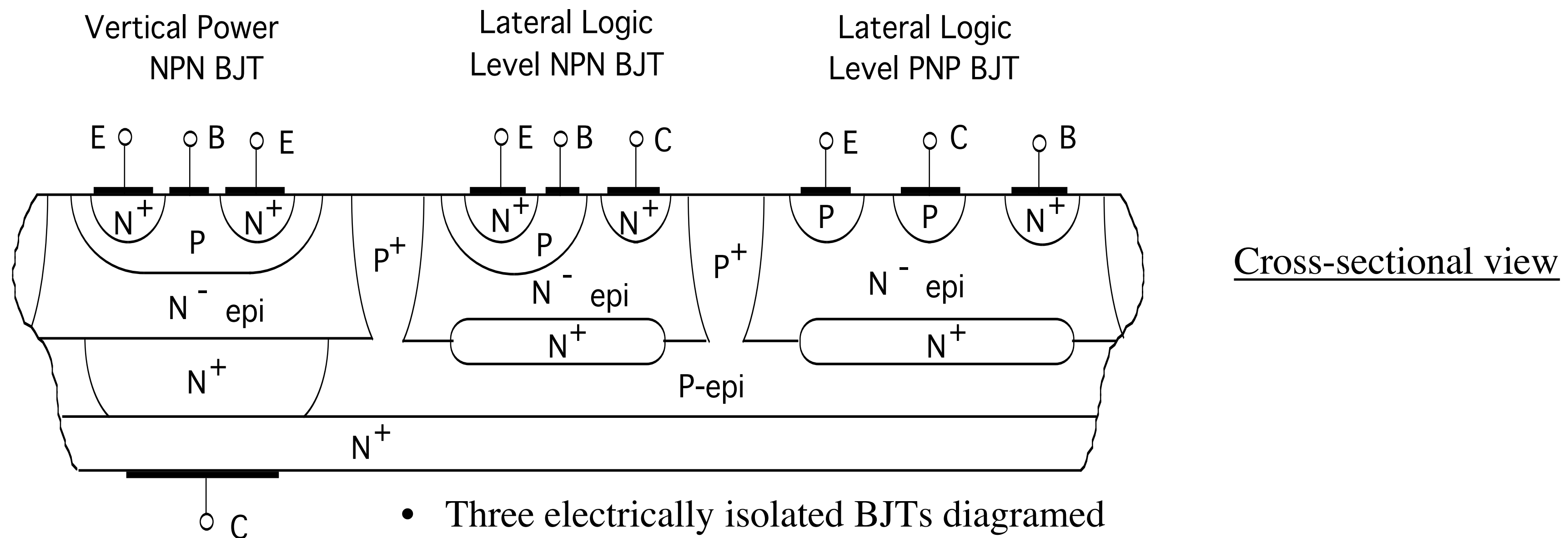
Smart Power Switch Using BJTs



Cross-sectional view

- Three electrically isolated BJTs diagramed
  - PN junction isolation via P-epi and top-side P^+ diffusion
- Double epitaxial process squence
  - P-epi grown on N^+ substrate
  - N^+ buried layer diffused in next
  - N-epi for drift region grown over P-epi
  - P^+ isolation diffusions to P-epi
  - Diffusion for base and emitters of BJTs

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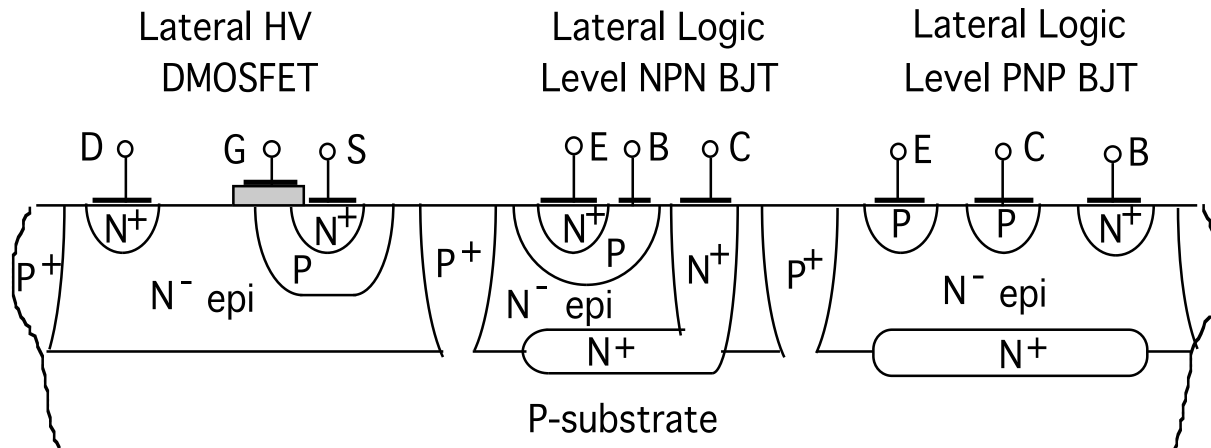
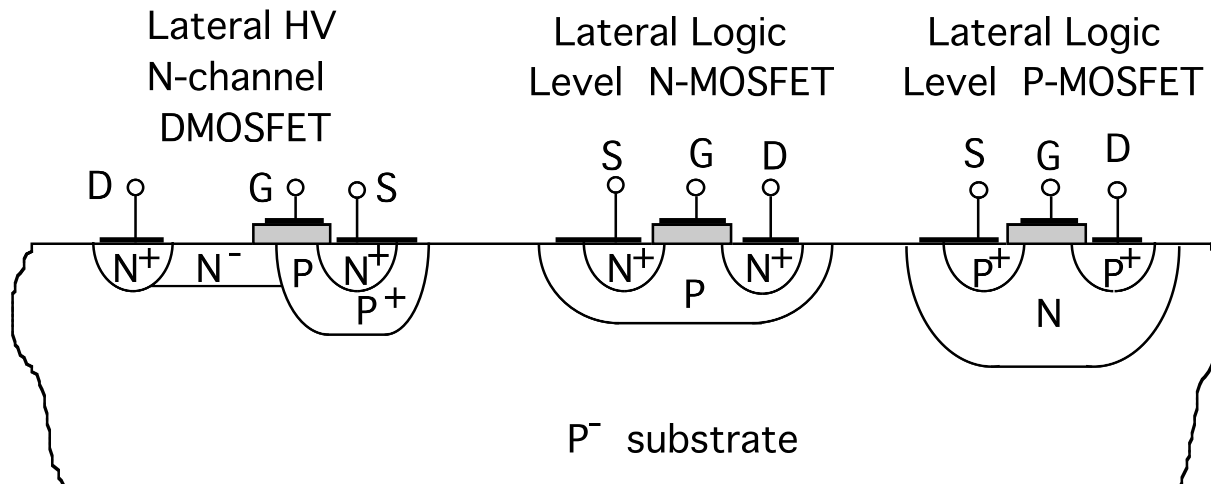
High Voltage Integrated Circuits (HVICs)



HVIC using junction isolation



HVIC using self-isolation

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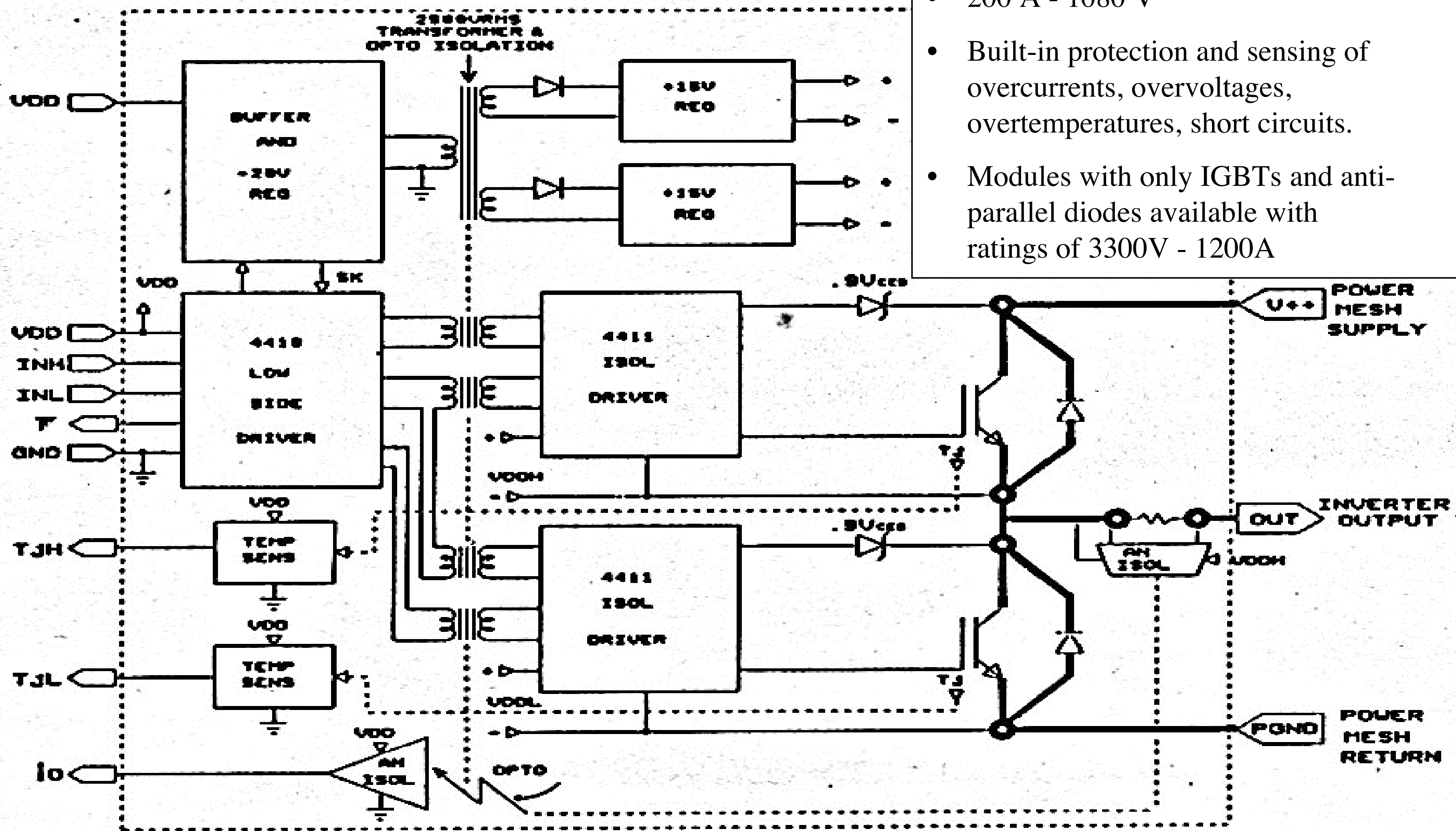
Discrete Module Example - IXYS I3M IGBT Module

- Intelligent isolated half-bridge
- 200 A - 1080 V
- Built-in protection and sensing of overcurrents, overvoltages, overtemperatures, short circuits.
- Modules with only IGBTs and anti-parallel diodes available with ratings of 3300V - 1200A



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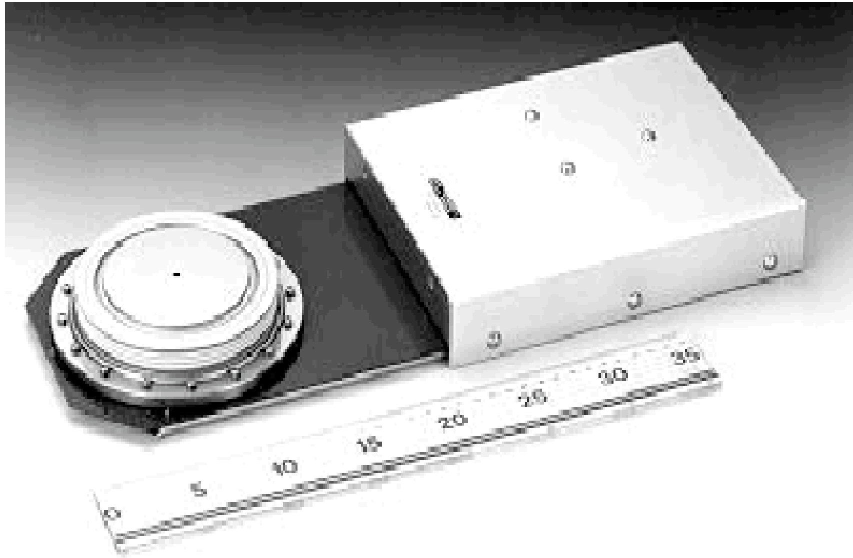
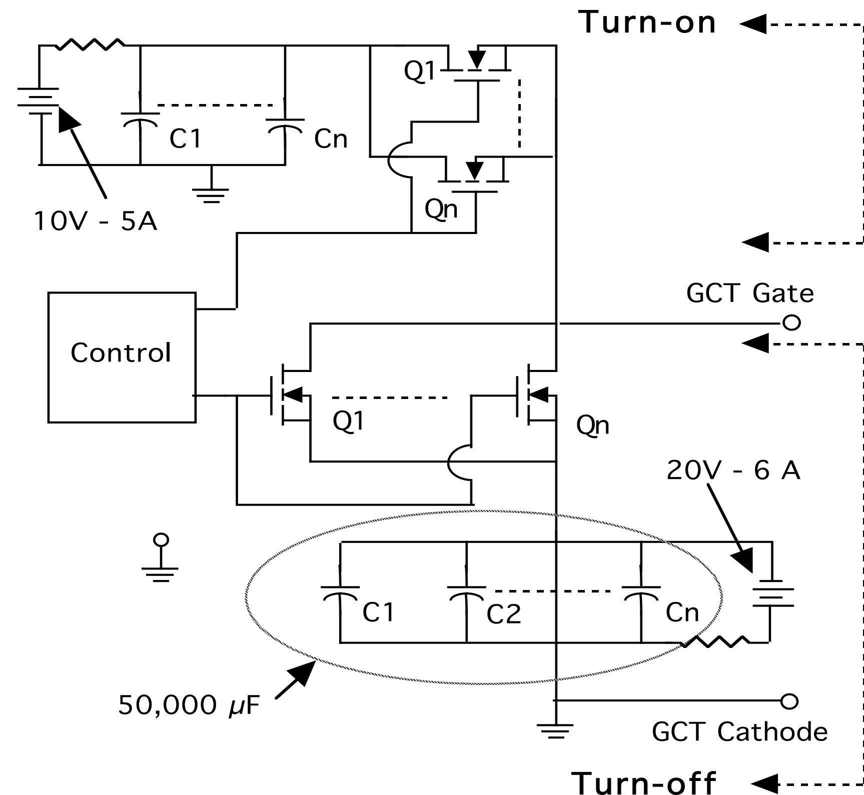
IGCT - Integrated Gate Commutated Thyristor





- Specially designed GTO with low inductance gate drive circuit
- Ratings
  - Blocking voltage - 4500V
  - Controllable on-state current - 4000A
  - Average fwd current - 1200A
  - Switching times - 10μsec

- Approximate gate drive circuit
  - Ion ≈ 500 A 10μsec
  - Ioff - full forward current 10 usec
- Very low series inductance - 3 nH

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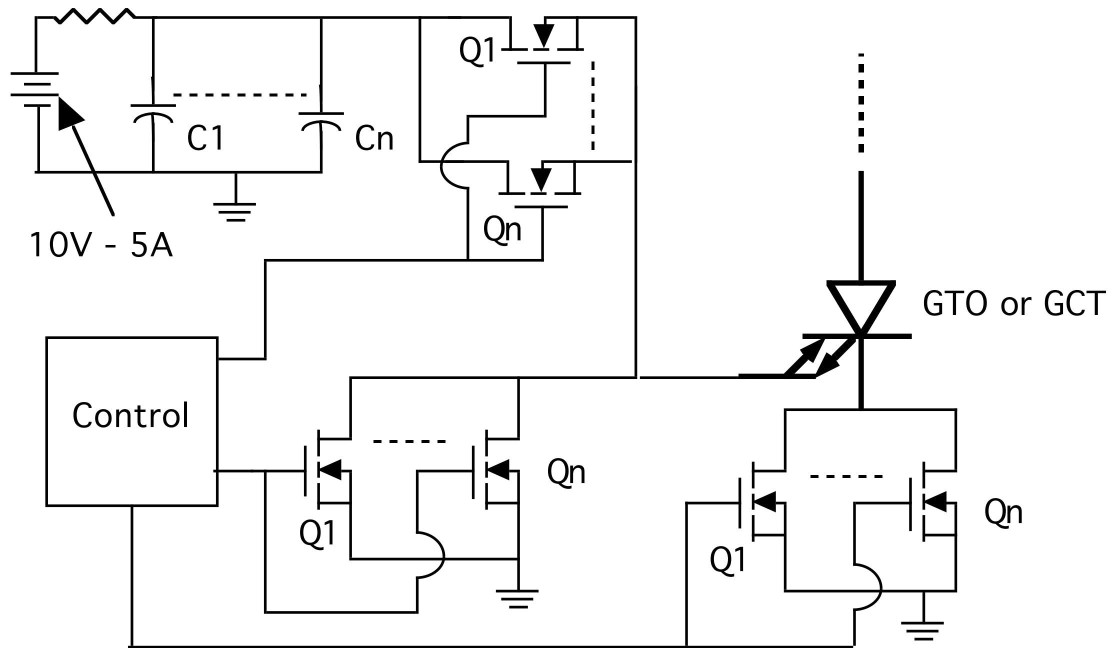
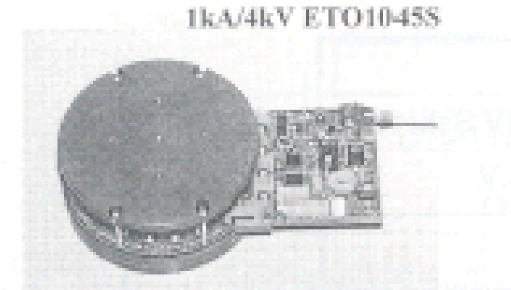
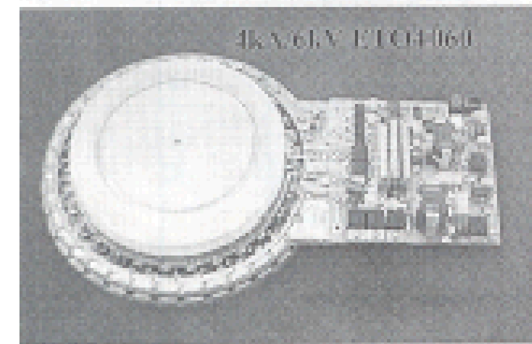
Emitter Turn-off Thyristor







- Performance similar to IGCTs
- Advantages over IGCTs
  - Simpler drive circuit
  - Easier to parallel - MOSFETs in series with GTO have positive temperature coefficient
  - Series MOSFETs can be used for overcurrent sensing

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Economic Considerations in PIC Availability

- PIC development costs (exclusive of production costs)
  - Discrete modules have lower development costs
  - Larger development costs for smart switches and HVICs

- Production costs (exclusive of development costs) of smart switches and HVICs lower than for discrete modules.

- Reliability of smart switches and HVICs better than discrete modules.
  - Greater flexibility/functionality in discrete modules
  - Wider range of components - magnetics, optocouplers

- PICs will be developed for high volume applications
  - Automotive electronics
  - Telecommunications
  - Power supplies
  - Office automation equipment
  - Motor drives
  - Flourescent lighting ballasts

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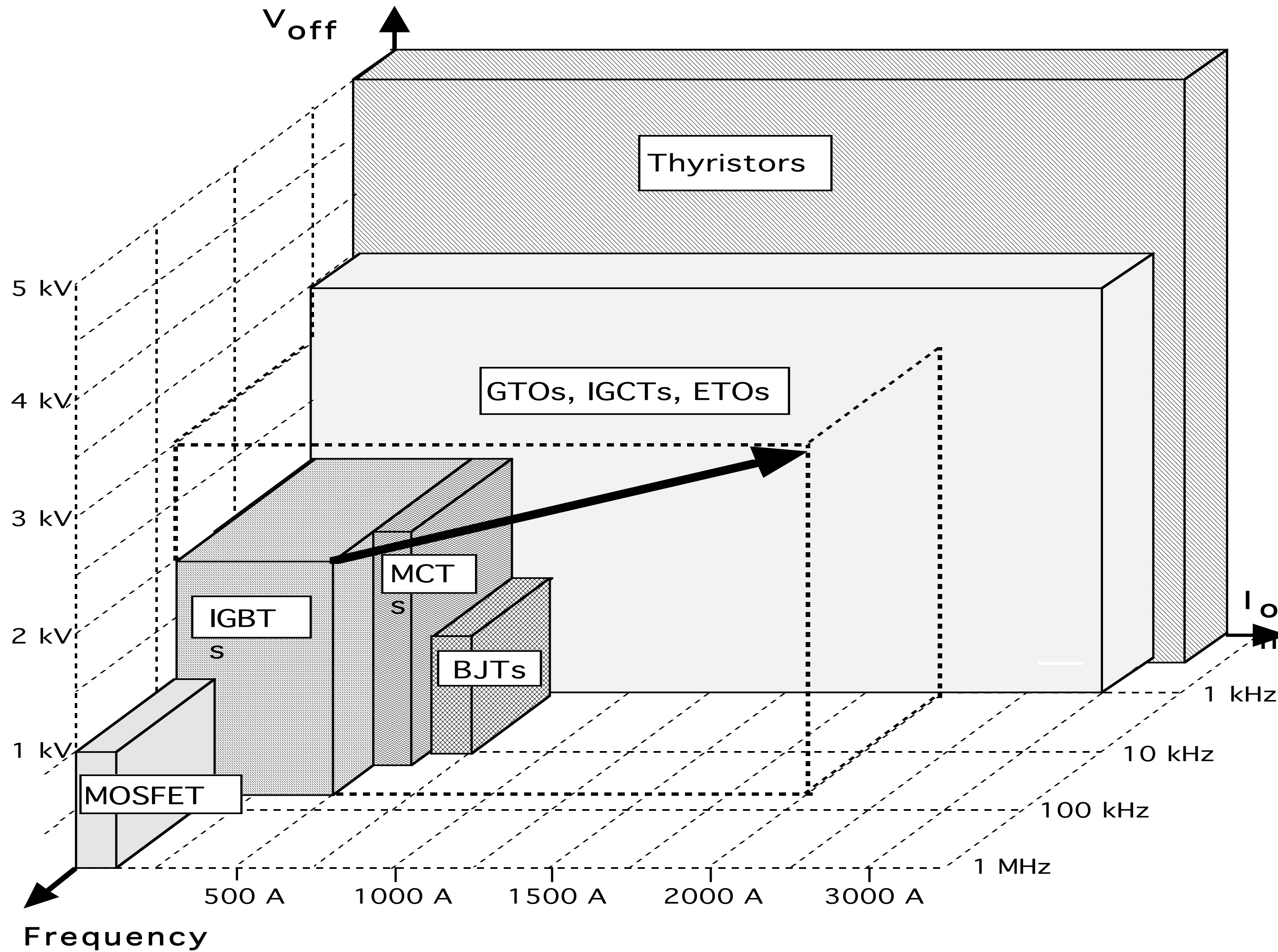
Summary of Silicon Power Device Capabilities



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New Semiconductor Materials for Power Devices

- Silicon not optimum material for power devices

- Gallium arsenide promising material
  - Higher electron mobilities (factor of about 5-6) - faster switching speeds and lower on-state losses
  - Larger band-gap E_g - higher operating temperatures

- Silicon carbide another promising materials
  - Larger bandgap than silicon or GaAs
  - Mobilities comparable to Si
  - Significantly larger breakdown field strength
  - Larger thermal conductivity than Si or GaAs

- Diamond potentially the best materials for power devices

  - Largest bandgap
  - Largest breakdown field strength
  - Largest thermal conductivity
  - Larger mobilities than silicon but less than GaAs

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Properties of Important Semiconductor Materials

Property	Si	GaAs	3C-SiC	6H-SiC	Diamond
Bandgap @ 300 K [ev]	1.12	1.43	2.2	2.9	5.5
Relative dielectric constant	11.8	12.8	9.7	10	5.5
Saturated drift velocity [cm/sec]	$1x10^7$	$2x10^7$	$2.5x10^7$	$2.5x10^7$	$2.7x10^7$
Thermal conductivity [Watts/cm- C]	1.5	0.5	5.0	5.0	20
Maximum operating temperature [K]	300	460	873	1240	1100
Intrinsic carrier density [cm^{-3}] @ 25 C	10^{10}	10^7	-	-	-
Melting temperature [C]	1415	1238	Sublime >1800	Sublime >1800	Phase change
Electron mobility @ 300 K [cm^2/V-sec]	1400	8500	1000	600	2200
Breakdown electric field [V/cm]	$2\text{-}3x10^5$	$4x10^5$	$2x10^6$	$2x10^6$	$1x10^7$

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On-State Resistance Comparison with Different Materials

- Specific drift region resistance of majority carrier device

  - $R_{on} \bullet A \approx \dfrac{4 \cdot q \cdot (BV_{BD})^2}{\epsilon \cdot \mu_n \cdot (E_{BD})^3}$

  - Normalize to silicon - assume identical areas and breakdown voltages

$$\frac{R_{on}(x) \cdot A}{R_{on}(Si) \cdot A} = \text{resistance ratio} = \frac{\epsilon_{Si} \cdot \mu_{Si}}{\epsilon_x \cdot \mu_x} \left[\frac{E_{BD,Si}}{E_{BD,x}}\right]^3$$

  - Numerical comparison

Material	Resistance Ratio
Si	1
GaAs	6.4×10^{-2}
SiC	9.6×10^{-3}
Diamond	3.7×10^{-5}

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Material Comparison: PN Junction Diode Parameters

- Approximate design formulas for doping density and drift region length of HV pn junctions

  - Based on step junction $P^+N^-N^+$ structure

  - N_d = drift region doping level $\approx \frac{e"[E_{BD}]^2}{2"q"BV_{BD}}$

  - W_d = drift region length $\approx \frac{2"BV_{BD}}{E_{BD}}$

- Numerical comparison - 1000 V breakdown rating

Material	$\mathbf{N_d}$		$\mathbf{W_d}$
Si	1.3×10^{14}	cm^{-3}	67 μm
GaAs	5.7×10^{14}		50
SiC	1.1×10^{16}		10
Diamond	1.5×10^{17}		2

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Material Comparison: Carrier Lifetime Requirements

- Drift region carrier lifetime required for 1000 V pn junction diode
  - Approximate design formula based on step junction

$$\tau \approx \frac{q \cdot W_d^2}{k \cdot T \cdot \mu_n} = \frac{4 \cdot q \cdot [BV_{BD}]^2}{k \cdot T \cdot \mu_n \cdot [E_{BD}]^2}$$

- Numerical comparison

Material	**Lifetime**
Si	1.2 μsec
GaAs	0.11 μsec
SiC	40 nsec
Diamond	7 nsec

  - Shorter carrier lifetimes mean faster switching minority carrier devices such as BJTs, pn junction diodes, IGBTs, etc.

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Recent Advances/Benchmarks

- Gallium arsenide
  - 600V GaAs Schottky diodes announced by Motorola. 250V available from IXYS
  - 3" GaAs wafers available
- Silicon carbide
  - 3" wafers available from Cree Research - expensive
  - 600V -6A Schottky diodes available commercially - Infineon Technologies AG (Siemens spinoff)
  - Controlled switches also demonstrated
    - 1800V - 3A BJT with beta of 20
    - 3100V - 12A GTO
- Diamond
  - Polycrystalline diamond films of several micron thickness grown over large (square centimeters) areas
  - Simple device structures demonstrated in diamond films.
    - PN junctions
    - Schottky diodes

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Projections

- GaAs
  - Devices such as Schottky diodes which are preesently at or near commercial introduction will become available and used.
  - GaAs devices offer only incremental improvements in performance over Si devices compared to SiC or diamond.
  - Broad introduction of several types of GaAs-based power devices unlikely.
- SiC
  - Rapid advances in SiC device technology
  - Spurred by the great potential improvement in SiC devices compared to Si devices.
  - Commercially available SiC power devices within 5-10 years.
- Diamond
  - Research concentrated in improving materials technology.
    - Growth of single crystal material
    - Ancilliary materials issues - ohmic contacts, dopants, etc.
  - No commercially available diamond-based power devices in the forseeable future (next 10-20 years).

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Lecture Notes

Snubber Circuits

Outline

A. Overview of Snubber Circuits

B. Diode Snubbers

C. Turn-off Snubbers

D. Overvoltage Snubbers

E. Turn-on Snubbers

F. Thyristor Snubbers

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Overview of Snubber Circuits for Hard-Switched Converters

Function: Protect semiconductor devices by:

- Limiting device voltages during turn-off transients
- Limiting device currents during turn-on transients
- Limiting the rate-of-rise (di/dt) of currents through the semiconductor device at device turn-on
- Limiting the rate-of-rise (dv/dt) of voltages across the semiconductor device at device turn-off
- Shaping the switching trajectory of the device as it turns on/off

Types of Snubber Circuits

1. Unpolarized series R-C snubbers
   - Used to protect diodes and thyristors
2. Polarized R-C snubbers
   - Used as turn-off snubbers to shape the turn-on switching trajectory of controlled switches.
   - Used as overvoltage snubbers to clamp voltages applied to controlled switches to safe values.
   - Limit dv/dt during device turn-off
3. Polarized L-R snubbers
   - Used as turn-on snubbers to shape the turn-off switching trajectory of controlled switches.
   - Limit di/dt during device turn-on

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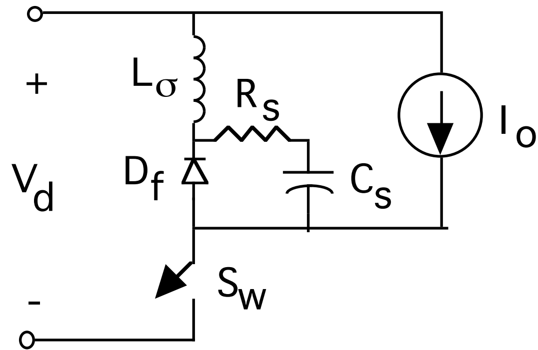
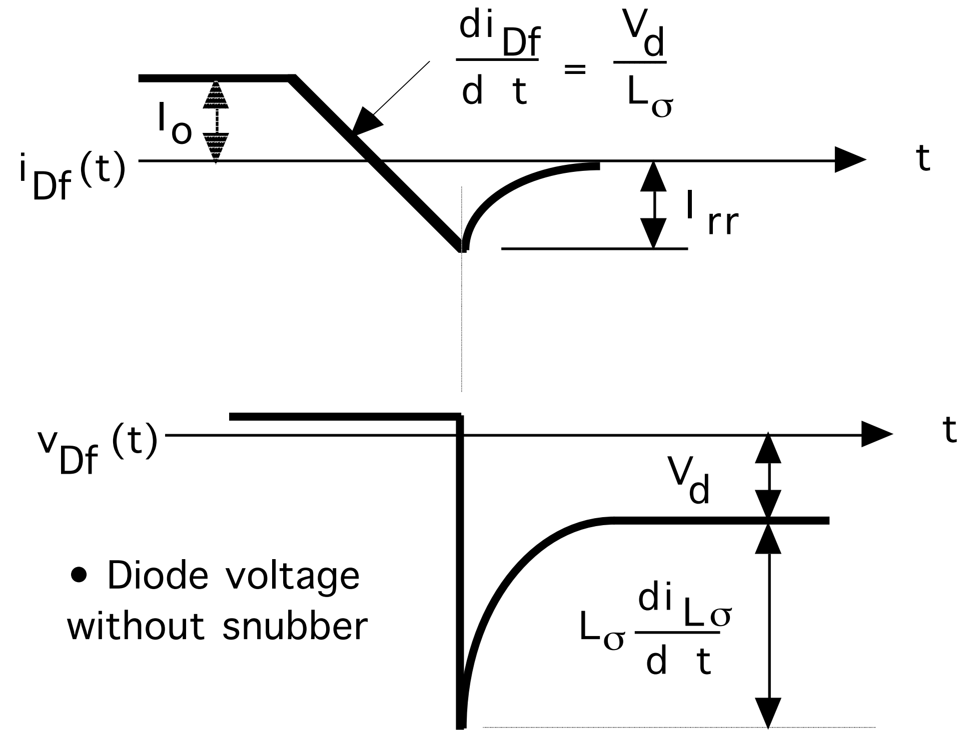
Need for Diode Snubber Circuit





- L_σ = stray inductance
- S_w closes at t = 0
- R_s - C_s = snubber circuit

- Diode breakdown if $V_d + L_\sigma \frac{di_{L\sigma}}{dt} > BV_{BD}$

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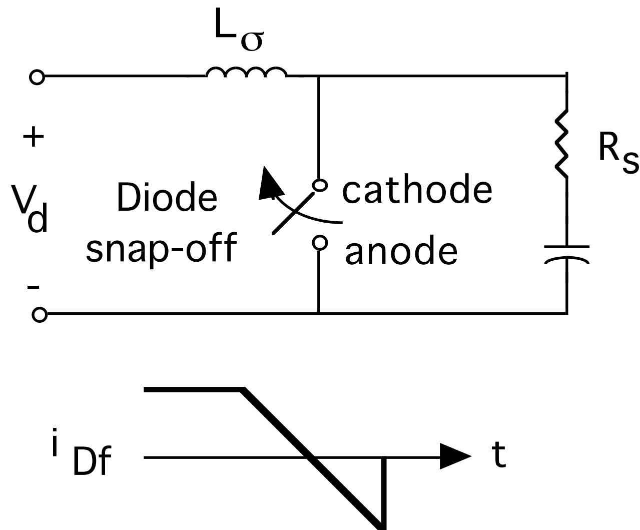
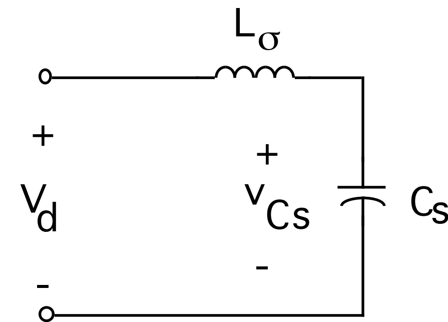
Equivalent Circuits for Diode Snubber



- Worst case assumption- diode snaps off instantaneously at end of diode recovery

- Simplified snubber - the capacitive snubber



- $R_s = 0$
- $v_{Cs} = -v_{Df}$

- Governing equation - $\frac{d^2 v_{Cs}}{dt^2} + \frac{v_{Cs}}{L_\sigma C_s} = \frac{V_d}{! \, L_\sigma C_s}$

- Boundary conditions - $v_{Cs}(0^+) = 0$ and $i_{L\sigma}(0^+) = I_{rr}$

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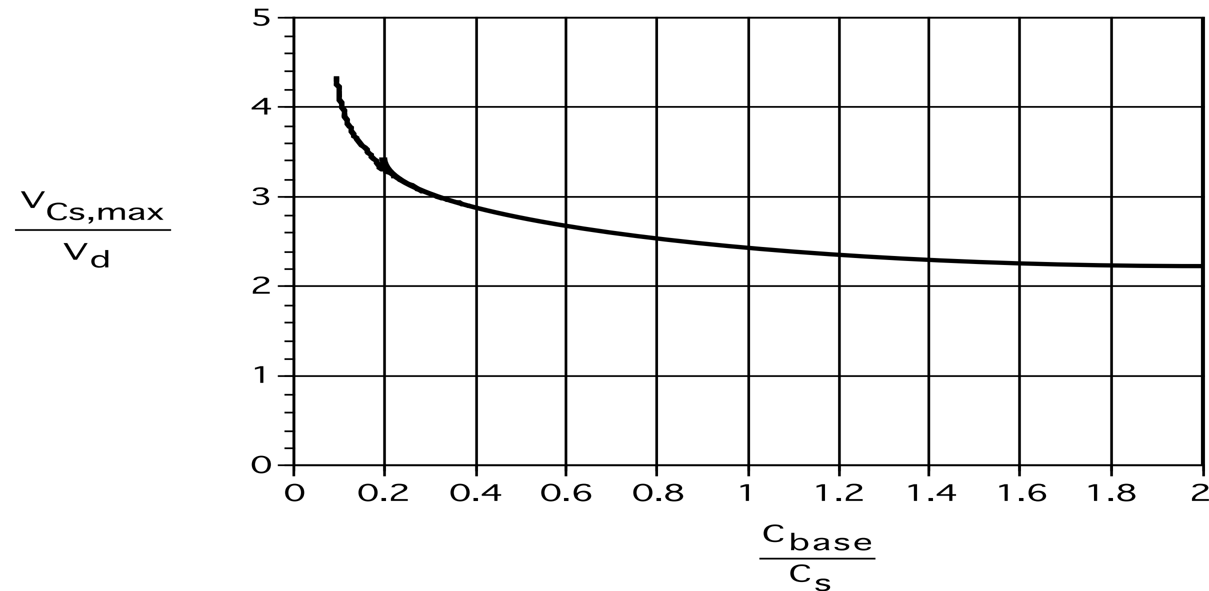
Performance of Capacitive Snubber

- $v_{Cs}(t) = V_d - V_d \cos(\omega_o t) + V_d \sqrt{\frac{C_{base}}{C_s}} \sin(\omega_o t)$

- $\omega_o = \frac{1}{\sqrt{L_\sigma C_s}}$; $C_{base} = L_\sigma \left[\frac{I_{rr}}{V_d}\right]^2$

- $V_{cs,max} = V_d \left\{ 1 + \sqrt{1 + \frac{C_{base}}{C_s}} \right\}$



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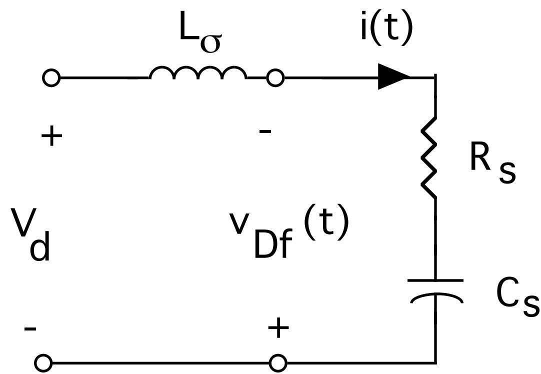
Effect of Adding Snubber Resistance

Snubber Equivalent Circuit



- Governing equation $L_\sigma \frac{d^2 i}{dt^2} + R_s \frac{di}{dt} + \frac{i}{C_s} = 0$

- Boundary conditions

  $i(0^+) = I_{rr}$ and $\frac{di(0^+)}{dt} = \frac{V_d\, -\, I_{rr}R_s}{L_\sigma}$

Diode voltage as a function of time

$$\frac{V_{df}}{V_d}(t) = -1 - \frac{e^{-\alpha t}}{\sqrt{\eta}\,\cos(\phi)} \sin(\omega_a t - \phi + \zeta) \quad ; \quad R_s \leq 2\, R_b$$

$$\omega_a = \omega_o \sqrt{1 -\, (\alpha/\,\omega_o)^2} \;;\; \alpha = \frac{R_s}{2\,L_\sigma} \;;\; \omega_o = \frac{1}{\sqrt{L_\sigma C_s}} \;;\; \phi = \tan^{-1}\left[\frac{(2-x)\sqrt{\eta}}{\sqrt{4\,-\,\eta x^2}}\right]$$

$$\eta = \frac{C_s}{C_b} \;;\; x = \frac{R_s}{R_b} \;;\; R_b = \frac{V_d}{I_{rr}} \;;\; C_b = \frac{L_\sigma\,[I_{rr}]^2}{V_d^{\,2}} \;;\; \zeta = \tan^{-1}(\alpha/\omega_a)$$

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Performance of R-C Snubber

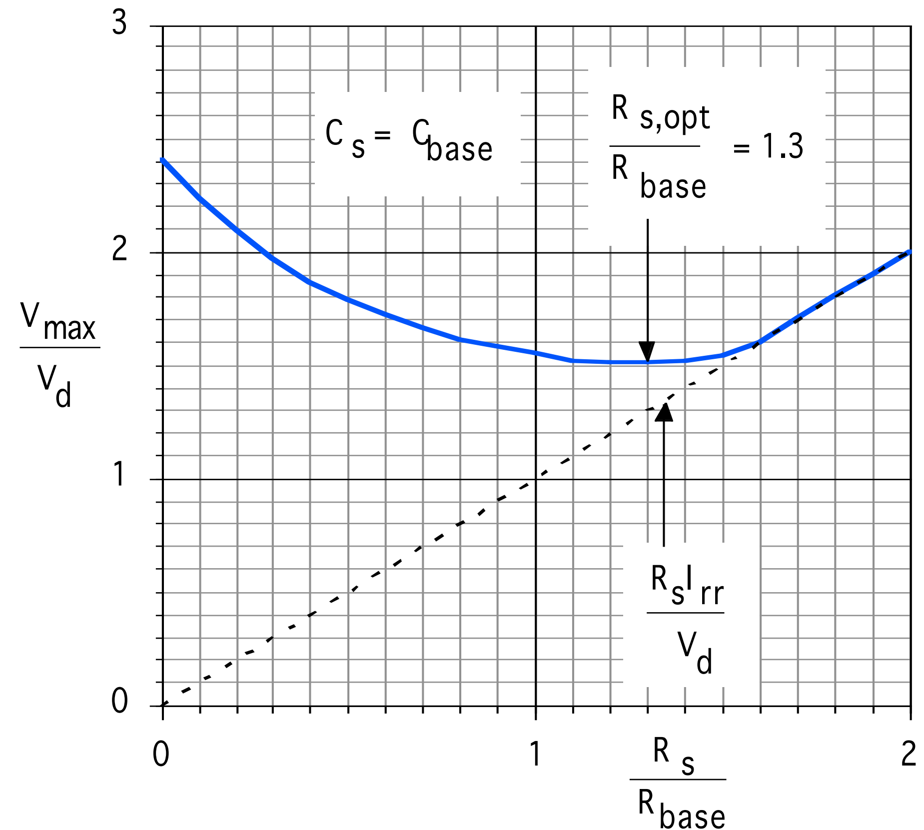
- At $t = t_m$ $v_{Df}(t) = V_{max}$

- $t_m = \dfrac{\tan^{-1}(\omega_a/\alpha)}{\omega_a} + \dfrac{\phi!\ -!\ \xi}{\omega_a} \geq 0$

- $\dfrac{V_{max}}{V_d} = 1 + \sqrt{1!\ +!\ \eta^{-1!}\ -!\ x}\ \exp(-\alpha t_m)$

- $\eta = \dfrac{C_s}{C_{base}}$ and $x = \dfrac{R_s}{R_{base}}$

- $C_{base} = \dfrac{L_s!\ I_{rr}^2}{V_d^2}$ and $R_{base} = \dfrac{V_d}{I_{rr}}$



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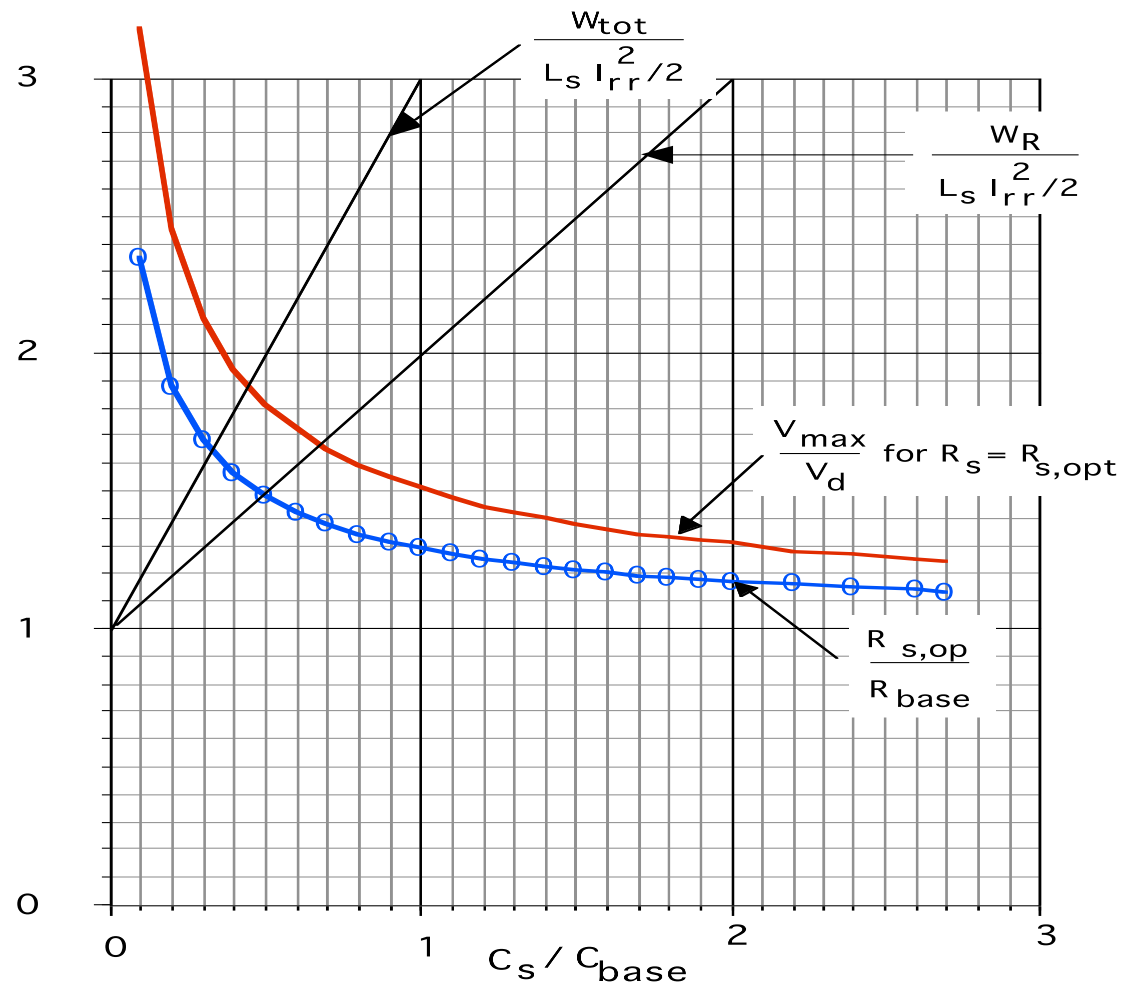
Diode Snubber Design Nomogram



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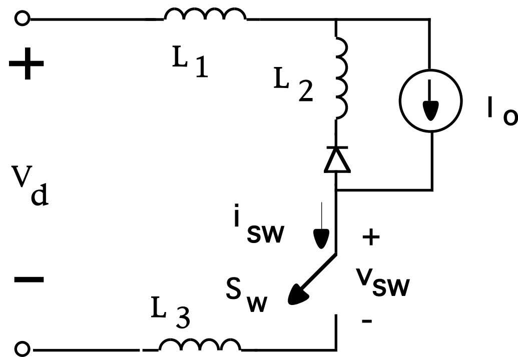
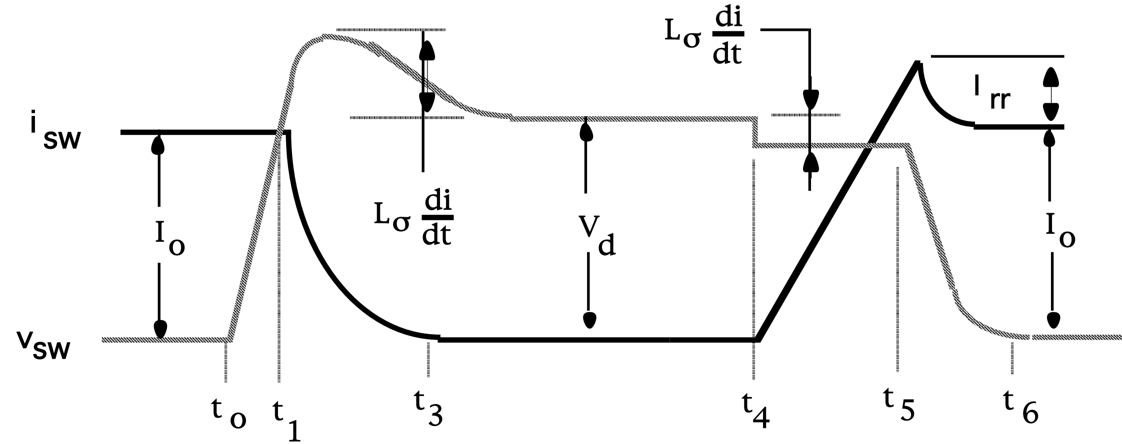
Need for Snubbers with Controlled Switches

Step-down converter

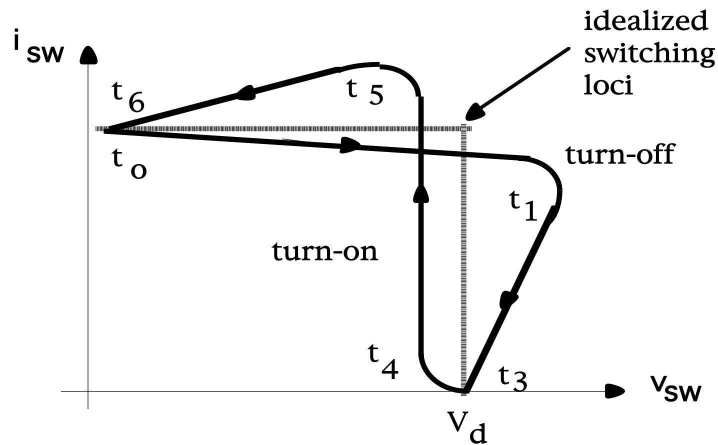


Switch current and voltage waveforms



- L_1 , L_2, L_3 = stray inductances
- $L\sigma = L_1 + L_2 + L_3$

Switching trajectory of switch



- Overvoltage at turn-off due to stray inductance
- Overcurrent at turn-on due to diode reverse recovery

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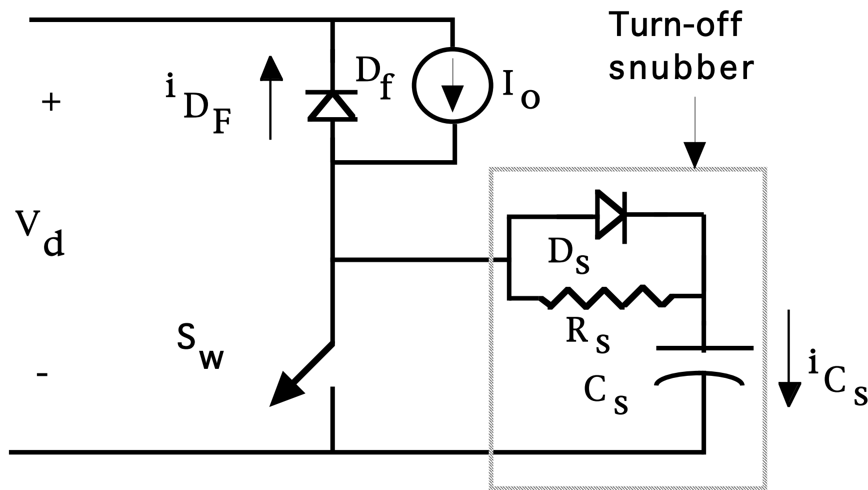
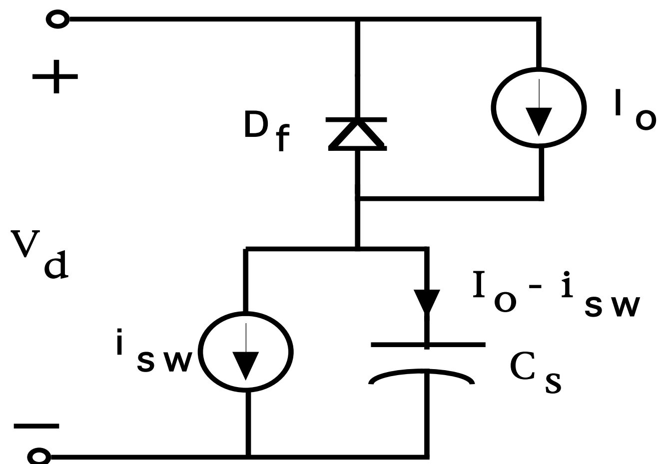
Turn-off Snubber for Controlled Switches



Step-down converter with turn-off snubber



Equivalent circuit during switch turn-off.

- Simplifying assumptions

1. No stray inductance.
2. $i_{sw}(t) = I_o(1 - t/t_{fi})$
3. $i_{sw}(t)$ uneffected by snubber circuit.

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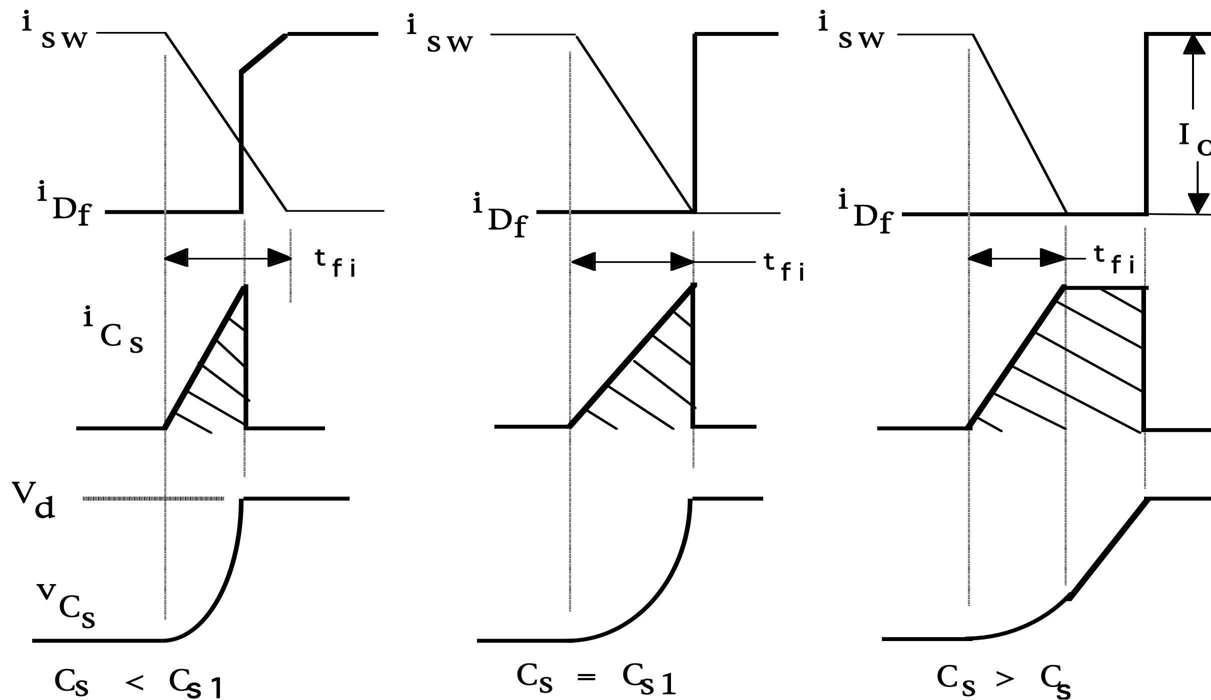
Turn-off Snubber Operation

- Capacitor voltage and current for $0 < t < t_{fi}$ $\quad i_{Cs}(t) = \frac{I_o t}{t_{fi}}$ and $v_{Cs}(t) = \frac{I_o t^2}{2C_s t_{fi}}$

- For $C_s = C_{s1}$, $v_{Cs} = V_d$ at $t = t_{fi}$ yielding $C_{s1} = \frac{I_o t_{fi}}{2V_d}$

Circuit waveforms for varying values of C_s



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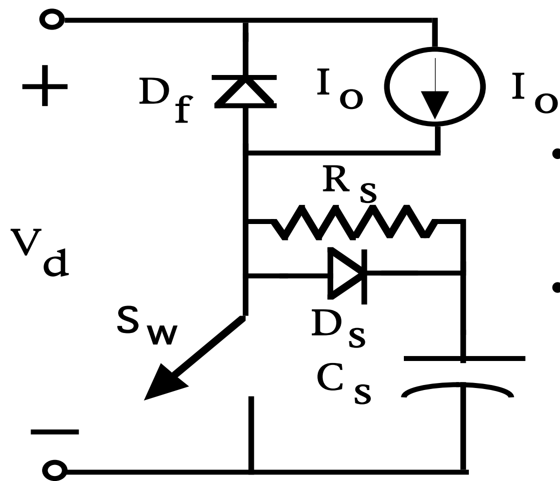
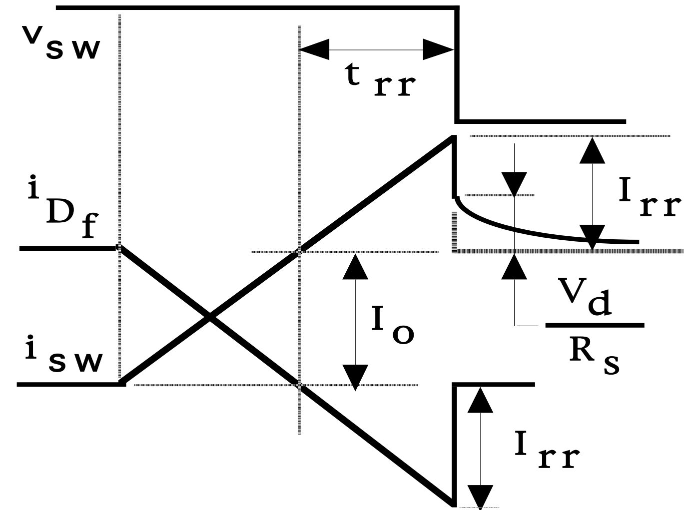
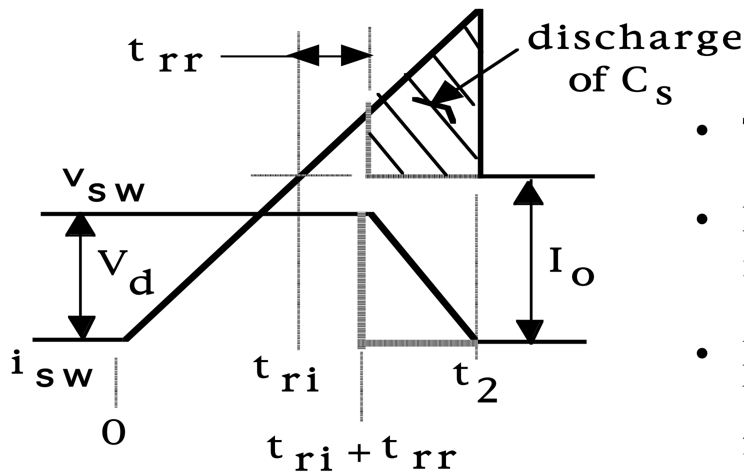
Benefits of Snubber Resistance at Switch Turn-on



- D_s shorts out R_s during S_w turn-off.
- During S_w turn-on, D_s reverse-biased and C_s discharges thru R_s.





- Turn-on with $R_s = 0$
- Energy stored on C_s dissipated in S_w.
- Extra energy dissipation in S_w because of lengthened voltage fall time.

- Turn-on with $R_s > 0$
- Energy stored on C_s dissipated in R_s rather than in S_w.
- Voltage fall time kept quite short.

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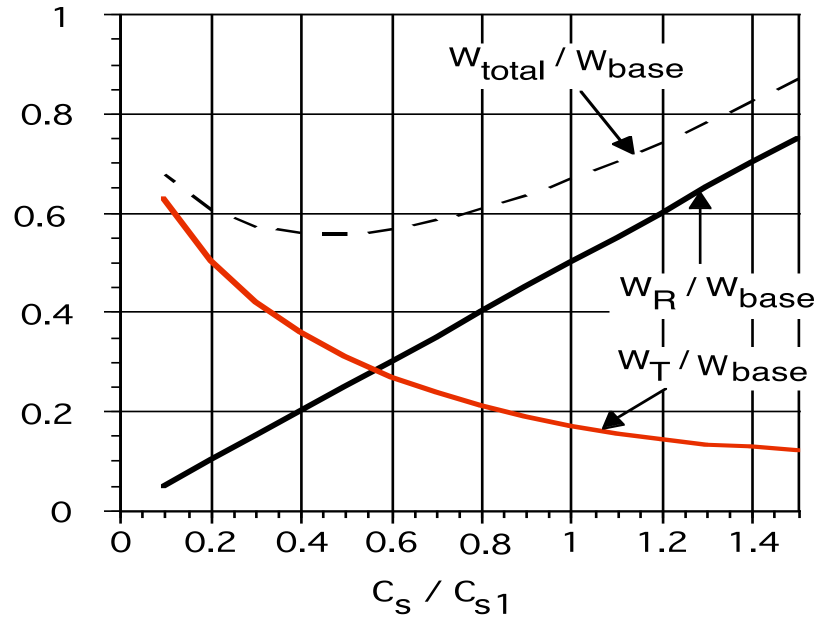
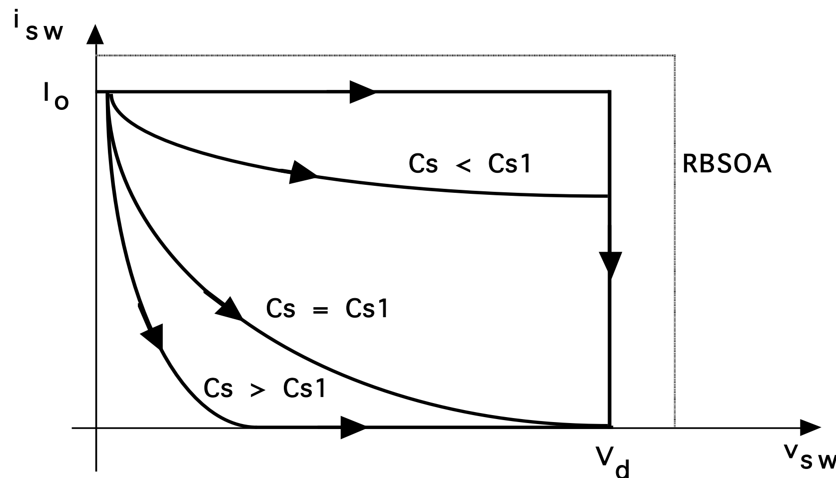
Effect of Turn-off Snubber Capacitance





Energy dissipation

W_R = dissipation in resistor

W_T = dissipation in switch S_w

$$C_{s1} = \frac{I_o t_{fi}}{2V_d}$$

$$W_{total} = W_R + W_T$$

$$W_{base} = 0.5\, V_d I_o t_{fi}$$

Switching trajectory

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Turn-off Snubber Design Procedure

Selection of C_s

- Minimize energy dissipation (W_T) in BJT at turn-on
- Minimize $W_R + W_T$
- Keep switching locus within RBSOA
- Reasonable value is $C_s = C_{s1}$

Selection of R_s

- Limit $i_{cap}(0^+) = \frac{V_d}{R_s} < I_{rr}$
- Usually designer specifies $I_{rr} < 0.2\ I_o$ so $\frac{V_d}{R_s} = 0.2\ I_o$

Snubber recovery time (BJT in on-state)

- Capacitor voltage $= V_d \exp(-t/R_sC_s)$
- Time for v_{Cs} to drop to $0.1V_d$ is $2.3\ R_sC_s$
- BJT must remain on for a time of $2.3\ R_sC_s$

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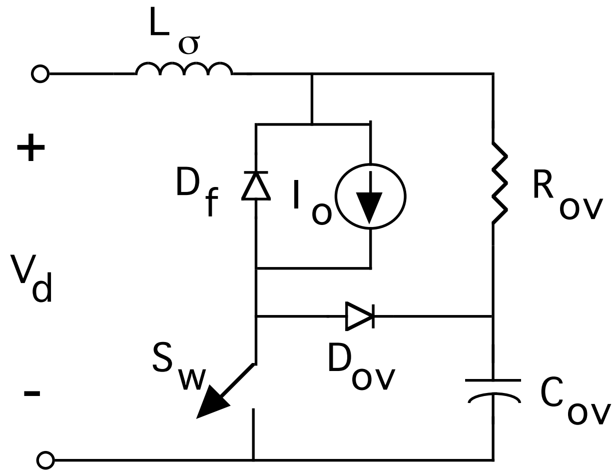
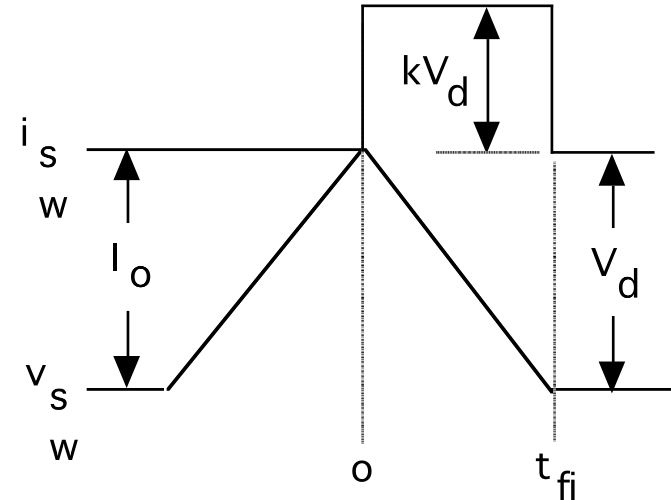
Overvoltage Snubber





- Step-down converter with overvoltage snubber comprised of D_{ov}, C_{ov}, and R_{ov}.

- Overvoltage snubber limits overvoltage (due to stray I nductance) across Sw as it turns off.

- Switch S_w waveforms without overvoltage snubber

- t_{fi} = switch current fall time ; kV_d = overvoltage on S_w

  - $kV_d = L_\sigma \frac{di_{L\sigma}}{dt} = L_\sigma \frac{I_o}{t_{fi}}$

  - $L_\sigma = \frac{kV_d t_{fi}}{I_o}$

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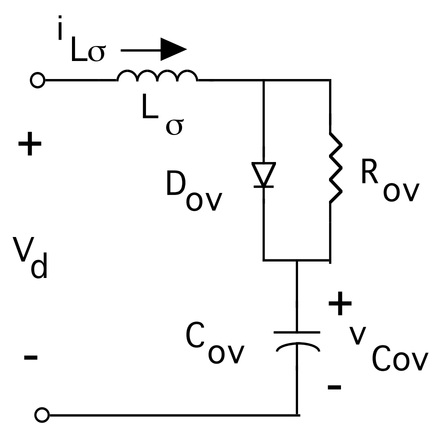
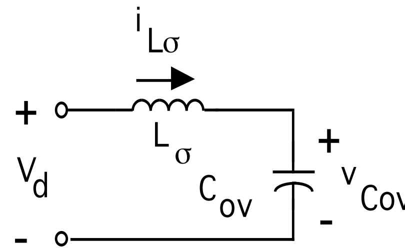
Operation of Overvoltage Snubber



- D_{ov} on for $0 < t < \frac{\pi\sqrt{L_\sigma C_{ov}}}{2}$

- $t_{fi} << \frac{\pi\sqrt{L_\sigma C_{ov}}}{2}$



- Equivalent circuit while inductor current decays to zero

$v_{Cov}(0^+) = V_d \qquad i_{L\sigma}(0^+) = I_o$

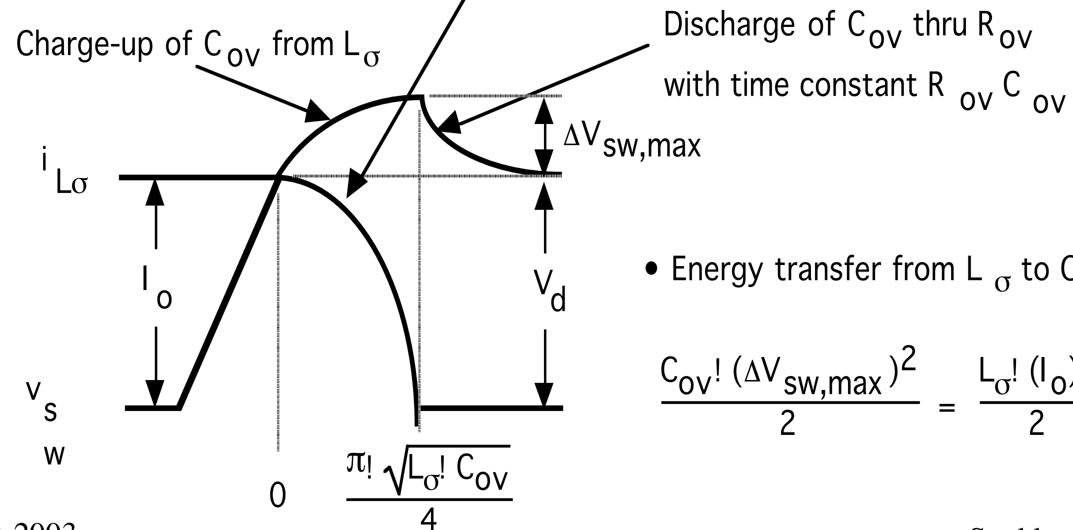
$$i_{L\sigma}(t) = I_o \cos\left[\frac{t}{\sqrt{L_\sigma C_{ov}}}\right]$$

- D_{ov},C_{ov} provide alternate path for inductor current as S_w turns off.

- Switch current can fall to zero much faster than L_s current.

- D_f forced to be on (approximating a short ckt) by I_o after S_w is off.

- Equivalent circuit after turn-off of S_w.



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Overvoltage Snubber Design

- $C_{ov} = \dfrac{L_s!\ I_o^2}{(\Delta v_{sw,max})^2}$

- Limit $\Delta v_{sw,max}$ to $0.1V_d$

- Using $L_s = \dfrac{kV_{d!}\ t_{fi}}{!\ !\ I_o}$ in equation for C_{ov} yields

- $C_{ov} = \dfrac{kV_d t_{fi} I_o^2}{!\ I_o(0.1V_d)^2} = \dfrac{100k!\ t_{fi!}\ I_o}{!\ !\ V_d}$

- $C_{ov} = 200\ k\ C_{s1}$ where $C_{s1} = \dfrac{t_{fi} I_o}{!\ 2V_d}$ which is used in turn-off snubber

- Recovery time of C_{ov} $(2.3R_{ov}C_{ov})$ must be less than off-time duration, t_{off}, of the switch Sw.

- $R_{ov} \approx \dfrac{t_{off}}{2.3!\ C_{ov}}$

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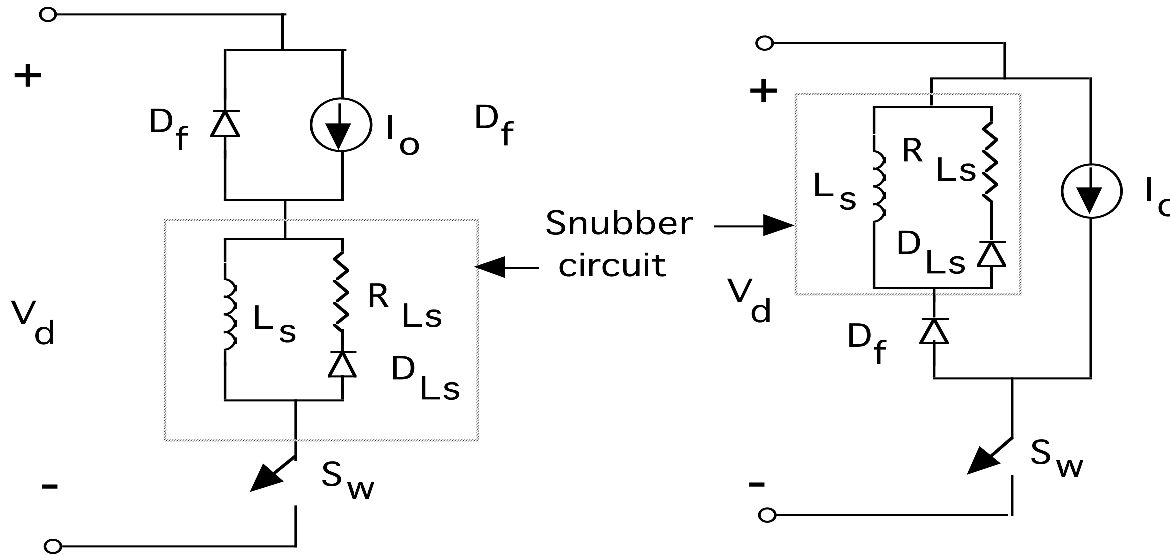
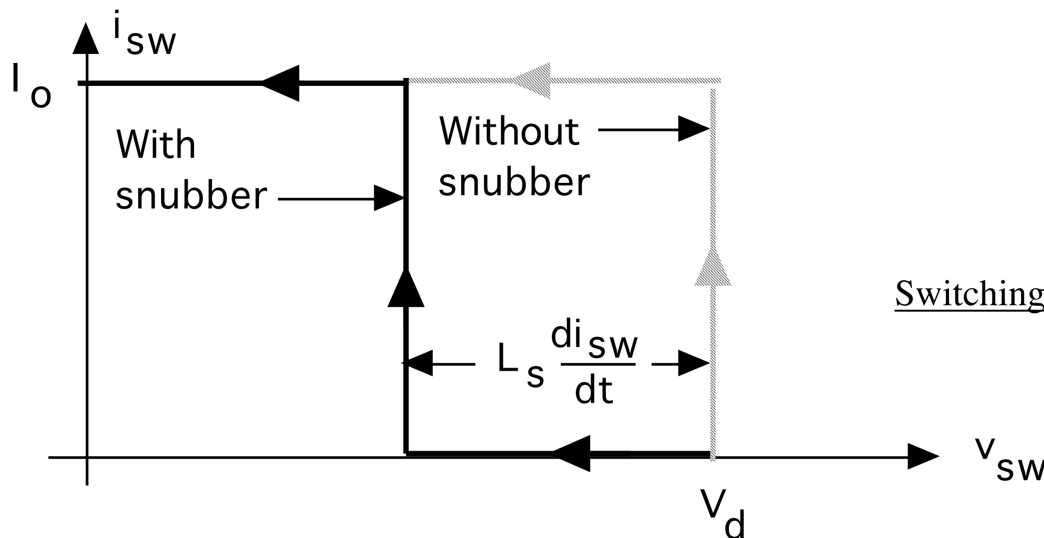
Turn-on Snubber



Step-down converter with turn-on snubber

- Snubber reduces V_{sw} at switch turn-on due drop across inductor L_s.
- Will limit rate-of-rise of switch current if L_s is sufficiently large.



Switching trajectory with and without turn-on snubber.

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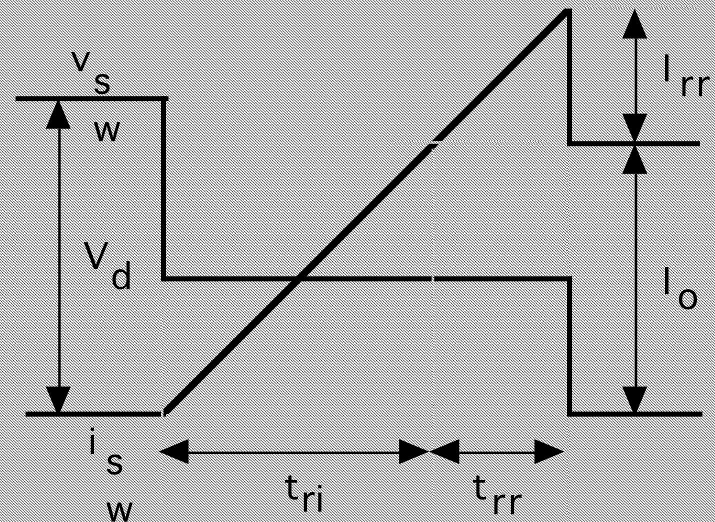
Turn-on Snubber Operating Waveforms

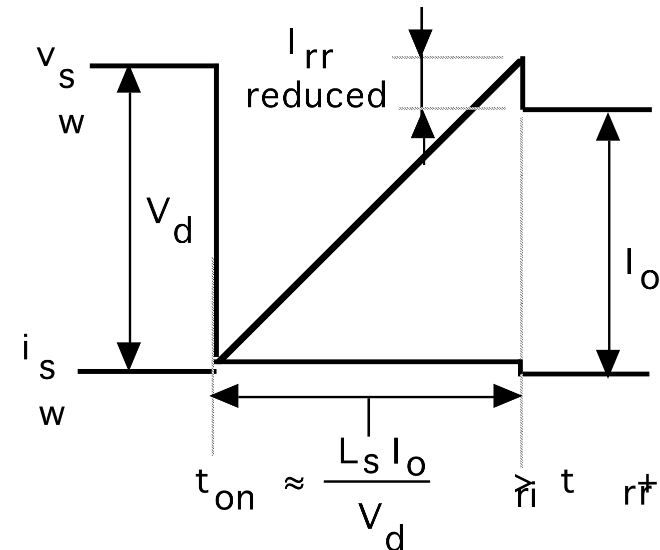
Small values of snubber inductance ($L_s < L_{s1}$)

- $\frac{di_{sw}}{dt}$ controlled by switch S_w and drive circuit.
- $\Delta v_{sw} = \frac{L_s I_o}{t_{ri}}$



Large values of snubber inductance ($L_s > L_{s1}$)

- $\frac{di_{sw}}{dt}$ limited by circuit to $\frac{V_d}{L_s} < \frac{I_o}{t_{ri}}$
- $L_{s1} = \frac{V_d t_{ri}}{I_o}$
- I_{rr} reduced when $L_s > L_{s1}$ because I_{rr} proportional to $\sqrt{\frac{di_{sw}}{dt}}$



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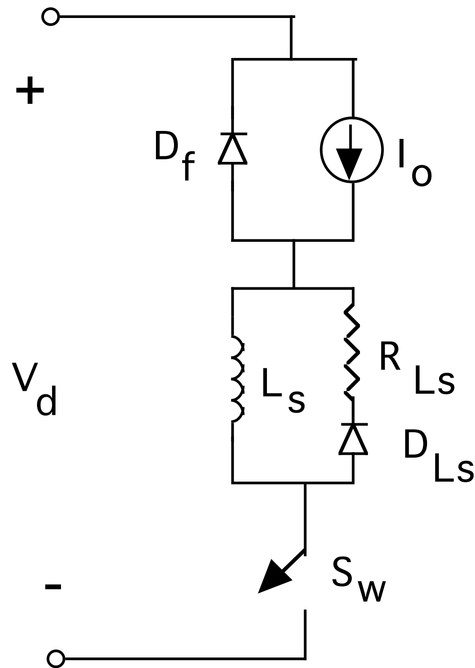
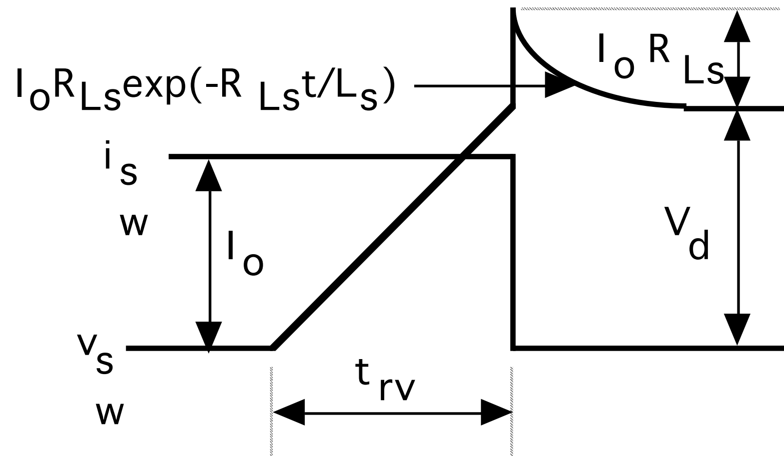
Turn-on Snubber Recovery at Switch Turn-off





- Assume switch current fall time $t_{ri} = 0$.
- Inductor current must discharge thru D_{Ls}- R_{Ls} series segment.

- Switch waveforms at turn-off with turn-on snubber in circuit.
- Overvoltage smaller if t_{fi} smaller.
- Time of 2.3 L_s/R_{Ls} required for inductor current to decay to 0.1 I_o
- Off-time of switch must be > 2.3 L_s/R_{Ls}

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Turn-on Snubber Design Trade-offs

Selection of inductor

- Larger L_s decreases energy dissipation in switch at turn-on
  - $W_{sw} = W_B (1 + I_{rr}/I_o)^2 [1 - L_s/L_{s1}]$
  - $W_B = V_d I_o t_{fi}/2$ and $L_{s1} = V_d t_{fi}/I_o$
  - $L_s > L_{s1}$ $W_{sw} = 0$
- Larger L_s increases energy dissipation in R_{Ls}
  - $W_R = W_B L_s / L_{s1}$
- $L_s > L_{s1}$ reduces magnitude of reverse recovery current I_{rr}
- Inductor must carry current I_o when switch is on - makes inductor expensive and hence turn-on snubber seldom used

Selection of resistor R_{Ls}

- Smaller values of R_{Ls} reduce switch overvoltage $I_o R_{Ls}$ at turn-off
- Limiting overvoltage to $0.1V_d$ yields $R_{Ls} = 0.1 V_d/I_o$
- Larger values of R_{Ls} shortens minimum switch off-time of $2.3 L_s/R_{Ls}$

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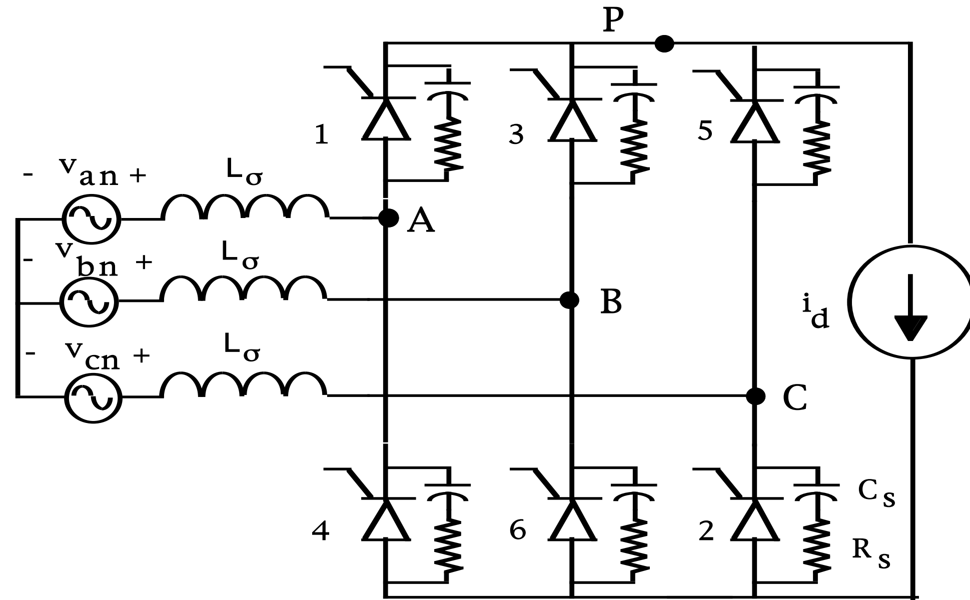
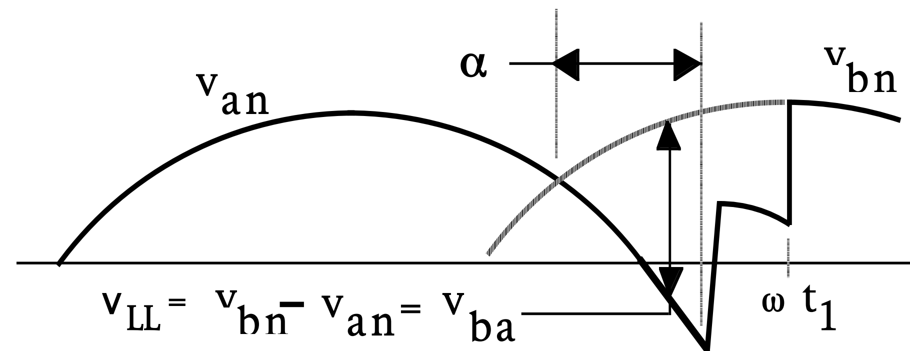
Thyristor Snubber Circuit

3-phase thyristor circuit with snubbers



- $v_{an}(t) = V_s\sin(\omega t)$, $v_{bn}(t) = V_s\sin(\omega t - 120\ )$, $v_{cn}(t) = V_s\sin(\omega t - 240\ )$

Phase-to-neutral waveforms



- $v_{LL}(t) = \sqrt{3}\ V_s\sin(\omega t - 60\ )$
- Maximum rms line-to-line voltage $V_{LL} = \sqrt{\frac{3}{2}}\ V_s$

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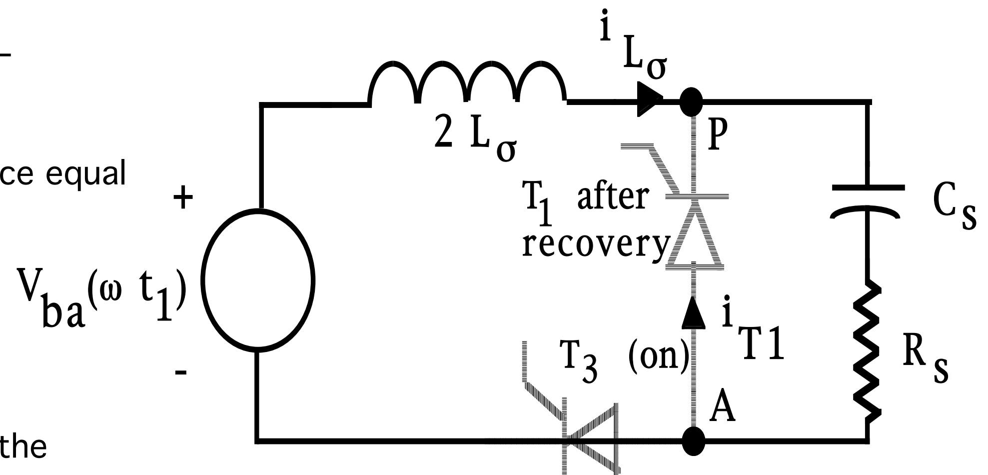
Equivalent Circuit for SCR Snubber Calculations

Assumptions

- Trigger angle $\alpha = 90$ so that $v_{LL}(t)$ = maximum = $\sqrt{2}\,V_{LL}$
- Reverse recovery time t_{rr} << period of ac waveform so that $v_{LL}(t)$ equals a constant value of $v_{ba}(\omega t_1) = \sqrt{2}\,V_{LL}$
- Worst case stray inductance L_σ gives rise to reactance equal to or less than 5% of line impedance.
- Line impedance $= \dfrac{V_s}{\sqrt{2} I_{a1}} = \dfrac{\sqrt{2} V_{LL}}{\sqrt{6} I_{a1}} = \dfrac{V_{LL}}{\sqrt{3} I_{a1}}$

  where I_{a1} = rms value of fundamental component of the line current.
- $\omega L_\sigma = 0.05 \dfrac{V_{LL}}{\sqrt{3} I_{a1}}$

Equivalent circuit after T1 reverse recovery



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Component Values for Thyristor Snubber

- Use same design as for diode snubber but adapt the formulas to the thyristor circuit notation
- Snubber capacitor $C_s = C_{base} = L_\sigma \left[\frac{I_{rr}}{V_d}\right]^2$
- From snubber equivalent circuit $2\, L_\sigma \frac{di_{L\sigma}}{dt} = \sqrt{2}\, V_{LL}$
- $I_{rr} = \frac{di_{L\sigma}}{dt} t_{rr} = \frac{\sqrt{2} V_{LL}}{2 L_\sigma} t_{rr} = \frac{\sqrt{2} V_{LL}}{2! \frac{0.05!\ V_{LL}}{\sqrt{3}!\ I_{a1}\omega}} t_{rr} = 25\ \omega I_{a1} t_{rr}$
- $V_d = \sqrt{2}\ V_{LL}$
- $C_s = C_{base} = \frac{0.05!\ V_{LL}}{\sqrt{3}!\ I_{a1}\omega} \left[\frac{25!\ \omega I_{a1} t_{rr}}{!\ \sqrt{2} V_{LL}}\right]^2 = \frac{8.7!\ \omega I_{a1} t_{rr}}{V_{LL}}$
- Snubber resistance $R_s = 1.3\ R_{base} = 1.3 \frac{V_d}{I_{rr}}$
- $R_s = 1.3 \frac{\sqrt{2} V_{LL}}{25 \omega I_{a1} t_{rr}} = \frac{0.07!\ V_{LL}}{!\ \omega I_{a1} t_{rr}}$
- Energy dissipated per cycle in snubber resistance = W_R
- $W_R = \frac{L_\sigma I_{rr}^2}{2} + \frac{C_s V_d^2}{2} = 18\ \omega\ I_{a1}\ V_{LL} (t_{rr})^2$

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Drive Circuits

Outline

- Drive circuit design considerations
- DC-coupled drive circuits
- Isolated drive circuits
- Protection measures in drive circuits
- Component/circuit layout considerations

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Functionality of Gate/Base Drive Circuits

- Turn power switch from off-state to on-state
  - Minimize turn-on time through active region where power dissipation is large
  - Provide adequate drive power to keep power switch in on-state
- Turn power switch from on-state to off-state
  - Minimize turn-off time through active region wherepower dissipation is large
  - Provide bias to insure that power switch remains off
- Control power switch to protect it when overvoltages or overcurrents are sensed
- Signal processing circuits which generate the logic control signals not considered part of the drive circuit
  - Drive circuit amplifies control signals to levels required to drive power switch
  - Drive circuit has significant power capabilities compared to logic level signal processing circuits
- Provide electrical isolation when needed between power switch and logic level signal processing/control circuits

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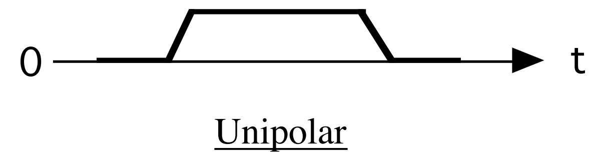
Drive Circuit Design Considerations

- Drive circuit topologies

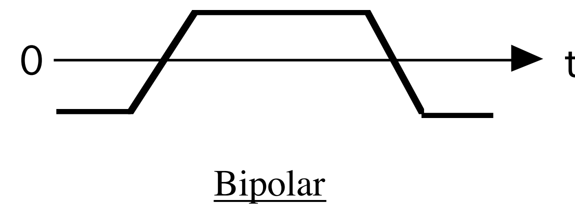
  - Output signal polarity - unipolar or bipolar
  - AC or DC coupled
  - Connected in shunt or series with power switch

- Output current magnitude
  - Large I_{on} shortens turn-on time but lengthens turn-off delay time
  - Large I_{off} shortens turn-off time but lengthens turn-on delay time



Unipolar

- Provisions for power switch protection
  - Overcurrents
  - Blanking times for bridge circuit drives



Bipolar

- Waveshaping to improve switch performance
  - Controlled di_B/dt for BJT turn-off
  - Anti-saturation diodes for BJT drives
  - Speedup capacitors
  - Front-porch/backporch currents

- Component layout to minimize stray inductance and shielding from switching noise

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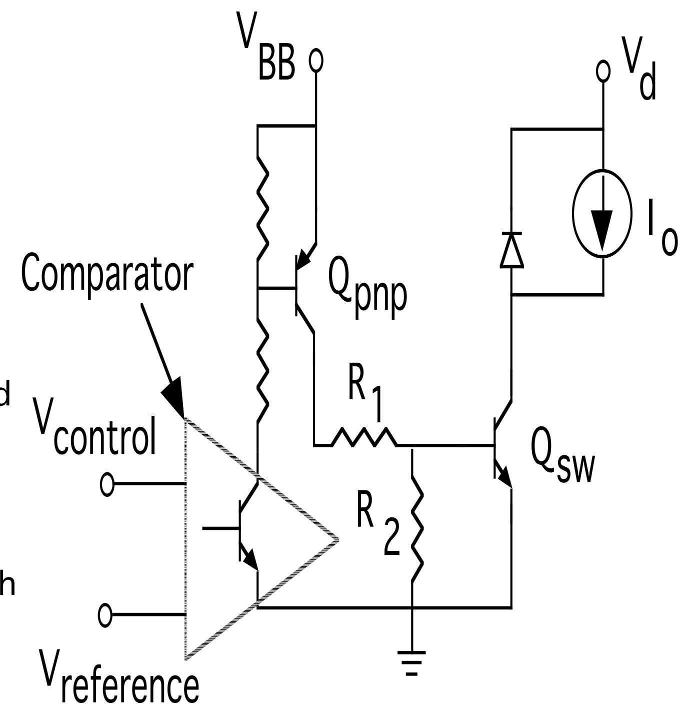
Unipolar DC-coupled Drive Circuit - BJT Example

- Circuit operation
  - $V_{control} > V_{reference}$ - BJT at comparator output on which puts Q_{pnp} and Q_{sw} on
  - $V_{control} < V_{reference}$ - BJT at comparator output off which turns Q_{pnp} off and thus Q_{sw} off

- Design procedure
  - $R_2 = \frac{V_{BE,off}}{I_{B,off}}$; $I_{B,off}$ based on desired turn-off time.
  - $I_{pnp} = I_{B,on} + \frac{V_{BE,on}}{R_2}$; $I_{B,on}$ value based on BJT beta and value of I_o.
  - $V_{BB} = V_{CE,on}(Q_{pnp}) + R_1 I_{C,pnp} + V_{BE,on}(Q_{sw})$
  - V_{BB} = 8 to 10 V ; compromise between larger values which minimize effects of V_{BE} variations and smaller values which minimize power dissipation in drive circuit



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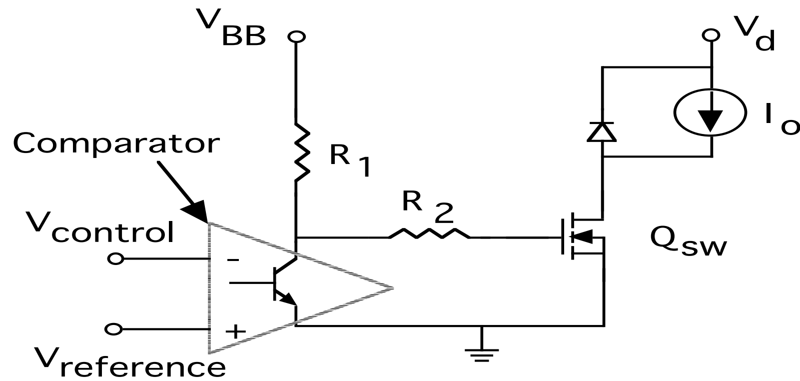
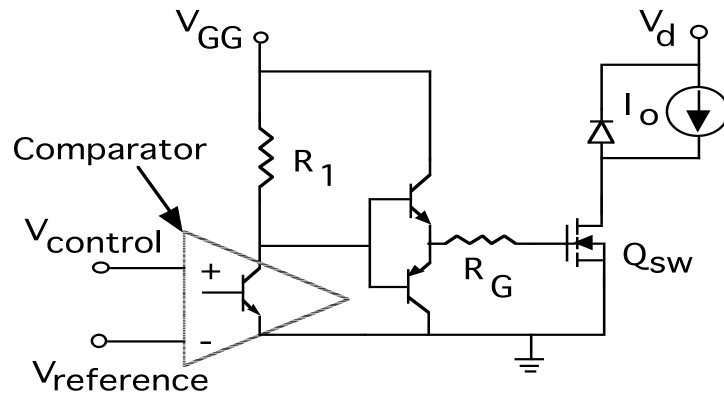
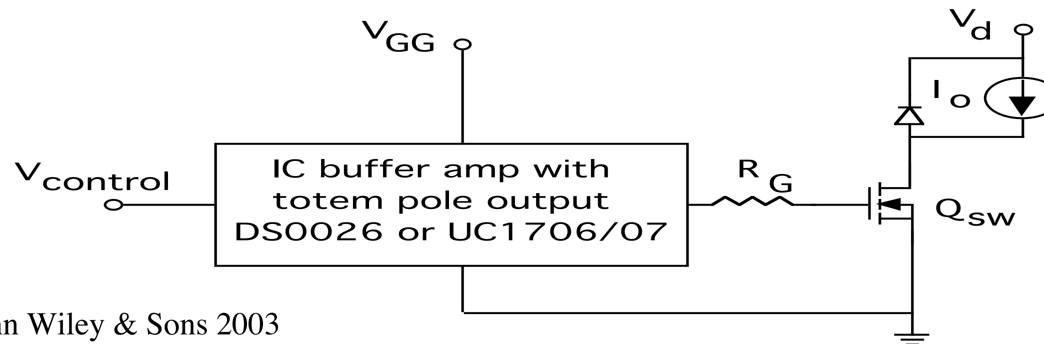
Unipolar DC-coupled Drive Circuits- MOSFET examples



- $V_{control} > V_{reference}$ comparator output high and Q_{sw} on
- $V_{control} < V_{reference}$ comparator output low and Q_{sw} off



- $V_{control} > V_{reference}$ comparator output high putting Q_{npn} on and thus Q_{sw} on
- $V_{control} < V_{reference}$ comparator output low putting Q_{pnp} on and thus Q_{sw} off



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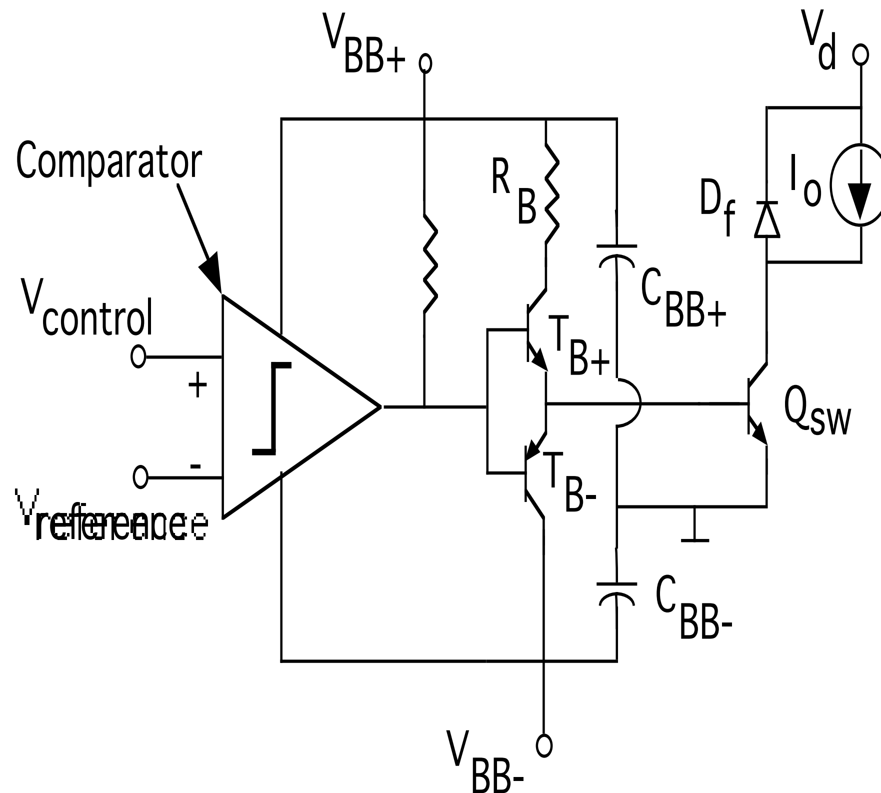
Bipolar DC-coupled Drive Circuit- BJT Example



- $V_{control} < V_{reference}$ - comparator output low, T_{B-} on and Q_{sw} off.
- Large reverse base current flows to minimize turn-off time and base-emitter of Q_{sw} reversed biased to insure off-state.
- $V_{control} > V_{reference}$ - comparator output high, T_{B+} on and Q_{sw} on.
- Large forward base current to minimize turn-on time and to insure saturation of Q_{sw} for low on-state losses

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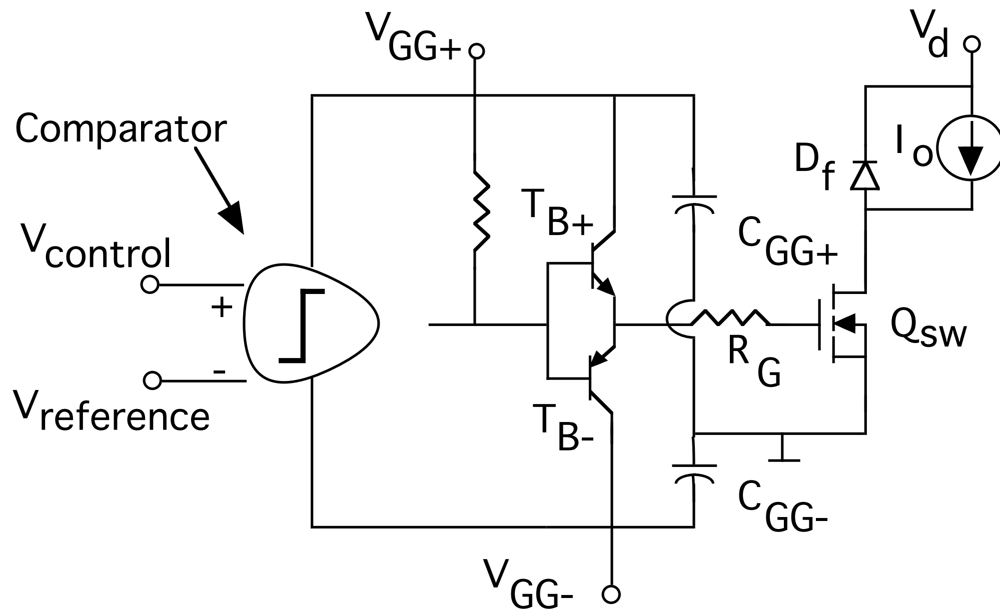
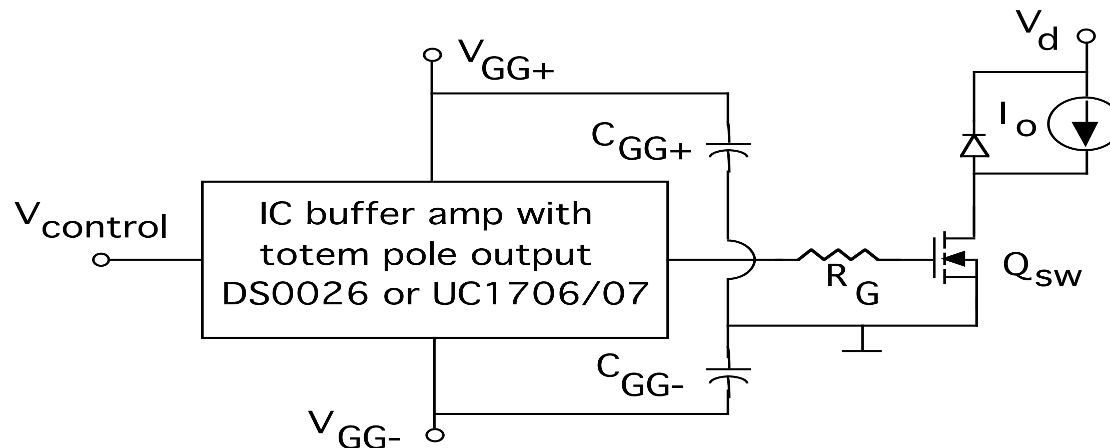
Bipolar DC-coupled Drive Circuit- MOSFET Example



- Bipolar drive with substantial output current capability



- Simple bipolar drive circuit with moderate (1 amp)output current capability

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Need for Electrical Isolation of Drive Circuits

- Negative half cycle of $v_s(t)$ - positive dc rail near safety ground potential. T_- emitter potential large and negative with respect to safety and logic ground

- Postive half cycle of $v_s(t)$ - negative dc rail near safety ground potential. T_+ emitter substantially positive with espect to safety ground if T_- is off

- Variation in emitter potentials with respect to safety and logic ground means that electrical isolation of emitters from logic ground is needed.

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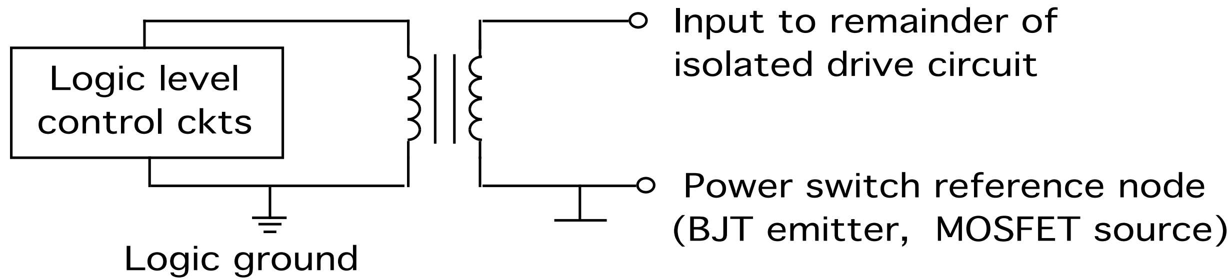
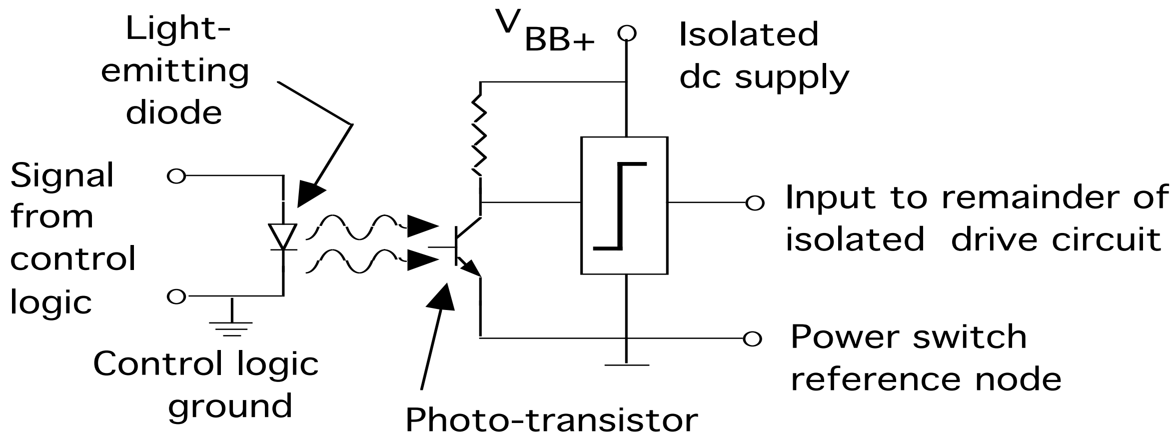
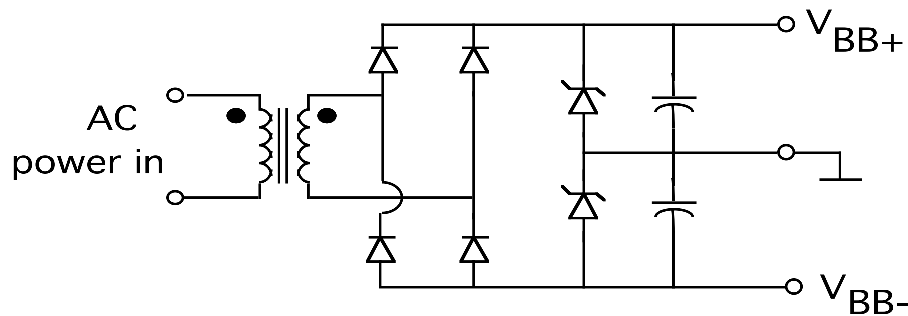
Methods of Control Signal Isolation



- Transformer isolation



- Opto-coupler isolation



- Isolated dc power supplies for drive circuits

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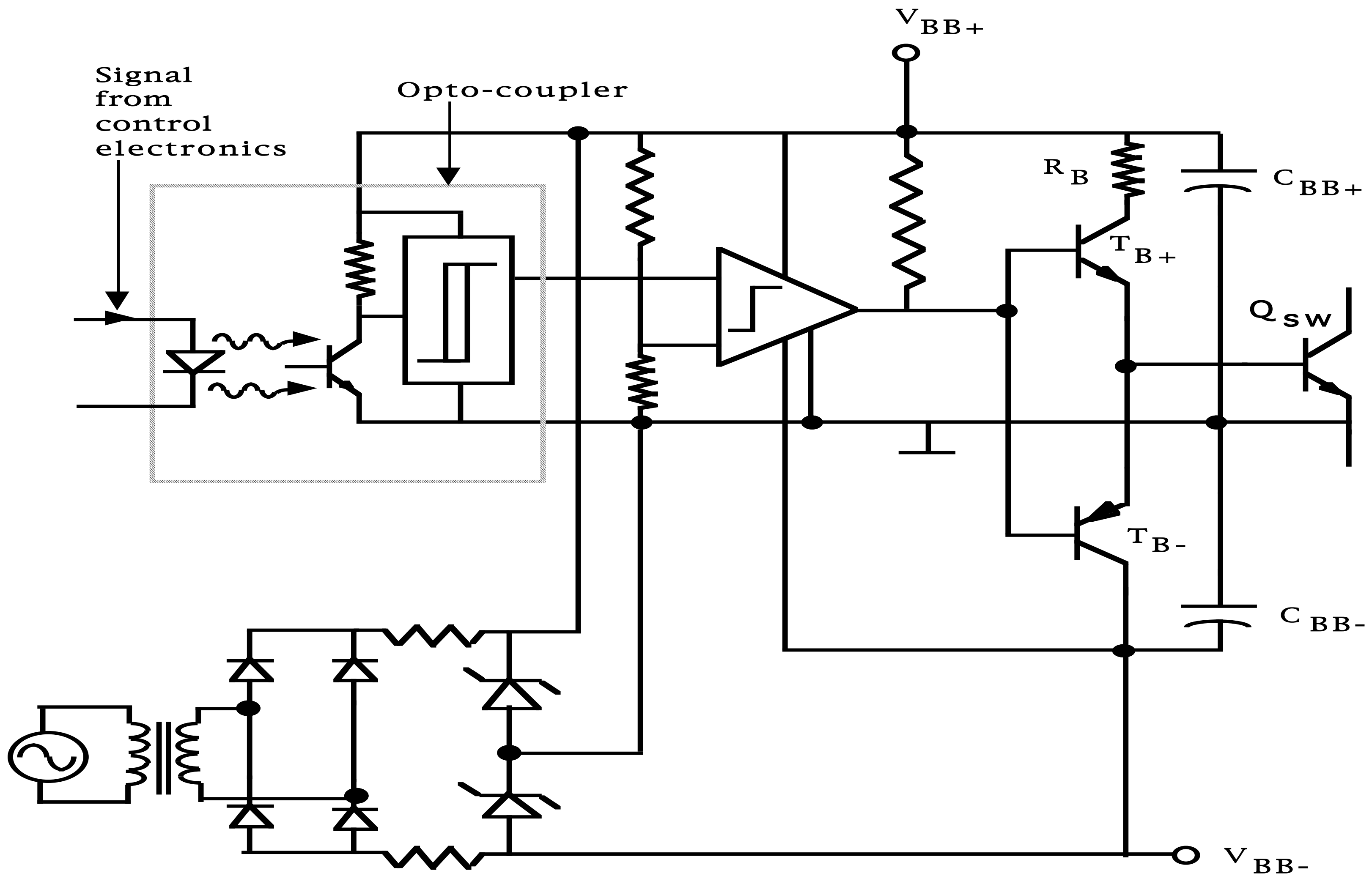
Opto-Coupler Isolated BJT Drive



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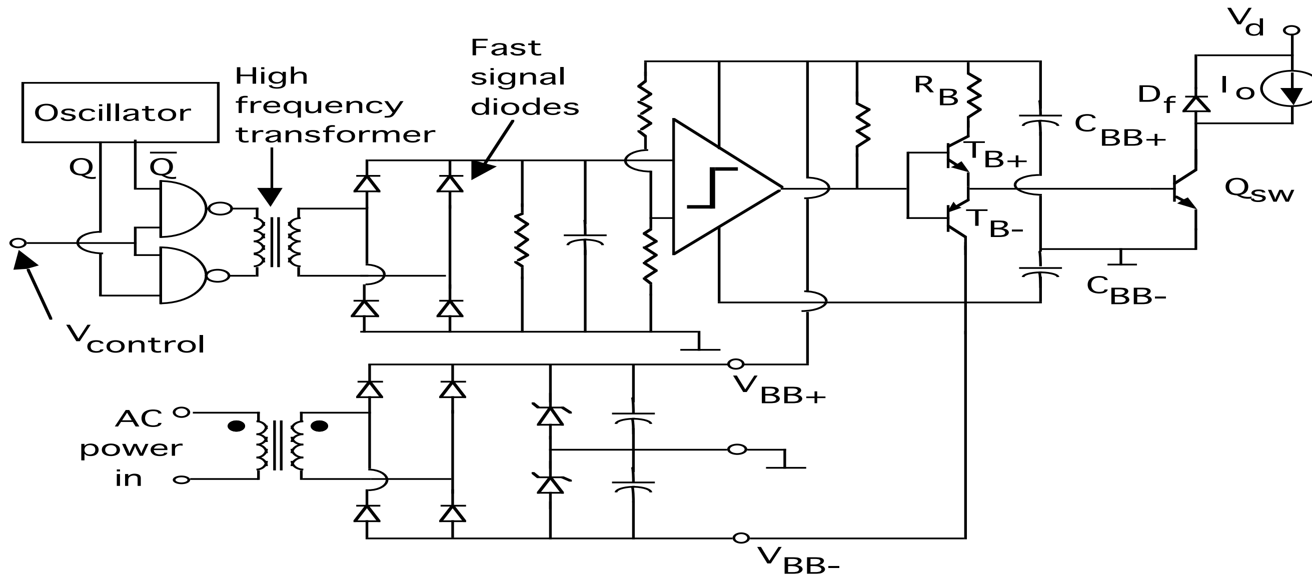
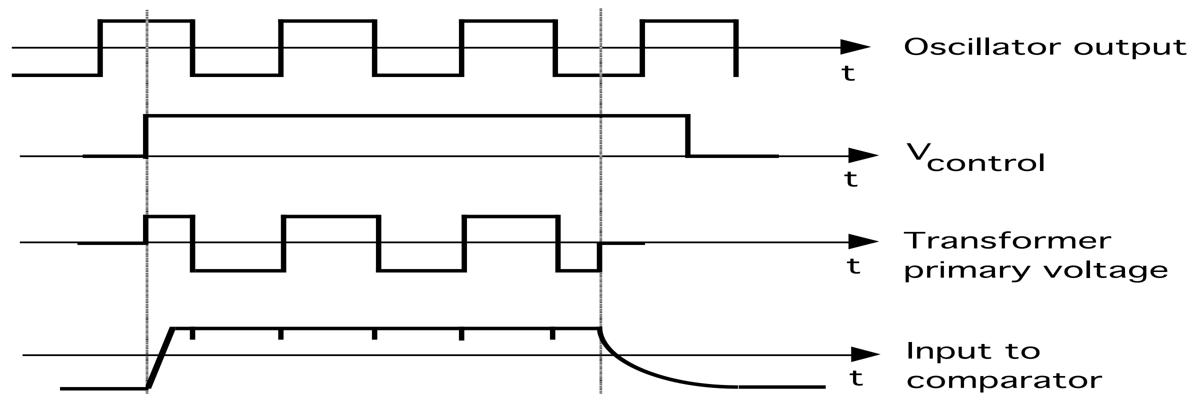
Transformer-coupled BJT Drive





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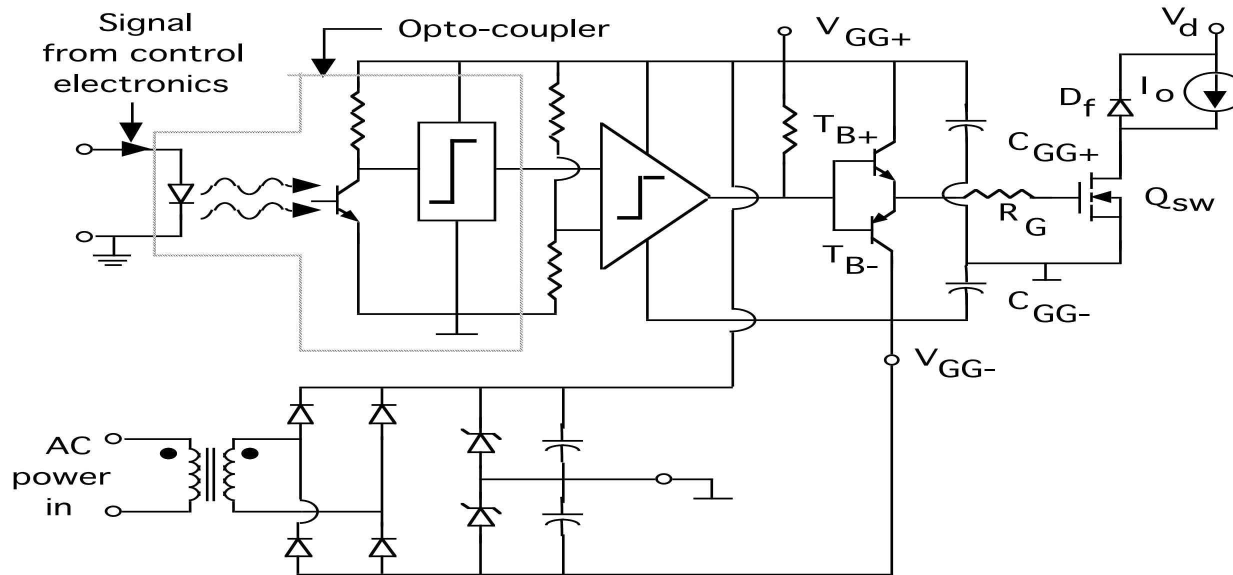
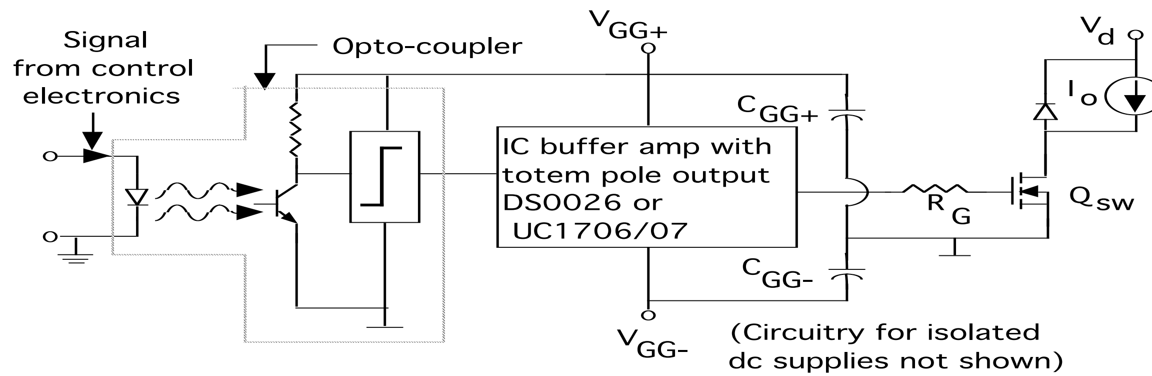
Opto-Coupler Isolated MOSFET Drives





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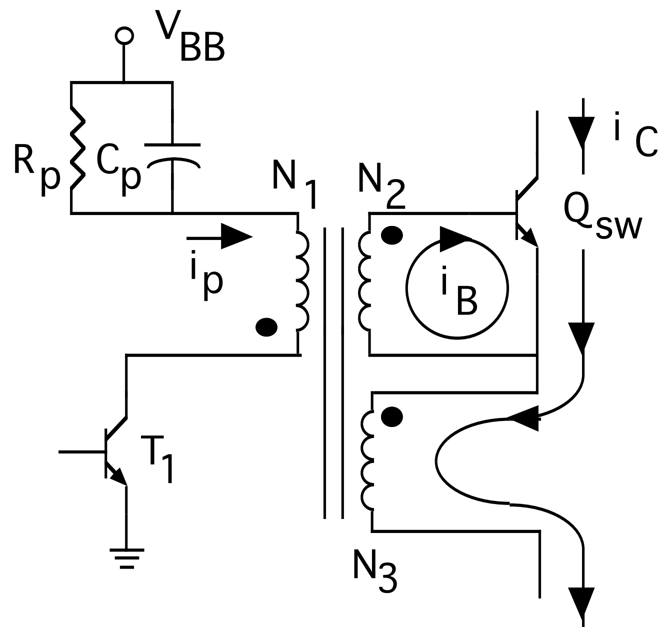
Isolated Drives Without Auxiliary DC Supplies - Proportional Flyback BJT Example



- Regenerative circuit operation
  - T_1 on - current $i_p = V_{BB}/R_p$ and Q_{sw} off
  - T_1 turned off - stored energy in gapped transformer core induces positive base current i_B in Q_{sw} causing it to go active and collector current i_C begins to flow
  - Regenerative action of transformer connections supplies a base current $i_B = N_3 i_C/N_2$ which keeps Q_{sw} on even with $i_p = 0$
  - T_1 turned on - positive current i_p causes a base current $i_B = N_3 i_C/N_2 - N_1 i_p/N_2$ in Q_{sw}
    - Initially i_p quite large ($i_p(0^+) = \beta i_{B1}(0^+)$) so Q_{sw} turned off
- Circuit design must insure turn-off i_B has adequate negative magnitude and duration
  - Best suited for high frequency operation - lower volt-second requirements on transformer.
  - Also best suited for limited variations in duty cycle

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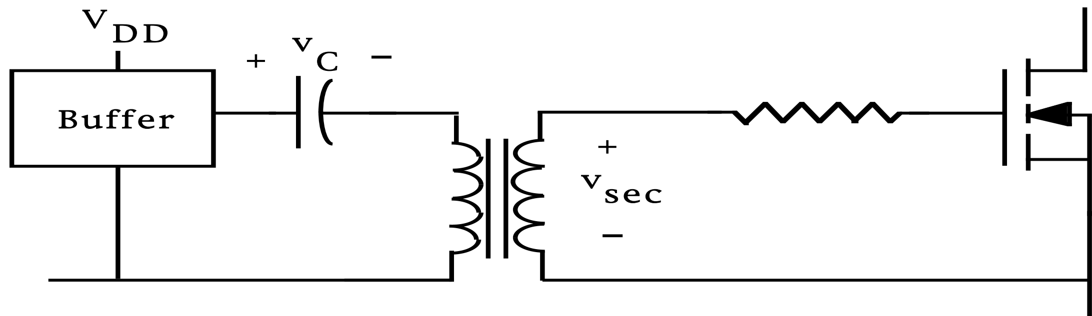
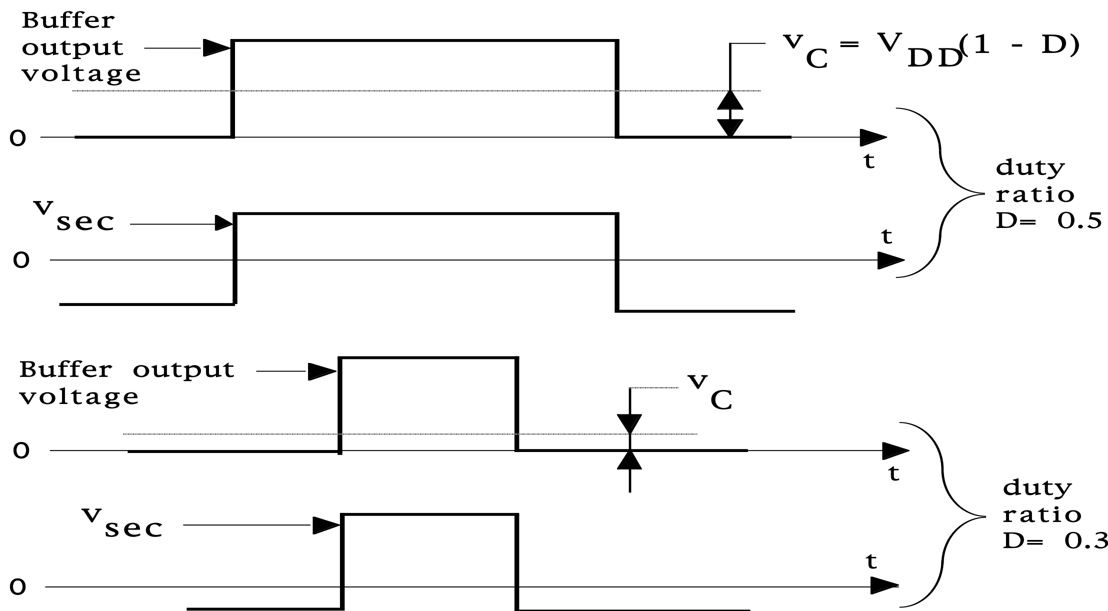
Isolated Drives Without Auxiliary DC Supplies - MOSFET Example





Most suitable for applications where duty cycle D is 50% or less. Positive-going secondary voltage decreases as D increases.

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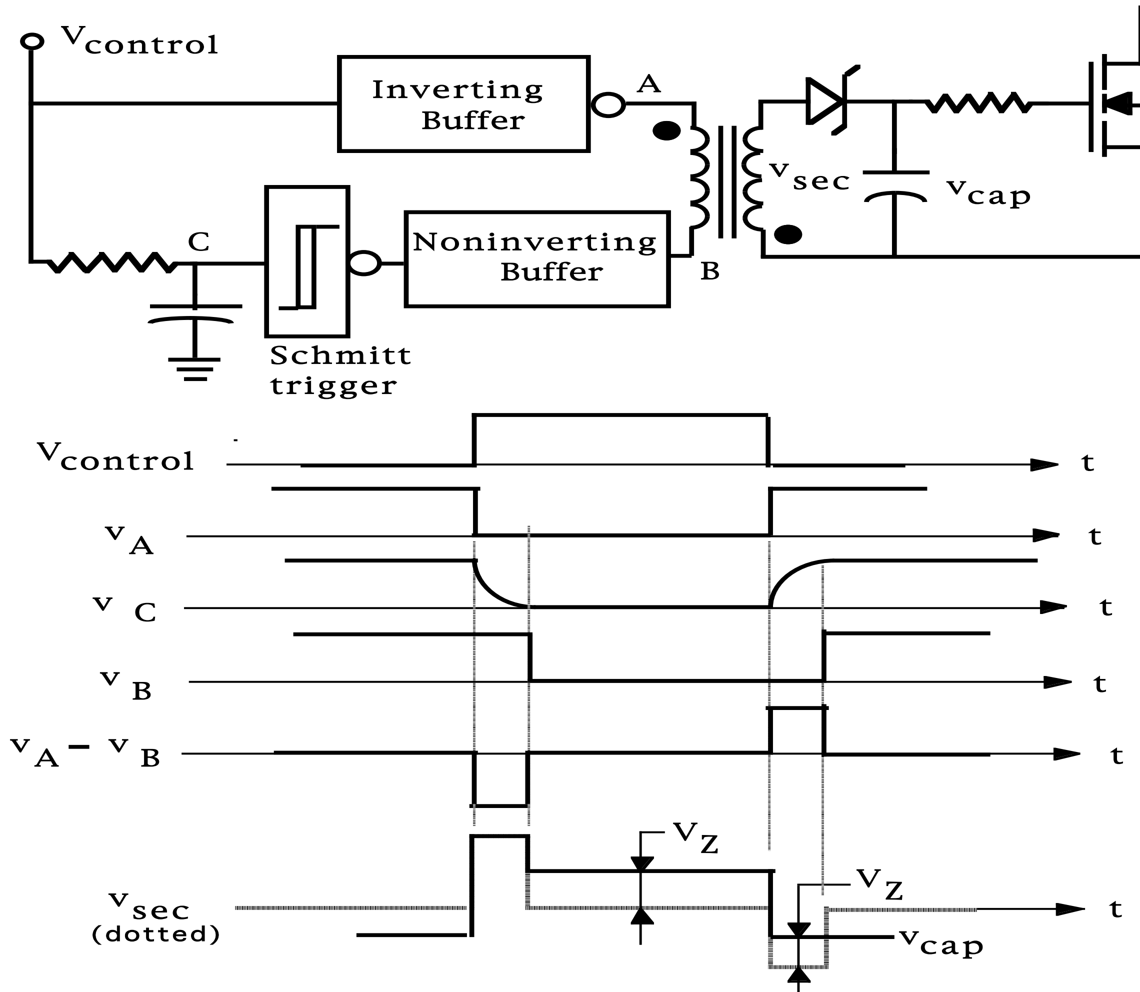
Isolated Drive Without Auxiliary DC Supplies - MOSFET Example



Zener diode voltage V_Z must be less than negative pulse out of transformer secondary or pulse will not reach MOSFET gate to turn it off.

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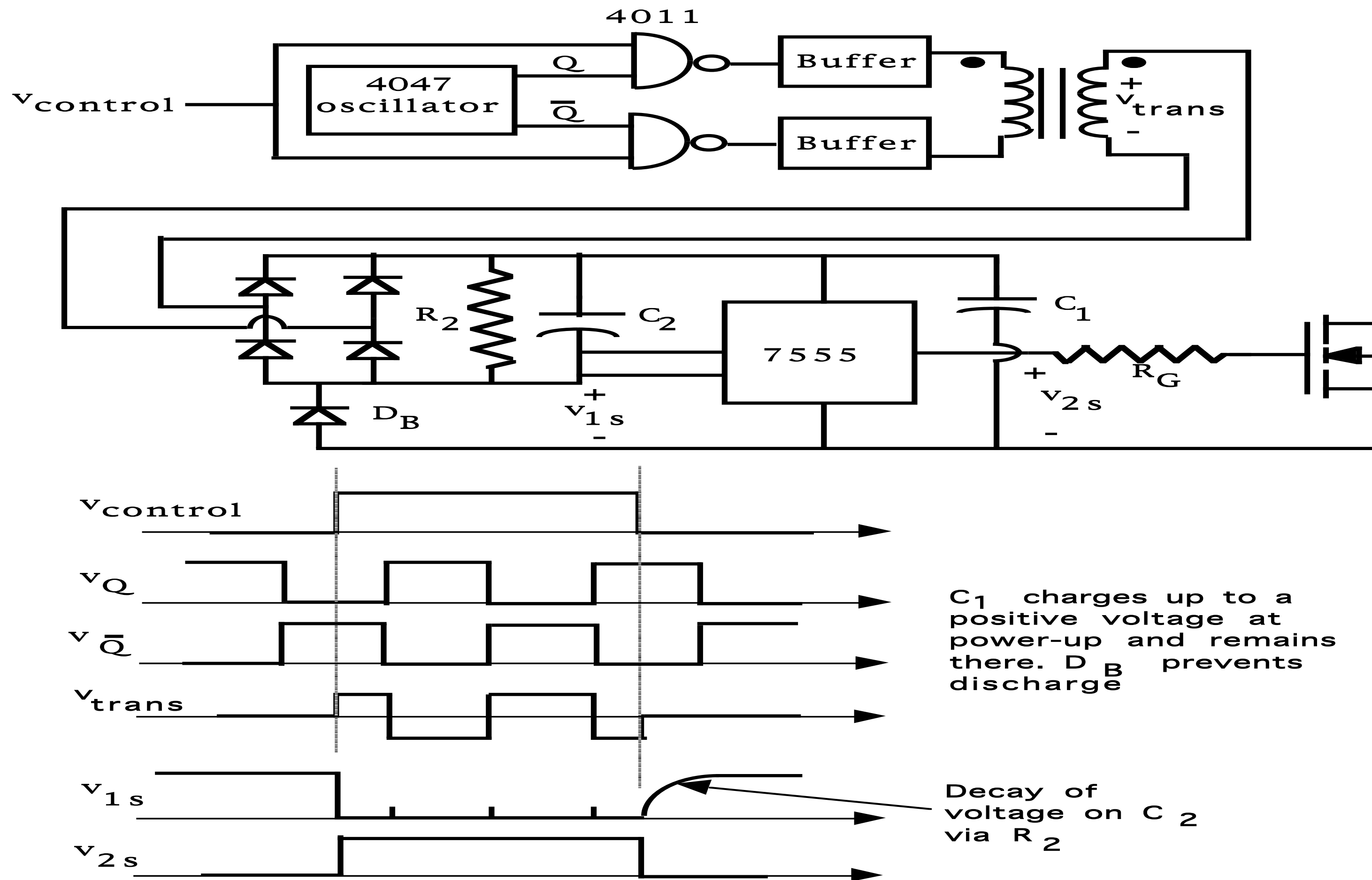
Isolated Drive Without Auxiliary DC Supplies - MOSFET Example



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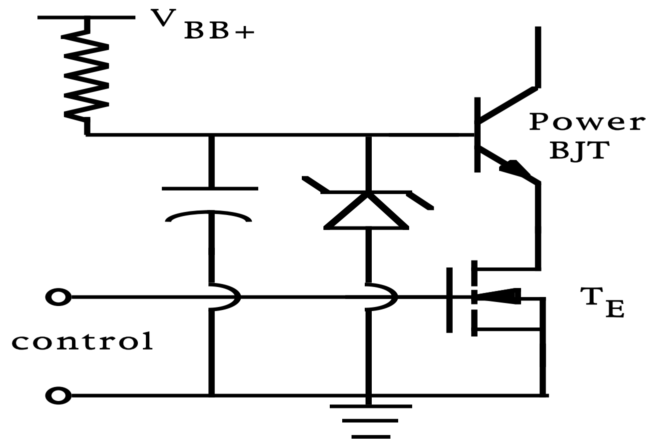
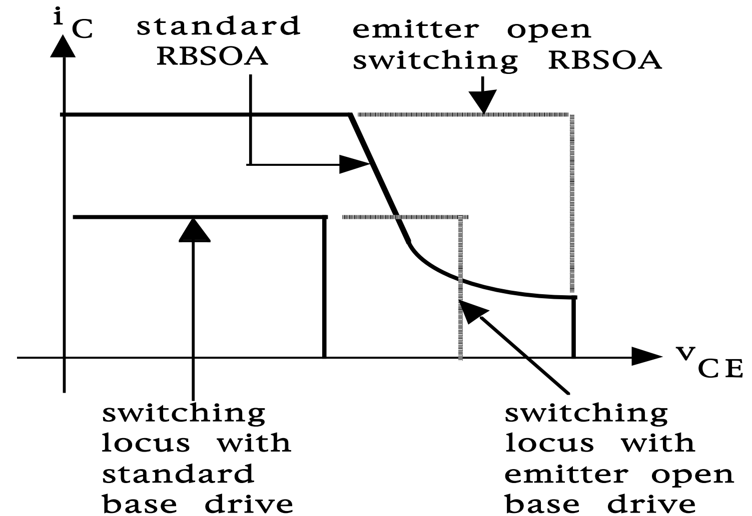
Emitter-Open Switching of BJTs





- Circuit operation
  - Turn on power BJT by turning on MOSFET T_E.
  - Turn off power BJT by turning off MOSFET T_E.
    - Collector current flows out base as negative base current.
  - Greater i_B(off) compared to standard drive circuits i_C = b i_B(off) removes stored charge much faster
    - Turn off times reduced (up to ten times).

- On-state losses of series combination of MOSFET and BJT minimized.
  - Low voltage MOSFET which has low losses can be used. Maximum off-state MOSFET voltage limited by Zener diode.
  - BJT base emitter junction reverse biased when T_E off so breakdown rating of BJT given by BV_{CBO} instead o of BV_{CEO}. With lower BV_{CEO} rating, BJT losses in on-state reduced.

- Circuit also useful for GTOs and FCTs.

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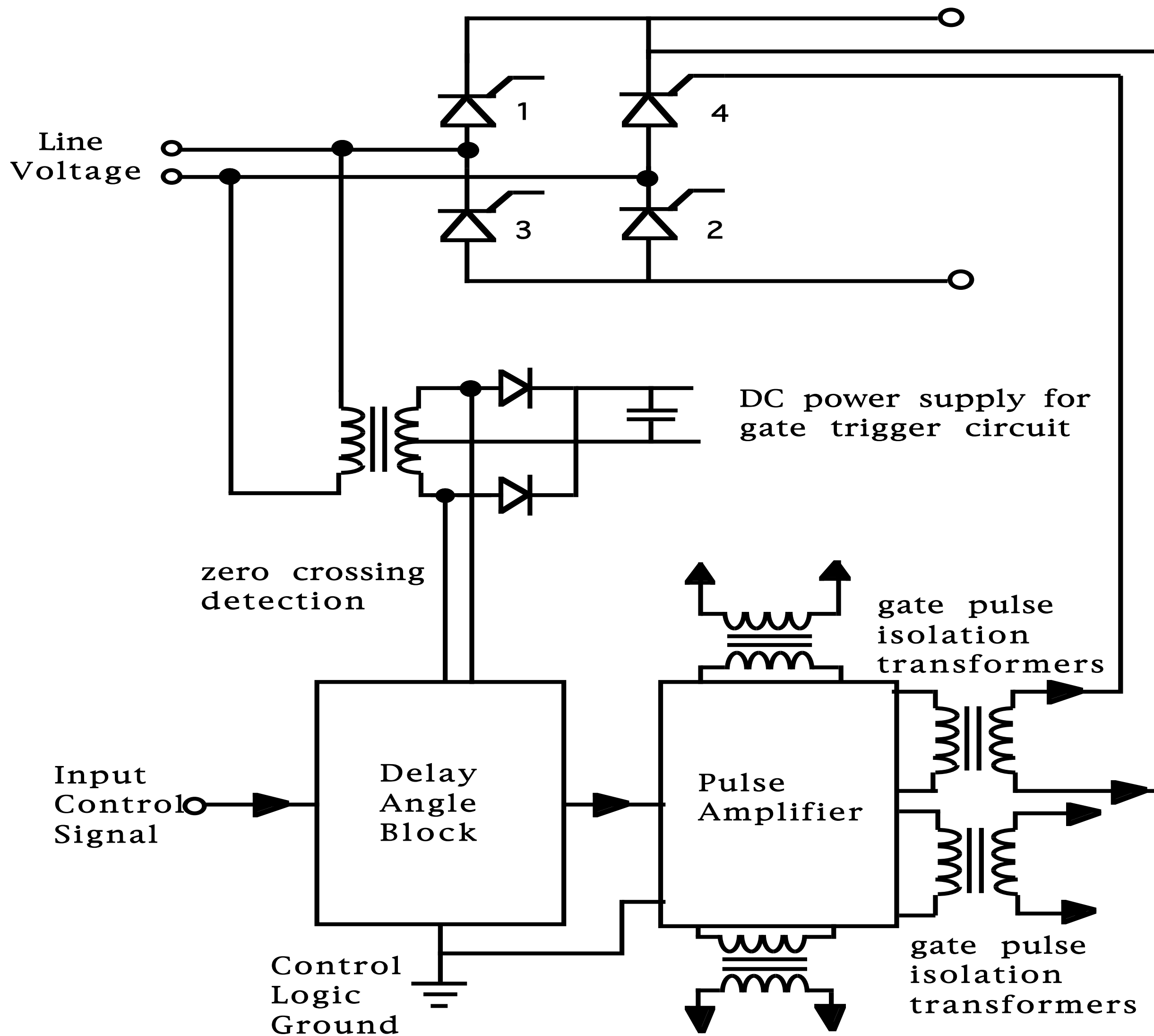
Thyristor Gate Drive Circuit



Delay angle block is commercially available integrated circuit - TCA780 circuit family

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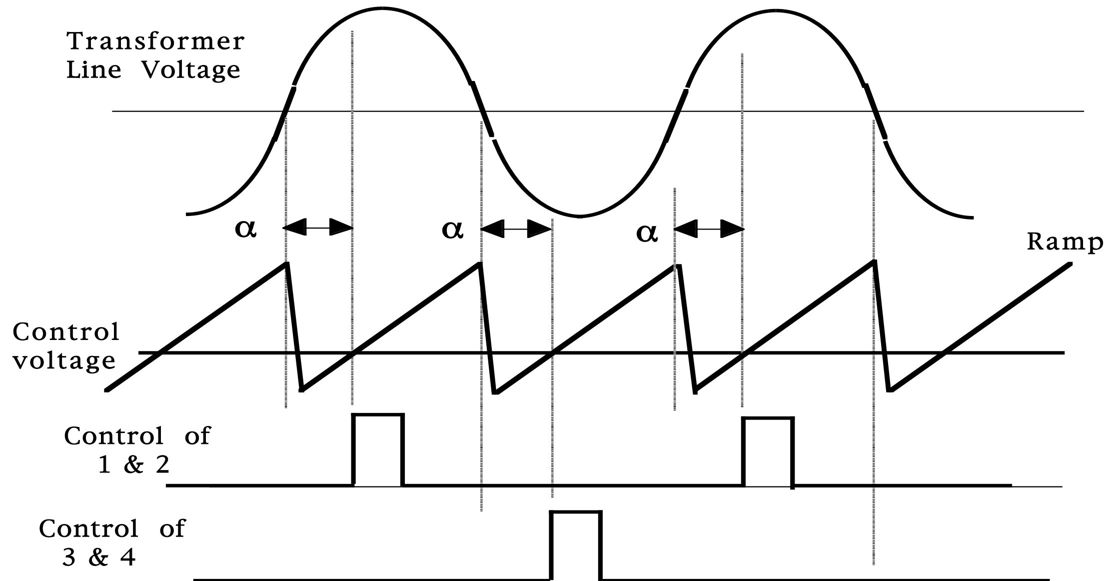
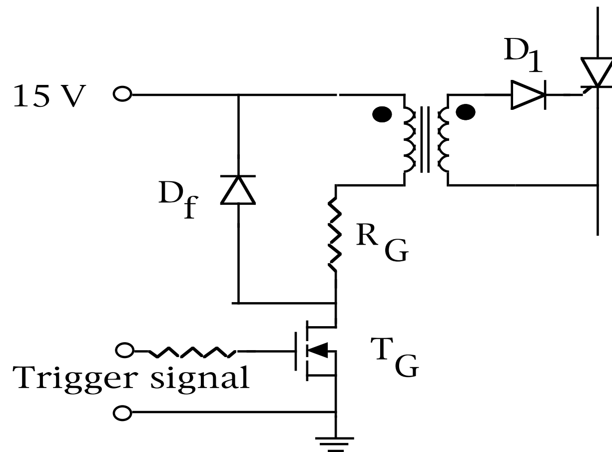
Thyristor Gate Drive Circuit (cont.)



Thyristor gate drive waveforms



Gate pulse amplifier

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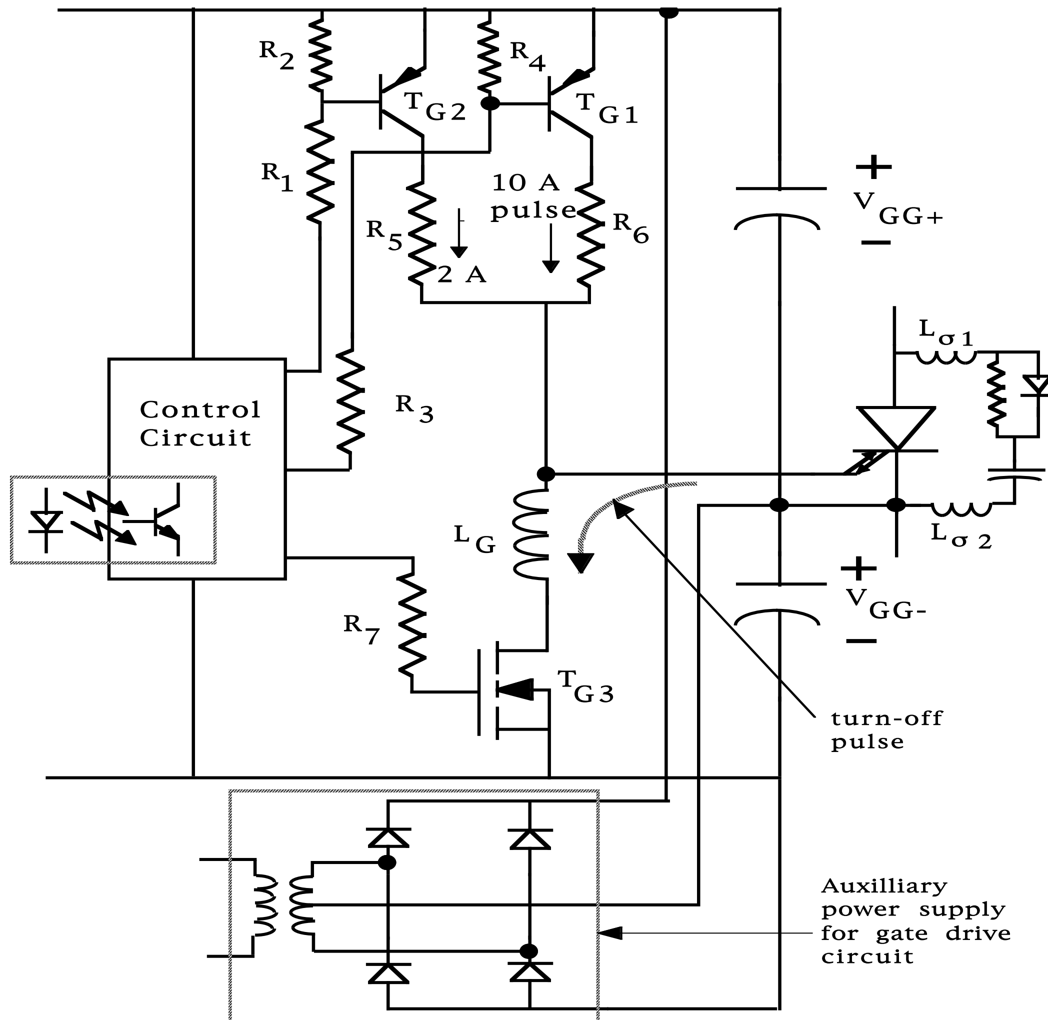
GTO Gate Drive Circuit



- **Turn on T_{G1} and T_{G2} to get large front-porch current**
- **Turn off T_{G1} after some specified time to reduce total gate current to back-porch value.**

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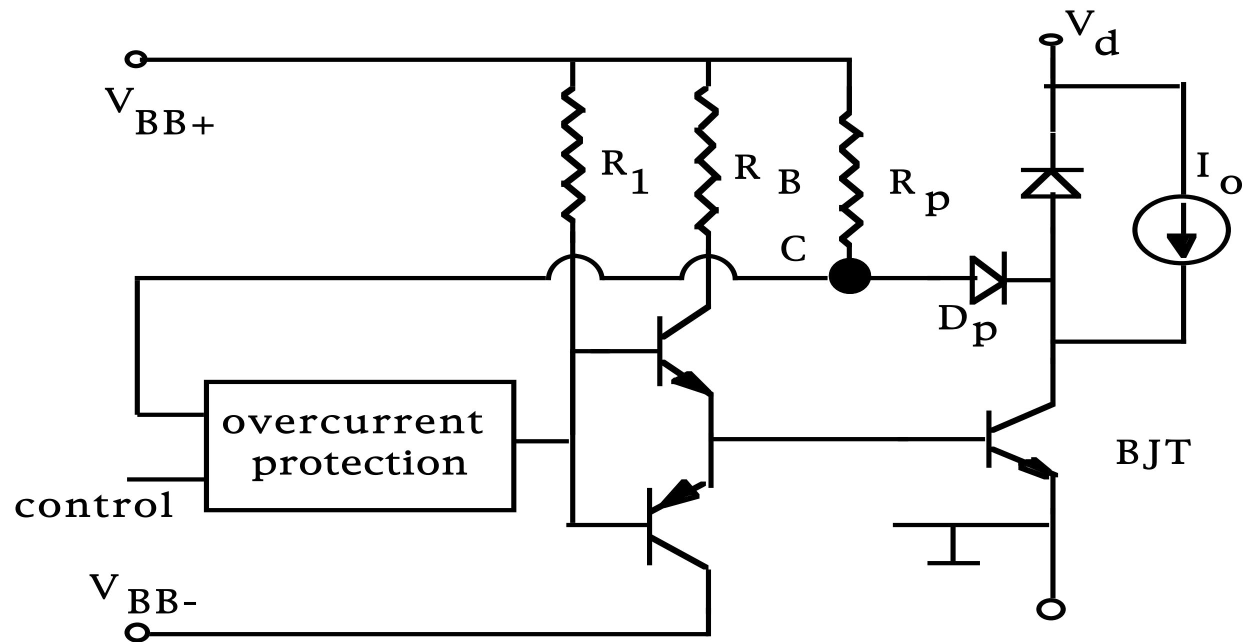
Overcurrent Protection With Drive Circuits



- Point C one diode drop above $V_{CE(sat)}$ when BJT is on. Overcurrent will increase V_{CE} and thus potential at C.

- If C rises above a threshold value and control signal is biasing BJT on, overcurrent protection block will turn off BJT. Conservate design would keep BJT off until a manual reset had been done.

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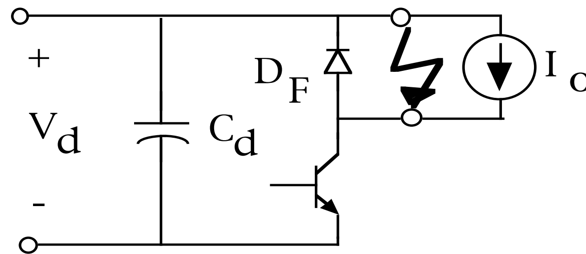
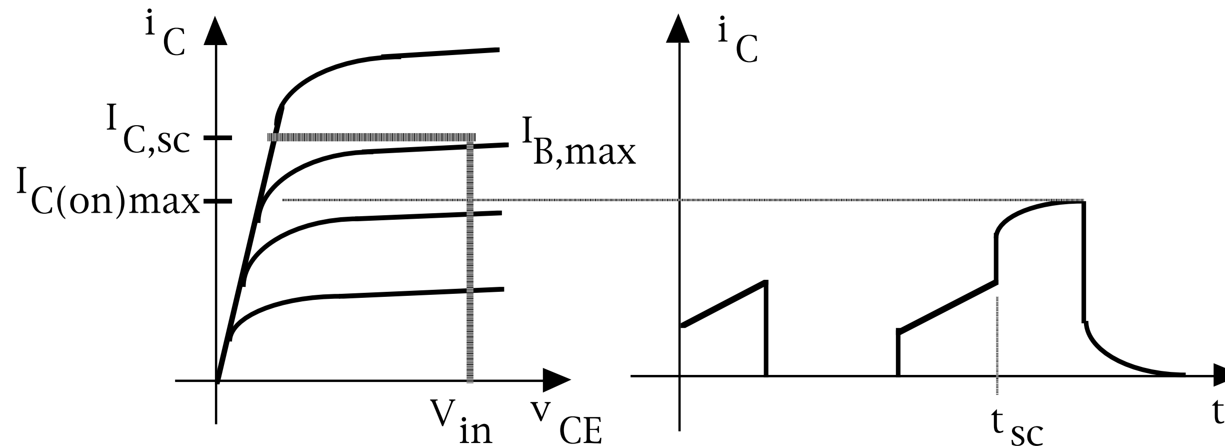
Limiting Overcurrents by Limiting On-state Base Current



- Stepdown converter with short curcuit at $t = t_{sc}$



- Overcurrent limited to $I_{C(on)max} < I_{C,sc}$ by keeping $I_{B,max} < I_{C,sc}/b$
- $I_{C,sc}$ = maximum allowable instantaneous collector current
- Same approach can be used with MOSFETs and IGBTs. V_{GS} mustbe restricted to keep drain current to safe values.

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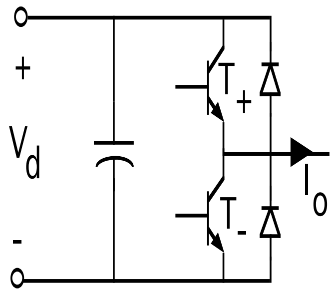
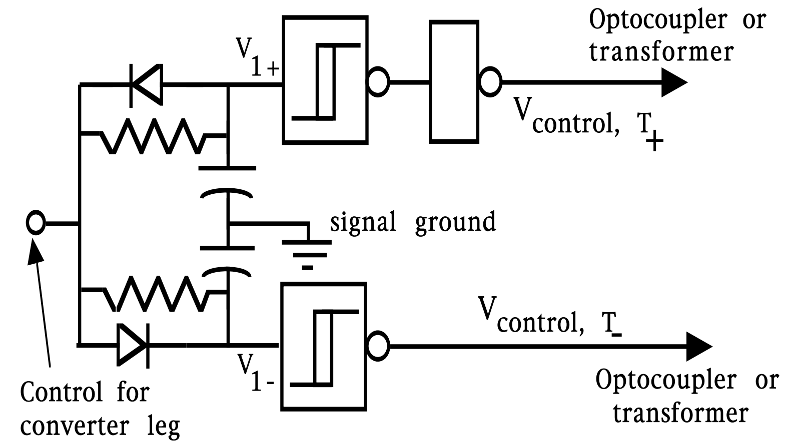
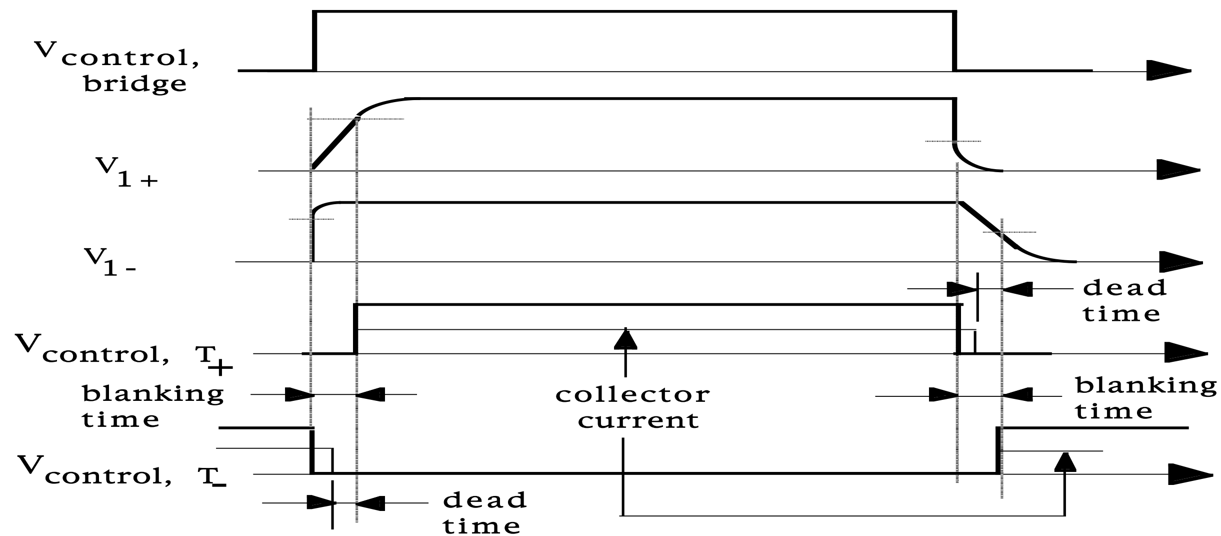
Blanking Times in Bridge Circuit Drives



- Turn off T+ before turning on T- in order to avoid cross-conduction (shorting out of Vd)





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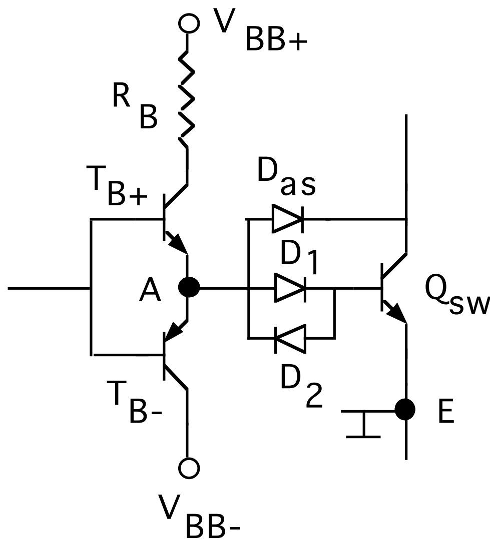
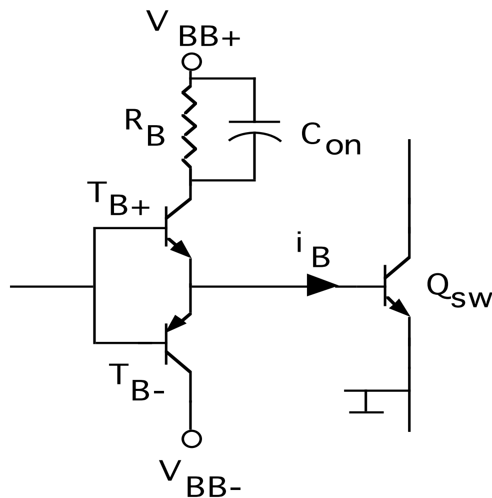
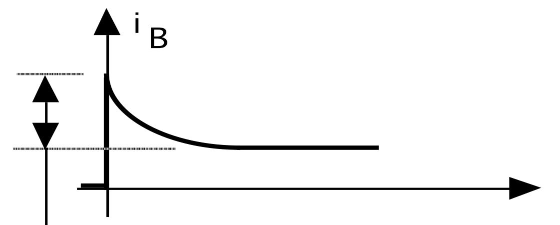
Drive Circuit Waveshaping for Improved Operation



- Anti-saturation diode D_{as} keeps Q_{sw} active.
  - $V_{AE} = V_{BE(on)} + V_{D1} = V_{CE(on)} + V_{das}$
  - $V_{CE(on)} = V_{BE(on)} > V_{CE(sat)}$ because $V_{D1} = V_{das}$
- D_s provides path for negative base current at Q_{sw} turn-off.
- Storage delay time at turn-off reduced but on-state losses increase slightly.

Speed-up capacitors





- Transient overdrive provided via C_{on} for faster turn-on of switch

- Same concept can be applied to MOSFET and IGBT drive circuits

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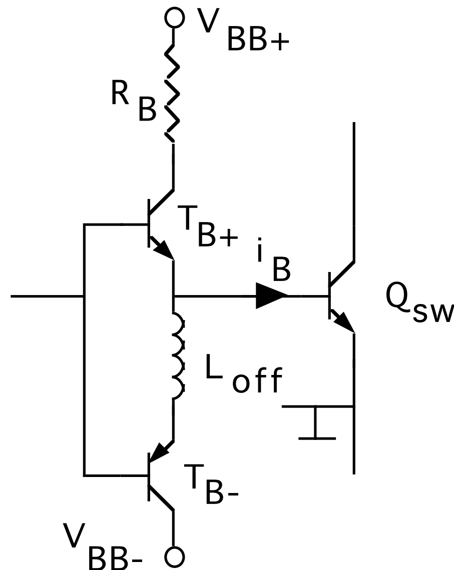
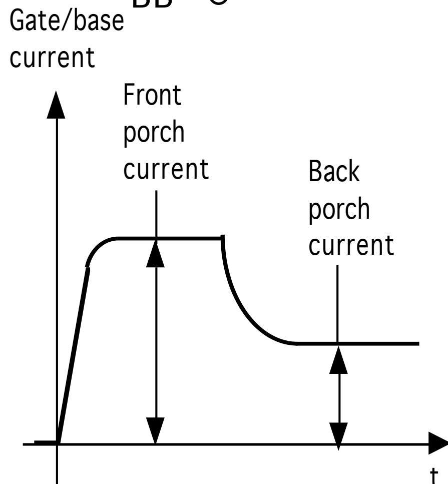
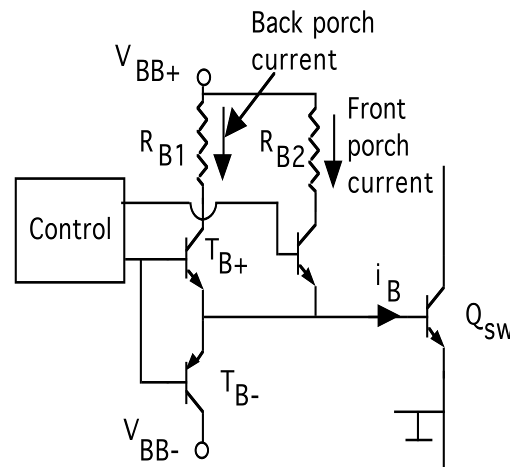
Drive Circuit Waveshaping (cont.)



Controlled rate of change of turn-off base current

- Excessively long collector current tailing time at BJT turn-off if $di_B(off)/dt$ is too large.
- Inductor L_{off} restricts $di_B(off)/dt$ to $- V_{BB}/L_{off}$





Front porch, back porch gate/base currents at turn-on

- Faster turn-on without putting device deeply into on-state where turn-off delay time will be substantially increased.
- Applicable to BJTs, MOSFETs, IGBTs, and GTOs.

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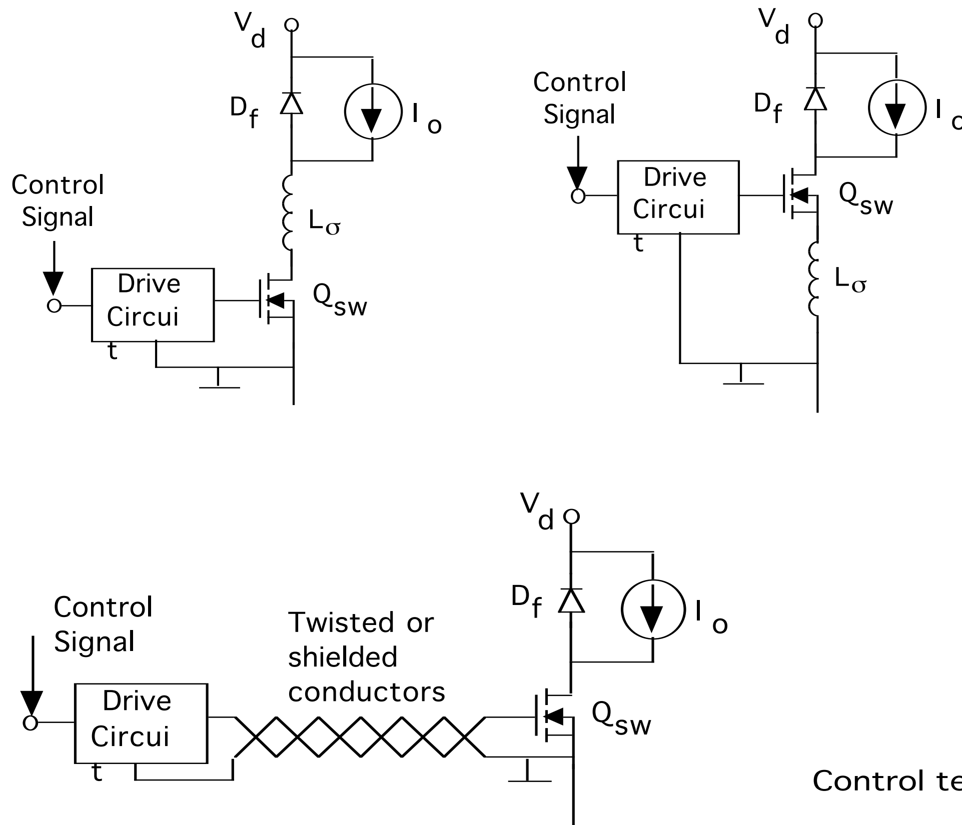
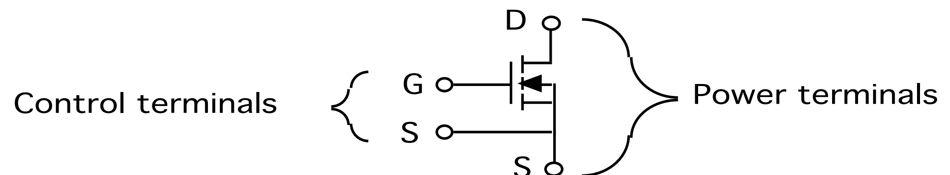
Circuit/Component Layout Considerations



Prime consideration is minimizing stray inductance

- Stray inductance in series with high-voltage side of power device Q_{sw} causes overvoltage at turn-off.
- Stray inductance in series with low-voltage side power device Q_{sw} can cause oscill-ations at turn-on and turn-off.
- One cm of unshielded lead has about 5 nH of series inductance.
- Keep unshielded lead lengths to an absolute minimum.



Use shielded conductors to connect drive circuit to power switch if there must be any appreciable separation (few cm or more) between them

Some power devices provided with four leads, two input leads and two power leads, to minimize stray inductance in input circuit.

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Lecture Notes

Heat Sinks and Component Temperature Control

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Need for Component Temperature Control

- All components, capacitors, inductors and transformers, and semiconductor devices and circuits have maximum operating temperatures specified by manufacturer.
    - Component reliability decreases with increasing temperature.Semiconductor failure rate doubles for every 10 - 15 C increase in temperature above 50 C (approx. rule-of-thumb).
- High component operating temperatures have undesirable effects on components.

<u>Capacitors</u>

Electrolyte evaporation rate increases significantly with temperature increases and thus shortens lifetime.

<u>Magnetic Components</u>

- Losses (at constant power input) increase above 100 C
- Winding insulation (lacquer or varnish) degrades above 100 C

<u>Semconductors</u>

- Unequal power sharing in paralleled or seriesed devices.
- Reduction in breakdown voltage in some devices.
- Increase in leakage currents.
- Increase in switching times.

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Temperature Control Methods

- Control voltages across and current through components via good design practices.
  - Snubbers may be required for semiconductor devices.
  - Free-wheeling diodes may be needed with magnetic components.
- Use components designed by manufacturers to maximize heat transfer via convection and radiation from component to ambient.
  - Short heat flow paths from interior to component surface and large component surface area.
- Component user has responsibility to properly mount temperature-critical components on heat sinks.
  - Apply recommended torque on mounting bolts and nuts and use thermal grease between component and heat sink.
  - Properly design system layout and enclosure for adequate air flow so that heat sinks can operate properly to dissipate heat to the ambient.

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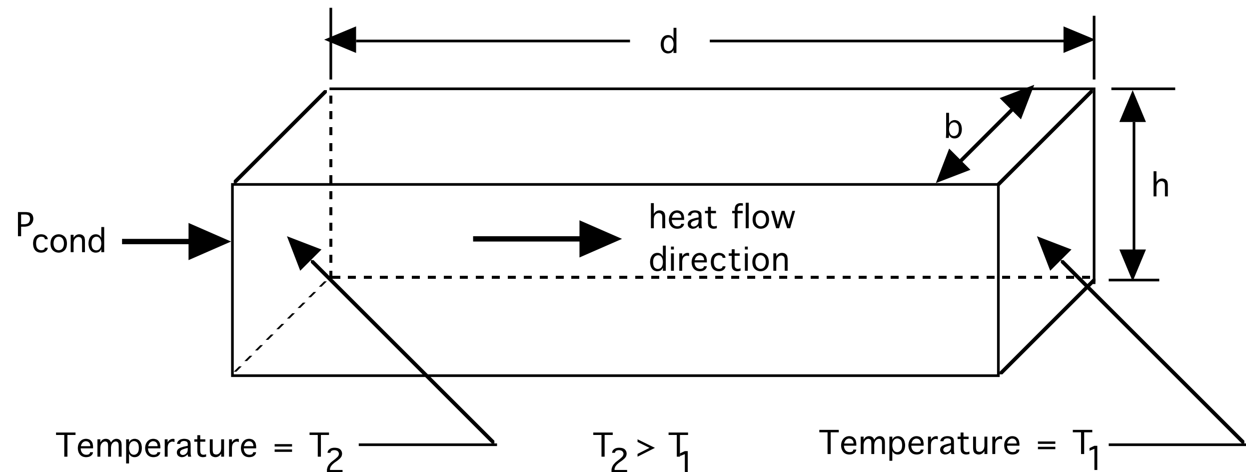
Heat Conduction Thermal Resistance

- Generic geometry of heat flow via conduction



- Heat flow P_{cond} [W/m^2] = $\lambda A (T_2 - T_1) / d$ = $(T_2 - T_1) / R_{\theta cond}$

- Thermal resistance $R_{\theta cond}$ = $d / [\lambda A]$
  - Cross-sectional area $A = hb$
  - λ = Thermal conductivity has units of W-m^{-1}- C^{-1} (λ_{Al} = 220 W-m^{-1}- C^{-1}).
  - Units of thermal resistance are C/W

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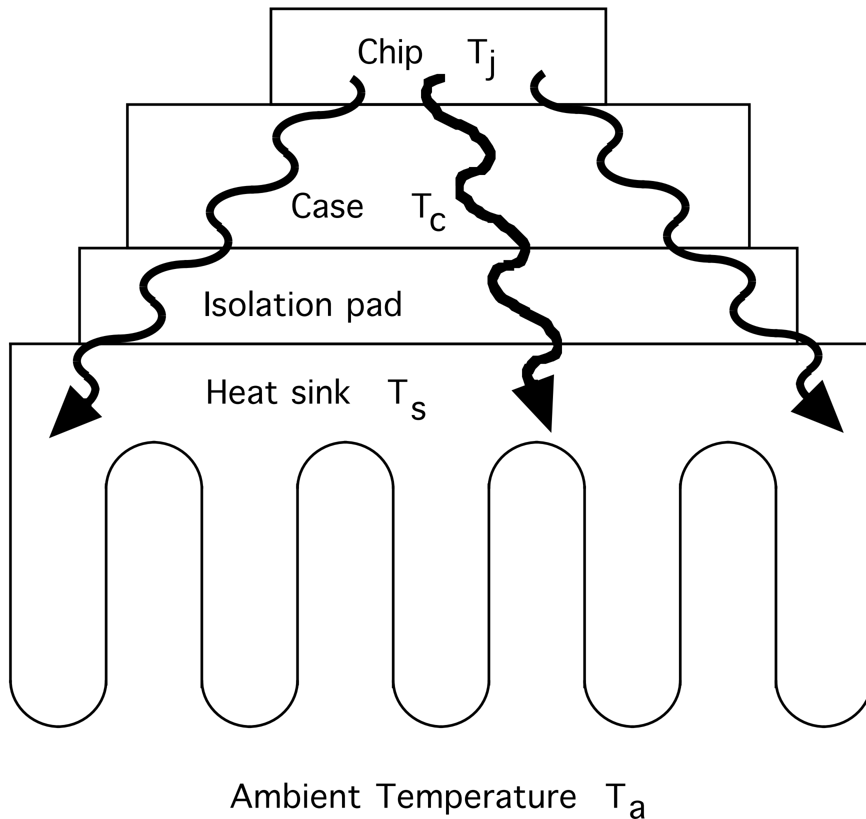
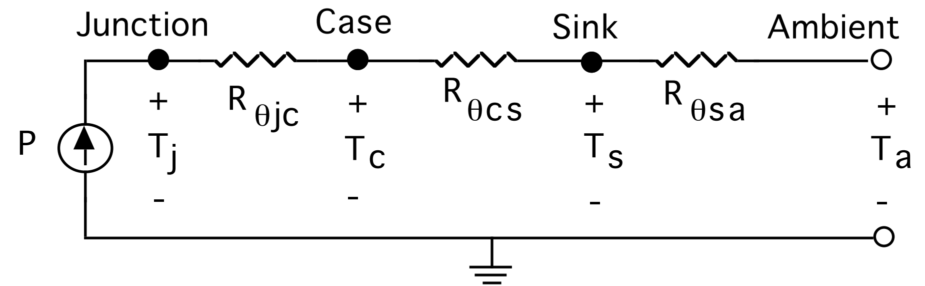
Thermal Equivalent Circuits

- Heat flow through a structure composed of layers of different materials.



- Thermal equivalent circuit simplifies calculation of temperatures in various parts of structure.



- $T_i = P_d\,(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) + T_a$

- If there parallel heat flow paths, then thermal resistances of the parallel paths combine as do electrical resistors in parallel.

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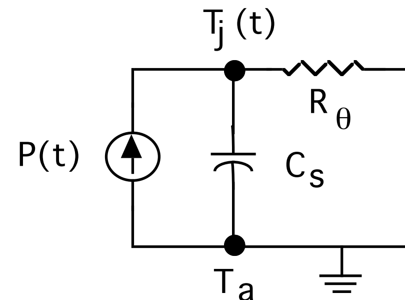
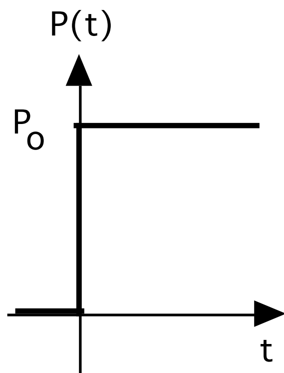
Transient Thermal Impedance

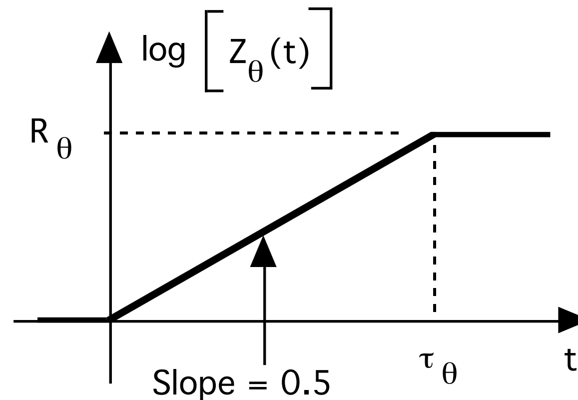
- Heat capacity per unit volume Cv = dQ/dT [Joules / C] prevents short duration high power dissipation surges from raising component temperature beyond operating limits.

  - Transient thermal equivalent circuit. $C_s = C_v V$ where V is the volume of the component.



- Transient thermal impedance $Z_\theta(t) = [T_j(t) - T_a]/P(t)$





- $\tau_\theta = \pi R_\theta C_s / 4$ = thermal time constant

- $T_j(t = \tau_\theta) = 0.833 \, P_o R_\theta$

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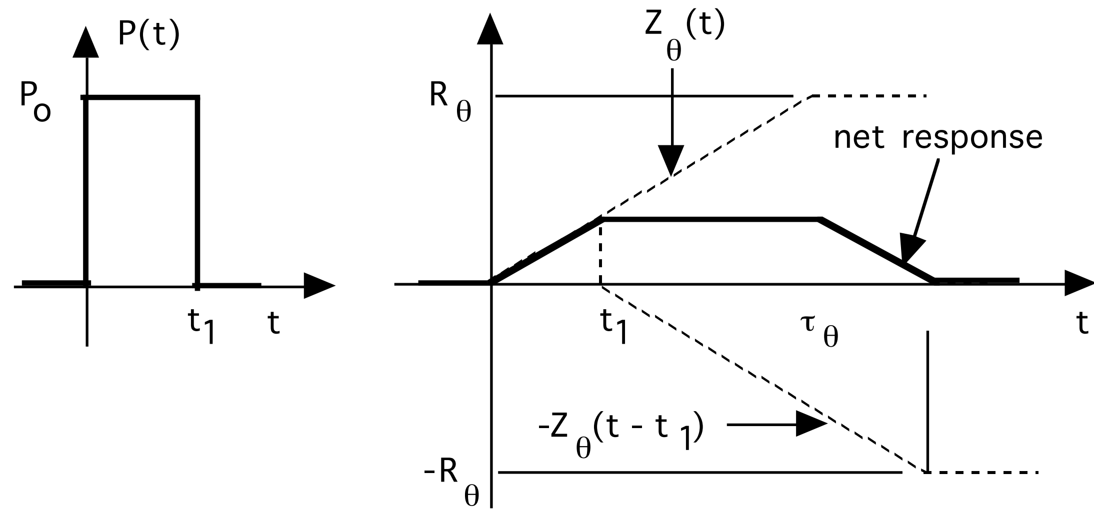
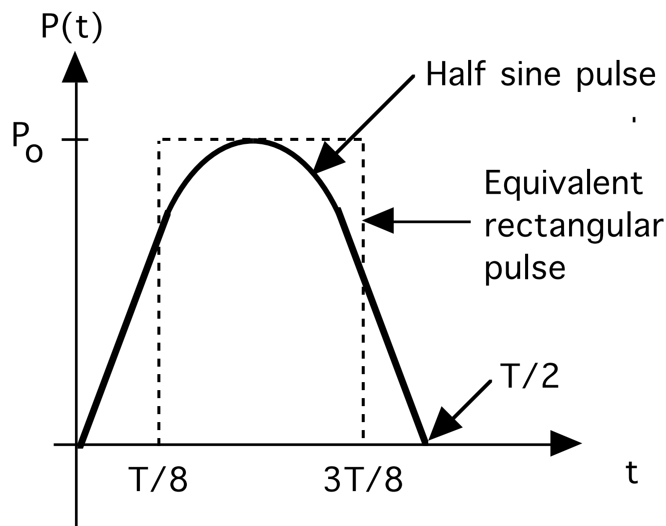
Application of Transient Thermal Impedance

- Symbolic response for a rectangular power dissipation pulse $P(t) = Po\ \{u(t) - u(t - t_1)\}$.

- $T_j(t) = Po\ \{\ Z_\theta(t) - Z_\theta(t - t_1)\ \}$





- Symbolic solution for half sine power dissipation pulse.
  - $P(t) = P_o\ \{u(t - T/8) - u(t - 3T/8)\}$; area under two curves identical.
  - $T_j(t) = Po\ \{\ Z_\theta(t - T/8) - Z_\theta(t - 3T/8)\ \}$

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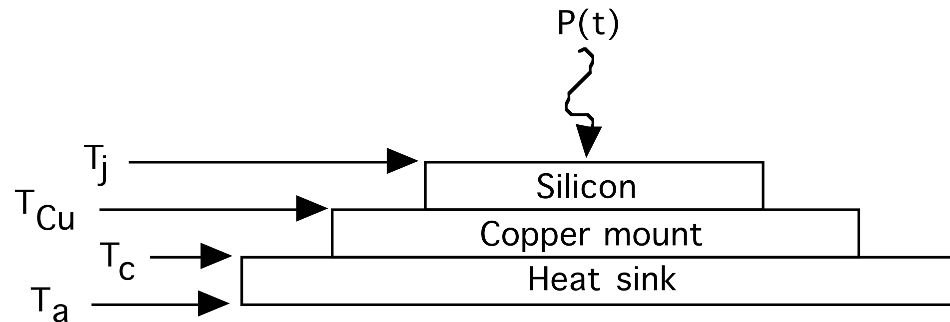
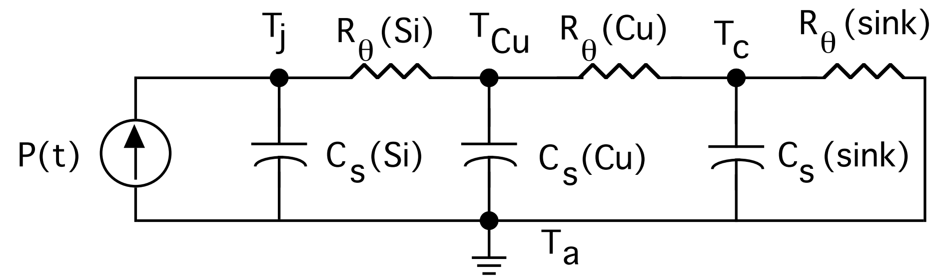
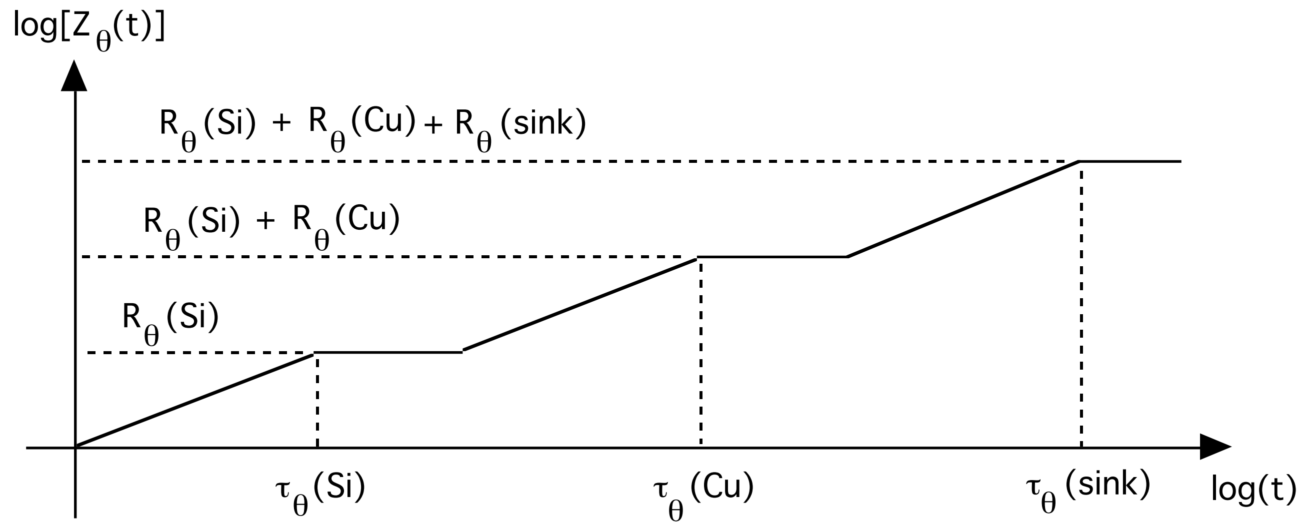
Z_θ for Multilayer Structures

- Multilayer geometry



- Transient thermal equivalent circuit





- Transient thermal impedance (asymptotic) of multilayer structure assuming widely separated thermal time constants.

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Heat Sinks

- Aluminum heat sinks of various shapes and sizes widely available for cooling components.
  - Often anodized with black oxide coating to reduce thermal resistance by up to 25%.
  - Sinks cooled by natural convection have thermal time constants of 4 - 15 minutes.
  - Forced-air cooled sinks have substantially smaller thermal time constants, typically less than one minute.
- Choice of heat sink depends on required thermal resistance, $R_{\theta sa}$, which is determined by several factors.
  - Maximum power, P_{diss}, dissipated in the component mounted on the heat sink.
  - Component's maximum internal temperature, $T_{j,max}$
  - Component's junction-to-case thermal resistance, $R_{\theta jc}$.
  - Maximum ambient temperature, $T_{a,max}$.
- $R_{\theta sa} = \{T_{j,max} - T_{a,max}\}P_{diss} - R_{\theta jc}$
  - P_{diss} and $T_{a,max}$ determined by particular application.
  - $T_{j,max}$ and $R_{\theta jc}$ set by component manufacturer.

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Radiative Thermal Resistance

- Stefan-Boltzmann law describes radiative heat transfer.
  - $P_{rad} = 5.7x10^{-8} EA [(T_s)^4 -(T_a)^4]$; $[P_{rad}]$ = [watts]
  - E = emissivity; black anodized aluminum E = 0.9 ; polished aluminum E = 0.05
  - A = surface area [m^2]through which heat radiation emerges.
  - T_s = surface temperature [K] of component. T_a = ambient temperature [K].

- $(T_s - T_a)/Prad = R_{\theta,rad} = [T_s - T_a][5.7EA \{(T_s/100)^4 -(T_a/100)^4 \}]^{-1}$

- Example - black anodized cube of aluminum 10 cm on a side. T_s = 120 C and T_a = 20 C
  - $R_{\theta,rad} = [393 - 293][(5.7) (0.9)(6x10-2)\{(393/100)^4 - (293/100)^4 \}]^{-1}$
  - $R_{\theta,rad}$ = 2.2 C/W

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Convective Thermal Resistance

- P_{conv} = convective heat loss to surrounding air from a vertical surface at sea level having a height d_{vert} [in meters] less than one meter.
  - $P_{conv} = 1.34\ A\ [Ts - Ta]^{1.25}\ d_{vert}^{-0.25}$
  - A = total surface area in [m^2]
  - T_s = surface temperature [K] of component. T_a = ambient temperature [K].
- $[T_s - T_a]/P_{conv} = R_{\theta,conv} = [T_s - T_a]\ [d_{vert}]^{0.25}[1.34\ A\ (T_s - T_a)^{1.25}]^{-1}$
  - $R_{\theta,conv} = [d_{vert}]^{0.25}\ \{1.34\ A\ [T_s - T_a]^{0.25}\}^{-1}$
- Example - black anodized cube of aluminum 10 cm on a side. T_s = 120 C and T_a = 20 C.
  - $R_{\theta,conv} = [10^{-1}]0.25([1.34]\ [6x10^{-2}]\ [120 - 20]^{0.25})^{-1}$
  - $R_{\theta,conv}$ = 2.2 C/W

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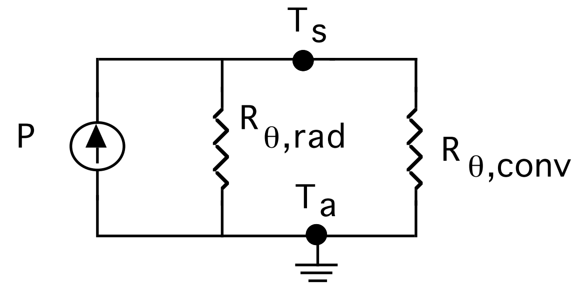
Combined Effects of Convection and Radiation

- Heat loss via convection and radiation occur in parallel.
  - Steady-state thermal equivalent circuit



  - $R_{\theta,sink} = R_{\theta,rad} R_{\theta,conv} / [R_{\theta,rad} + R_{\theta,conv}]$

- Example - black anodized aluminum cube 10 cm per side
  - $R_{\theta,rad}$ = 2.2 C/W and $R_{\theta,conv}$ = 2.2 C/W
  - $R_{\theta,sink}$ = (2.2) (2.2) /(2.2 + 2.2) = 1.1 C/W

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Design of Magnetic Components

Outline

A. Inductor/Transformer Design Relationships

B. Magnetic Cores and Materials

C. Power Dissipation in Copper Windings

D. Thermal Considerations

E. Analysis of Specific Inductor Design

F. Inductor Design Procedures

G. Analysis of Specific Transformer Design

H. Eddy Currents

J. Transformer Leakage Inductance

K. Transformer Design Procedures

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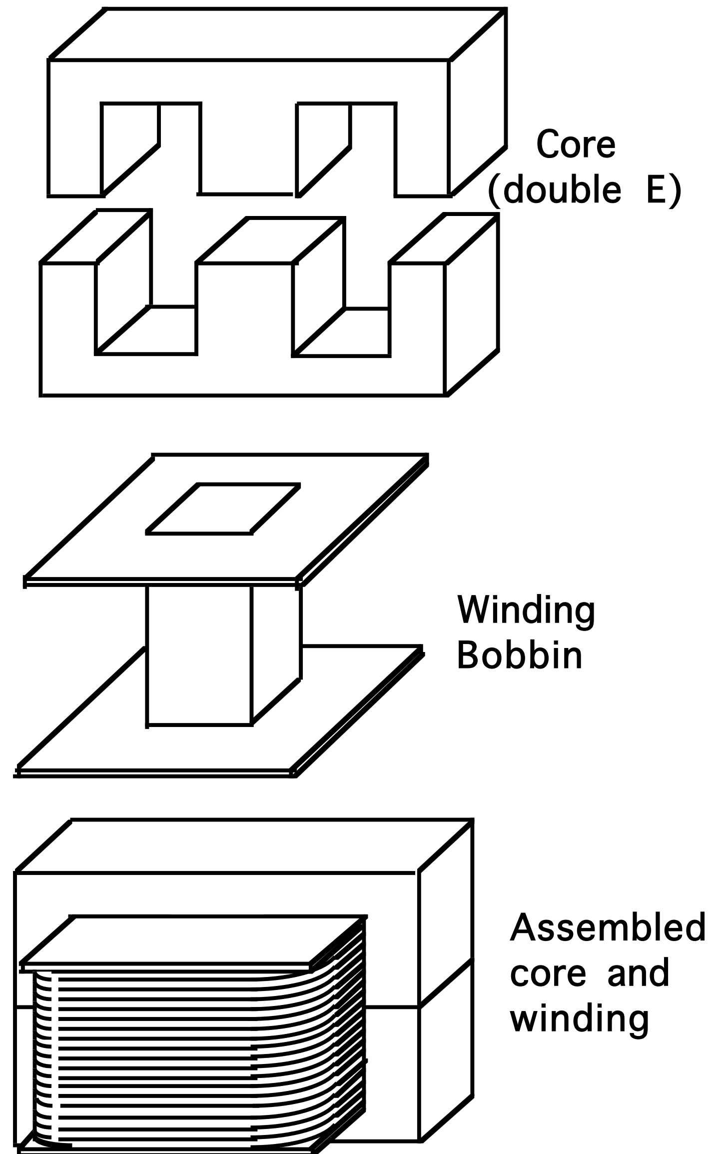
Magnetic Component Design Responsibility of Circuit Designer

- Ratings for inductors and transformers in power electronic circuits vary too much for commercial vendors to stock full range of standard parts.
- Instead only magnetic cores are available in a wide range of sizes, geometries, and materials as standard parts.
- Circuit designer must design the inductor/transformer for the particular application.
- Design consists of:

1. Selecting appropriate core material, geometry, and size
2. Selecting appropriate copper winding parameters: wire type, size, and number of turns.



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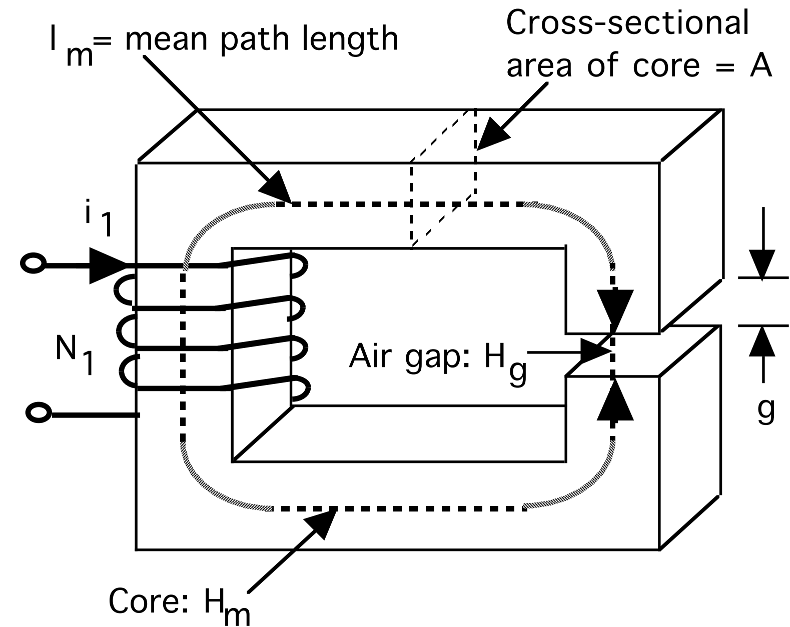
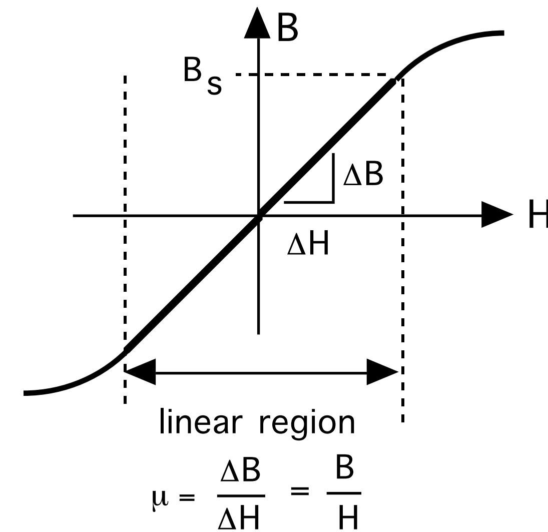
Review of Inductor Fundamentals

- Assumptions
  - No core losses or copper winding losses
  - Linearized B-H curve for core with $\mu_m >> \mu_o$
  - $l_m >> g$ and $A >> g^2$
  - Magnetic circuit approximations (flux uniform over core cross-section, no fringing flux)
- Starting equations
  - $H_m l_m + H_g g = N I$ (Ampere's Law)
  - $B_m A = B_g A = \phi$ (Continuity of flux assuming no leakage flux)
  - $\mu_m H_m = B_m$ (linearized B-H curve) ; $\mu_o H_g = B_g$
- Results
  - $B_s > B_m = B_g = \dfrac{NI}{l_m/\mu_m + g/\mu_o} = \phi/A$
  - $LI = N\phi$; $L = \dfrac{A N^2}{l_m/\mu_m + g/\mu_o}$





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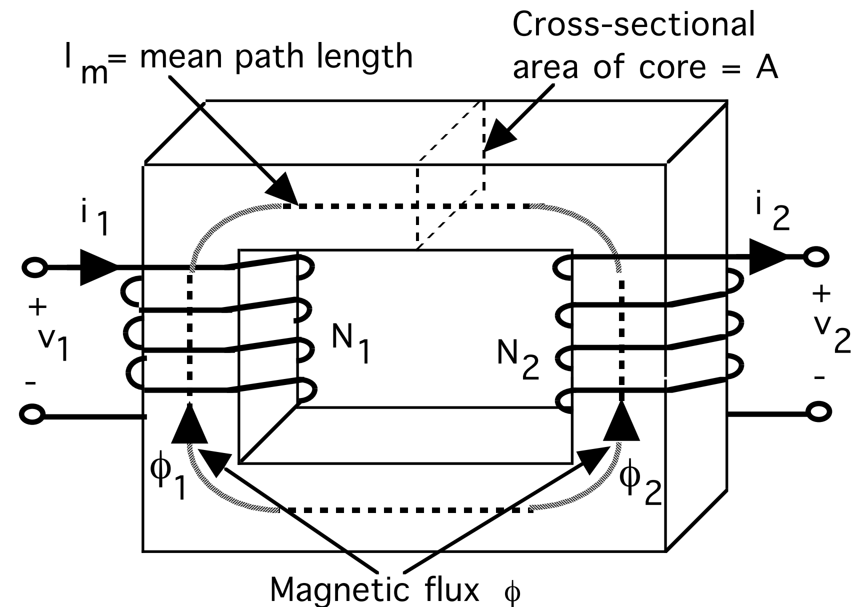
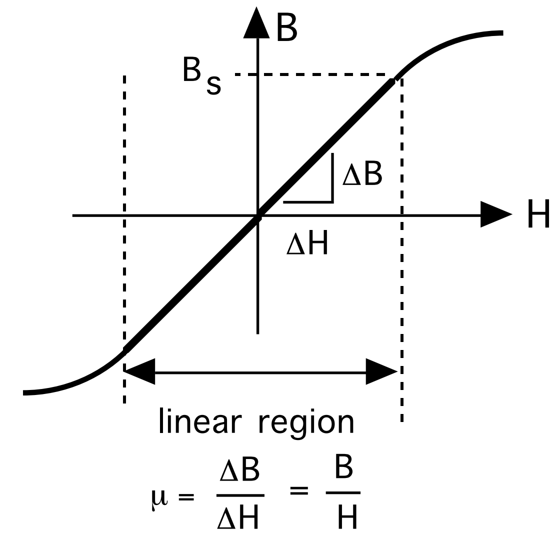
Review of Transformer Fundamentals

- Assumptions same as for inductor
- Starting equations
  - $H_1 L_m = N_1 I_1$; $H_2 L_m = N_2 I_2$ (Ampere's Law)
  - $H_m L_m = (H_1 - H_2) L_m = N_1 I_1 - N_2 I_2$
  - $\mu_m H_m = B_m$ (linearized B-H curve)
  - $v_1 = N_1 \frac{d\phi_1}{dt}$; $v_2 = N_2 \frac{d\phi_2}{dt}$ (Faraday's Law)
  - Net flux $\phi = \phi_1 - \phi_2 = \mu_m H_m A$ $= \frac{\mu_m A (N_1 I_1 - N_2 I_2)}{L_m}$



- Results assuming $\mu_m \Rightarrow \infty$, i.e. ideal core or ideal transformer approximation.
  - $\frac{\phi}{\mu_m} = 0$ and thus $N_1 I_1 = N_2 I_2$
  - $\frac{d(\phi_1 - \phi_2)}{dt} = 0 = \frac{v_1}{N_1} - \frac{v_2}{N_2}$; $\frac{v_1}{N_1} = \frac{v_2}{N_2}$



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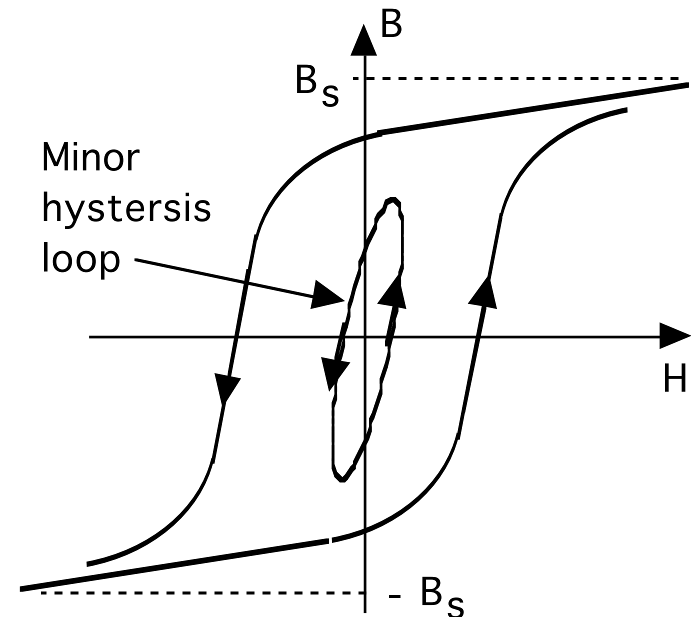
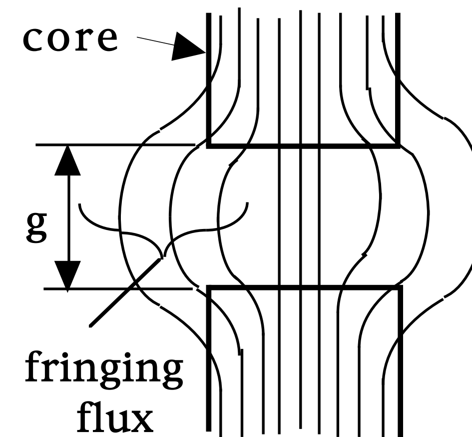
Current/Flux Density Versus Core Size

- Larger electrical ratings require larger current I and larger flux density B.
  - Core losses (hysteresis, eddy currents) increase as B^2 (or greater)
  - Winding (ohmic) losses increase as I^2 and are accentuated at high frequencies (skin effect, proximity effect)
- To control component temperature, surface area of component and thus size of component must be increased to reject increased heat to ambient.
  - At constant winding current density J and core flux density B, heat generation increases with volume V but surface area only increases as $V^{2/3}$.
  - Maximum J and B must be reduced as electrical ratings increase.
- Flux density B must be < B_s
  - Higher electrical ratings ⇒ larger total flux ⇒ larger component size
  - Flux leakage, nonuniform flux distribution complicate design





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Magnetic Component Design Problem

- Challenge - conversion of component operating specs in converter circuit into component design parameters.

- Goal - simple, easy-to-use procedure that produces component design specs that result in an acceptable design having a minimum size, weight, and cost.

- Inductor electrical (e.g.converter circuit) specifications.
  - Inductance value L
  - Inductor currents rated peak current I, rated rms current I_{rms} , and rated dc current (if any) I_{dc}
  - Operating frequency f.
  - Allowable power dissipation in inductor or equivalently maximum surface temperature of the inductor T_s and maximum ambient temperature T_a.

- Transformer electrical (converter circuit) specifications.
  - Rated rms primary voltage V_{pri}
  - Rated rms primary current I_{pri}
  - Turns ratio N_{pri}/N_{sec}
  - Operating frequency f
  - Allowable power dissipation in transformer or equivalently maximum temperatures T_s and T_a

- Design procedure outputs.
  - Core geometry and material.
  - Core size (A_{core} , A_w)
  - Number of turns in windings.
  - Conductor type and area A_{cu}.
  - Air gap size (if needed).

- Three impediments to a simple design procedure.

1. Dependence of J_{rms} and B on core size.

.

2. How to chose a core from a wide range of materials and geometries.

3. How to design low loss windings at high operating frequencies.

- Detailed consideration of core losses, winding losses, high frequency effects (skin and proximity effects), heat transfer mechanisms required for good design procedures.

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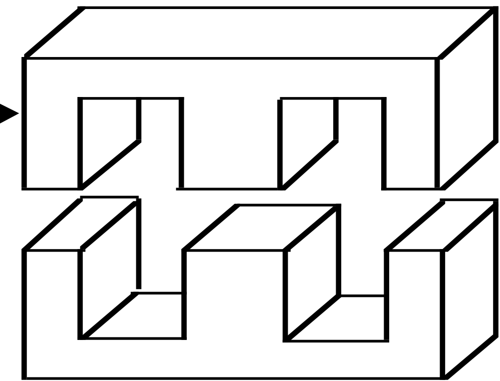
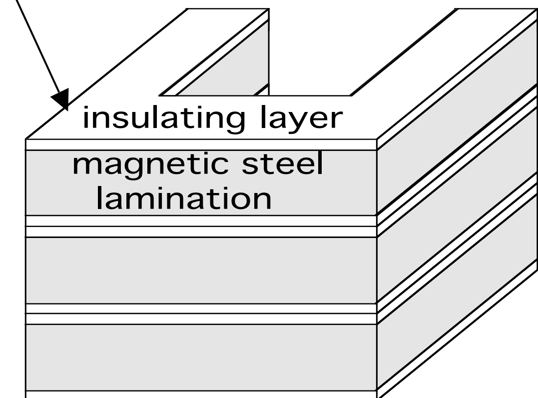
Core Shapes and Sizes

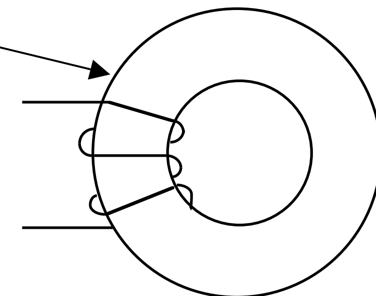
- Magnetic cores available in a wide variety of sizes and shapes.
  - Ferrite cores available as U, E, and I shapes as well as pot cores and toroids.
  - Laminated (conducting) materials available in E, U, and I shapes as well as tape wound toroids and C-shapes.
  - Open geometries such as E-core make for easier fabrication but more stray flux and hence potentially more severe EMI problems.
  - Closed geometries such as pot cores make for more difficult fabrication but much less stray flux and hence EMI problems.

- Bobbin or coil former provided with most cores.

- Dimensions of core are optimized by the manufacturer so that for a given rating (i.e. stored magnetic energy for an inductor or V-I rating for a transformer), the volume or weight of the core plus winding is minimized or the total cost is minimized.
  - Larger ratings require larger cores and windings.
  - Optimization requires experience and computerized optimization algorithm.
  - Vendors usually are in much better position to do the optimization than the core user.







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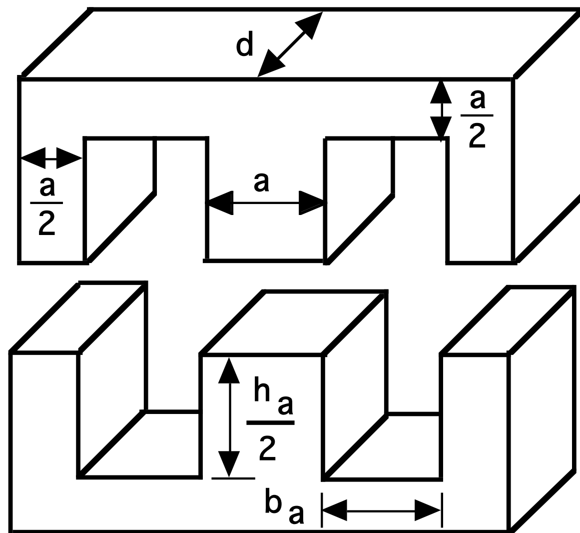
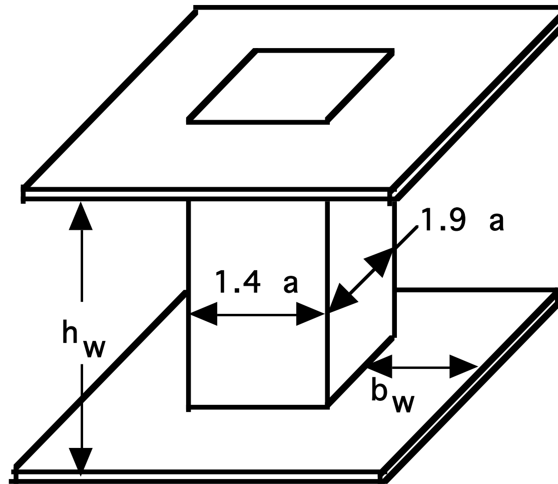
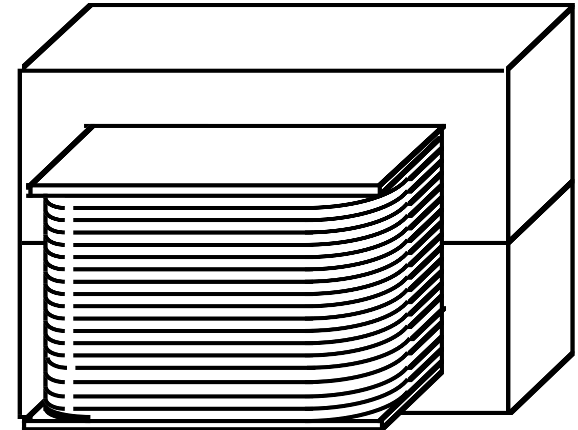
Double-E Core Example







Characteristic	Relative Size	Absolute Size for a = 1 cm
Core area A_{core}	$1.5\ a^2$	$1.5\ cm^2$
Winding area A_W	$1.4\ a^2$	$1.4\ cm^2$
Area product $AP = A_W A_c$	$2.1\ a^4$	$2.1\ cm^4$
Core volume V_{core}	$13.5\ a^3$	$13.5\ cm^3$
Winding volume V_W	$12.3a^3$	$12.3\ cm^3$
Total surface area of assembled core and winding	$59.6\ a^2$	$59.6\ cm^2$

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Types of Core Materials

- Iron-based alloys
  - Various compositions
    - Fe-Si (few percent Si)
    - Fe-Cr-Mn
    - METGLASS (Fe-B, Fe-B-Si, plus many other compositions)
  - Important properties
    - Resistivity _ = (10 - 100) ρ_{Cu}
    - B_s = 1 - 1.8 T (T = tesla = 10^4 oe)
  - METGLASS materials available only as tapes of various widths and thickness.
  - Other iron alloys available as laminations of various shapes.
  - Powdered iron can be sintered into various core shapes. Powdered iron cores have larger effective resistivities.

- Ferrite cores
  - Various compositions - iron oxides, Fe-Ni-Mn oxides
  - Important properties
    - Resistivity ρ very large (insulator) - no ohmic losses and hence skin effect problems at high frequencies.
    - B_s = 0.3 T (T = tesla = 10^4 oe)

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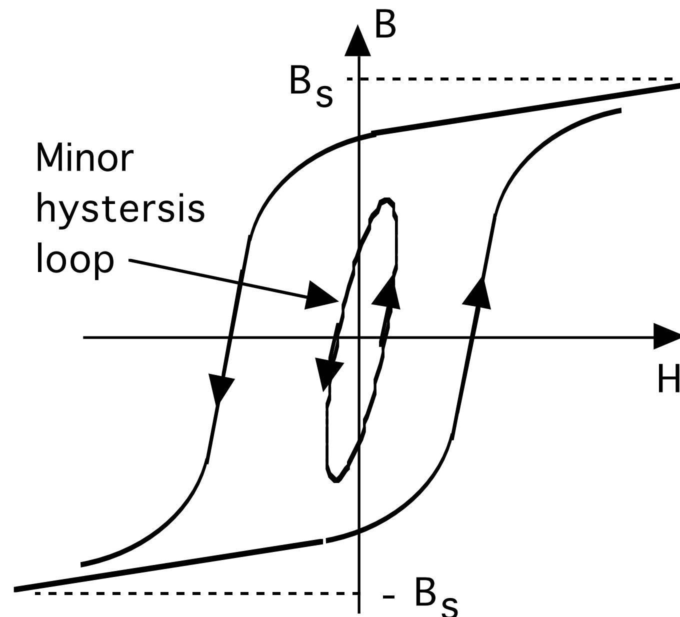
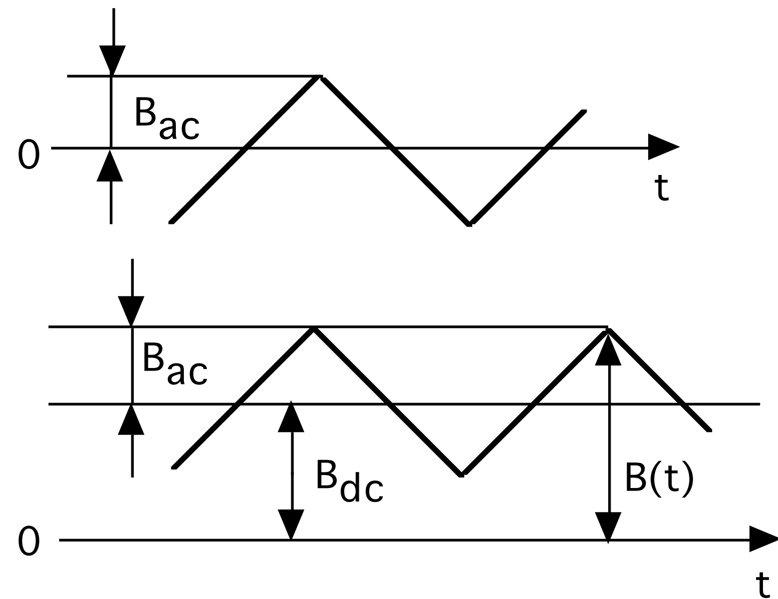
Hysteresis Loss in Magnetic Materials





- Area encompassed by hysteresis loop equals work done on material during one cycle of applied ac magnetic field. Area times frequency equals power dissipated per unit volume.

- Typical waveforms of flux density, B(t) versus time, in an inductor.
- Only B_{ac} contributes to hysteresis loss.

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Quantitative Description of Core Losses

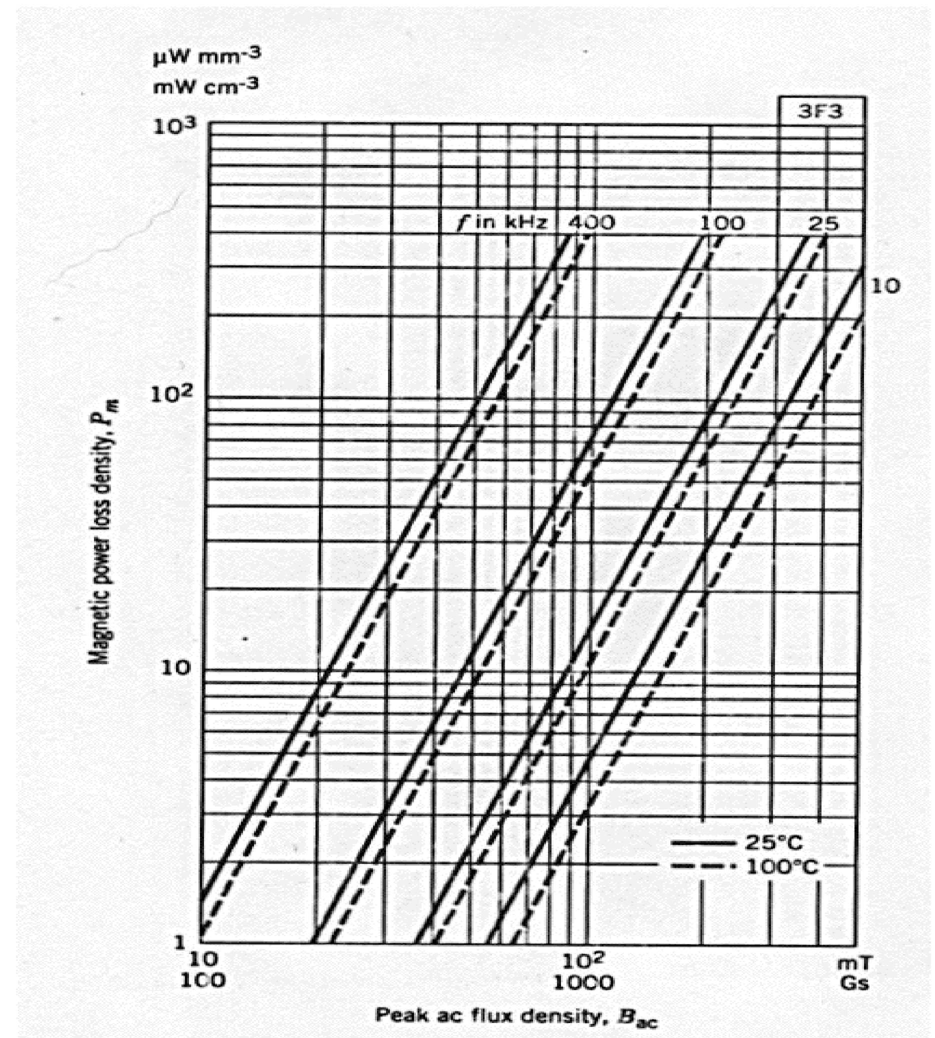
- Eddy current loss plus hysteresis loss = core loss.
- Empirical equation - $P_{m,sp} = k\, f^{a}\ [B_{ac}]^{d}$

.

f = frequency of applied field. B_{ac} = base-to-peak value of applied ac field. k, a, and d are constants which vary from material to material

  - $P_{m,sp} = 1.5\text{x}10^{-6}\ \ f^{1.3}\ \ [B_{ac}]^{2.5}$ mW/cm^3 for 3F3 ferrite. (f in kHz and B in mT)
  - $P_{m,sp} = 3.2\text{x}10^{-6}\ \ f^{1.8}\ \ [B_{ac}]^{2}$ mW/cm^3 METGLAS 2705M (f in kHz and B in mT)
  - Example: 3F3 ferrite with f = 100 kHz and B_{ac} = 100 mT, $P_{m,sp}$ = 60 mW/cm^3

- 3F3 core losses in graphical form.



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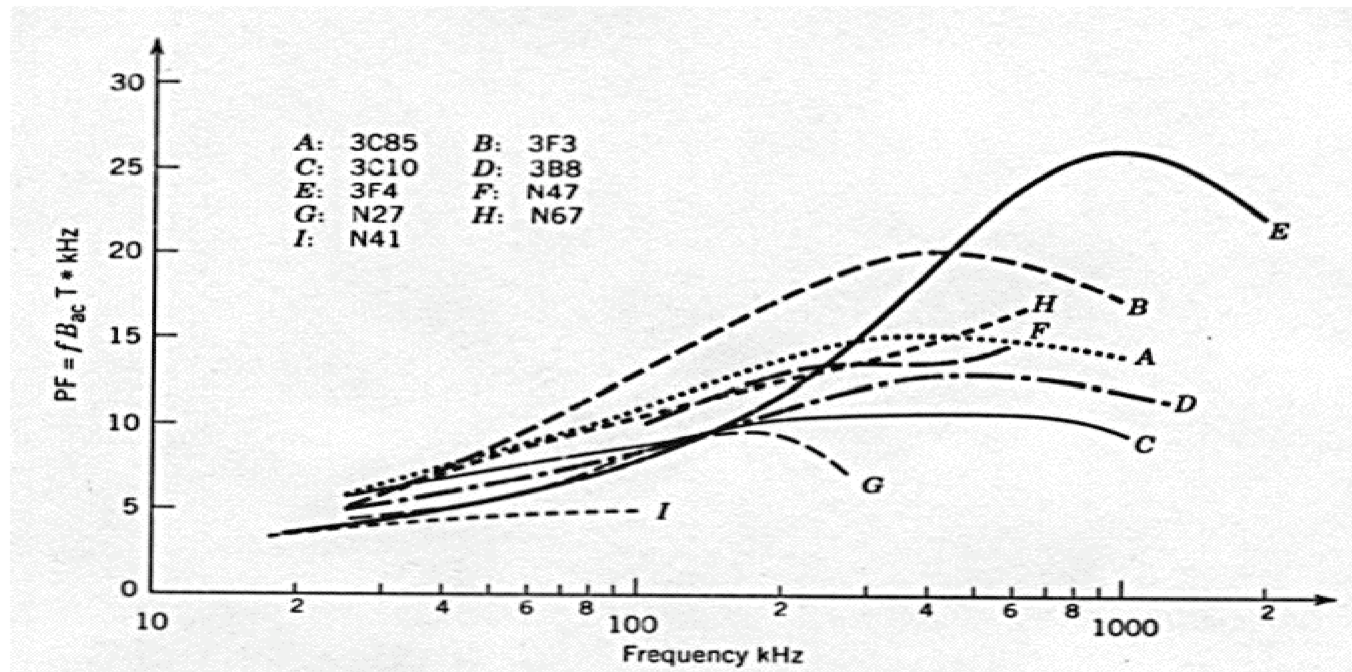
Core Material Performance Factor

- Volt-amp (V-A) rating of transformers proportional to f B_{ac}
- Core materials have different allowable values of B_{ac} at a specific frequency. B_{ac} limted by allowable $P_{m,sp}$.
- Most desirable material is one with largest B_{ac}.
- Choosing best material aided by defining an emperical performance factor PF = f B_{ac}. Plots of PF versus frequency for a specified value of $P_{m,sp}$ permit rapid selection of best material for an application.
- Plot of PF versus frequency at $P_{m,sp}$ = 100 mW/cm^3 for several different ferrites shown below.



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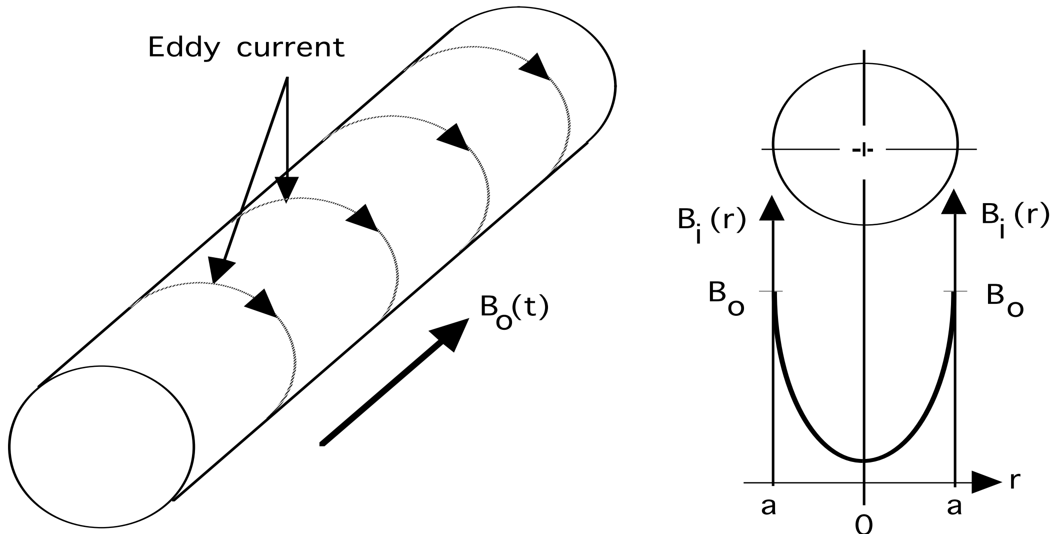
Eddy Current Losses in Magnetic Cores



- $\dfrac{B_i(r)}{B_o} = \exp(\{r - a\}/\delta)$
- δ = skin depth = $\sqrt{\dfrac{2}{\omega\mu\sigma}}$
  - $\omega = 2\pi f$, f = frequency
  - μ = magnetic permeability ; μ_o for magnetic materials.
  - σ = conductivity of materi
- AC magnetic fields generate eddy currents in conducting magnetic materials.
  - Eddy currents dissipate power.
  - Shield interior of material from magnetic field.
- Numerical example
  - $\sigma = 0.05\ \sigma_{cu}$; $\mu = 10^3\ \mu_o$ f = 100 Hz
  - δ = 1 mm

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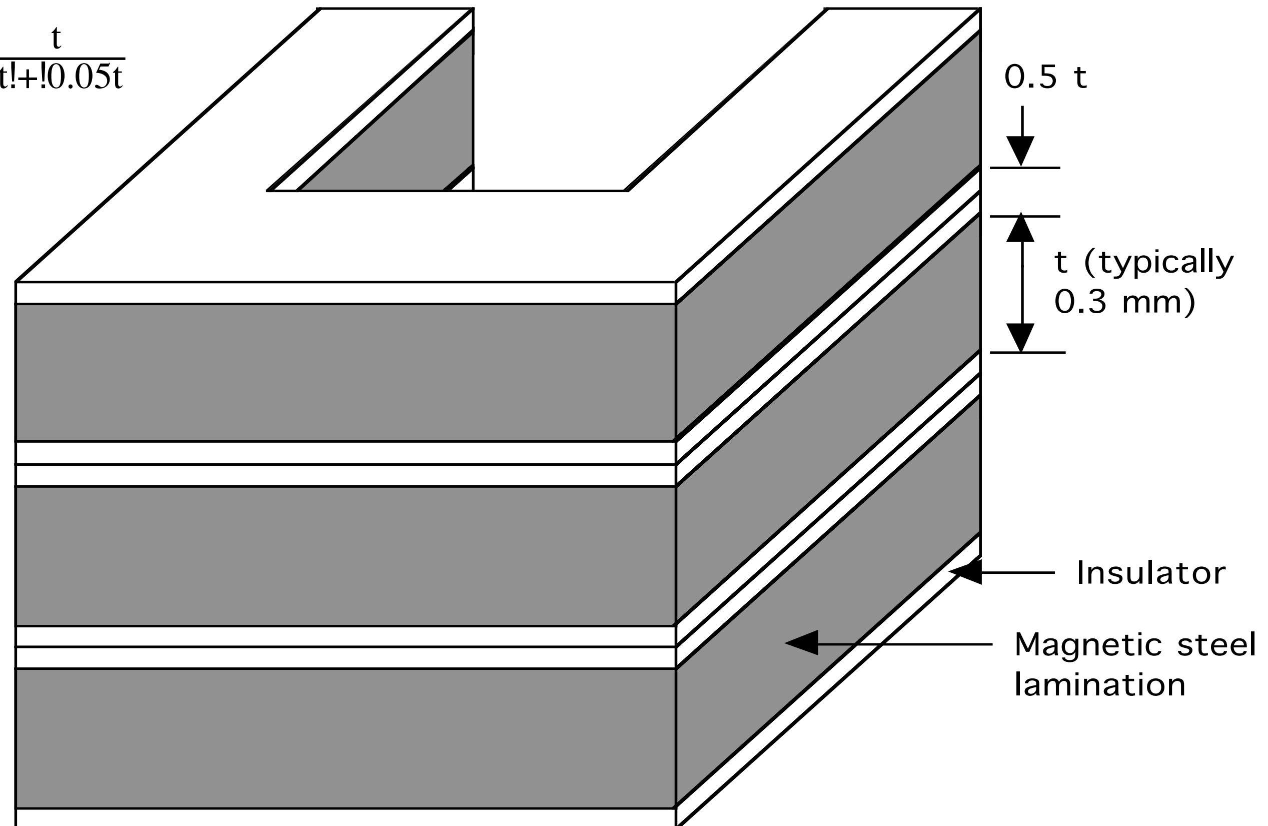
Laminated Cores

- Cores made from conductive magnetic materials must be made of many thin laminations. Lamination thickness < skin depth.

- Stacking factor $k_{stack} = \frac{t}{t + 0.05t}$



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Eddy Current Losses in Laminated Cores

- Flux $\phi(t)$ intercepted by current loop of area 2xw given by $\phi(t) = 2xwB(t)$
- Voltage in current loop $v(t) = 2xw\,\dfrac{dB(t)}{dt}$

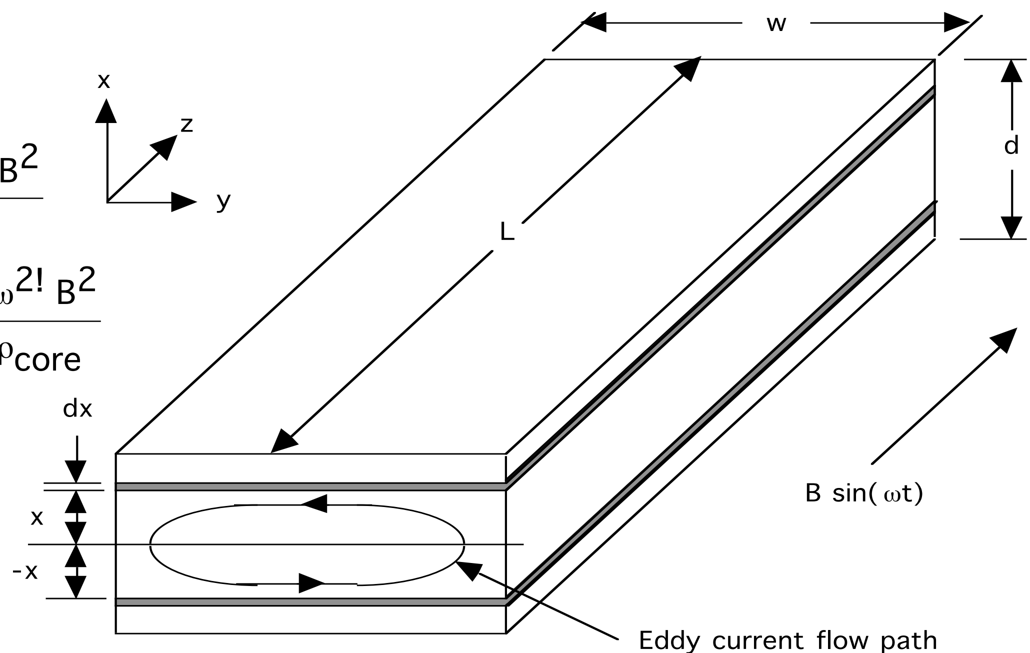
  $= 2wx\omega B\cos(\omega t)$
- Current loop resistance $r = \dfrac{2w\rho_{core}}{L!\ dx}$; $w >> d$
- Instantaneous power dissipated in thin loop

  $\delta p(t) = \dfrac{[v(t)]^2}{r}$
- Average power P_{ec} dissipated in lamination

  given by $P_{ec} = <\int \delta p(t)dV> \; = \dfrac{w!\ L!\ d^{3!}\ \omega^{2!}\ B^2}{24!\rho_{core}}$
- $P_{ec,sp} = \dfrac{P_{ec}}{V} = \dfrac{w!\ L!\ d^{3!}\ \omega^{2!}\ B^2}{24!\rho_{core}}\ \dfrac{1}{dwL} = \dfrac{d^{2!}\ \omega^{2!}\ B^2}{24!\rho_{core}}$

- Average power P_{ec} dissipated in lamination

  given by $P_{ec} = <\int \delta p(t)dV> \; = \dfrac{w!\ L!\ d^{3!}\ \omega^{2!}\ B^2}{24!\rho_{core}}$
- $P_{ec,sp} = \dfrac{P_{ec}}{V} = \dfrac{w!\ L!\ d^{3!}\ \omega^{2!}\ B^2}{24!\rho_{core}}\ \dfrac{1}{dwL} = \dfrac{d^{2!}\ \omega^{2!}\ B^2}{24!\rho_{core}}$



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Power Dissipation in Windings

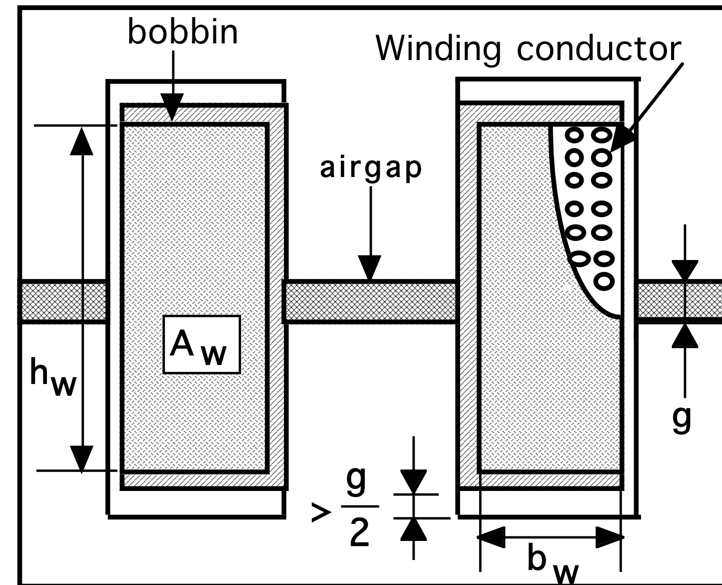
- Average power per unit volume of copper dissipated in copper winding = $P_{cu,sp} = \rho_{cu} (J_{rms})^2$ where $J_{rms} = I_{rms}/A_{cu}$ and ρ_{cu} = copper resistivity.

- Average power dissipated per unit volume of winding = $P_{w,sp} = k_{cu} \rho_{cu} (J_{rms})^2$; $V_{cu} = k_{cu} V_w$ where V_{cu} = total volume of copper in the winding and V_w = total volume of the winding.

- Copper fill factor $k_{cu} = \frac{N!A_{cu}}{A_w} < 1$

  - N = number of turns; A_{cu} = cross-sectional area of copper conductor from which winding is made; $A_w = b_w l_w$ = area of winding window.

  - k_{cu} = 0.3 for Leitz wire; k_{cu} = 0.6 for round conductors; $k_{cu} \Rightarrow$ 0.7-0.8 for rectangular conductors.



Double-E core example

- $k_{cu} < 1$ because:

  - Insulation on wire to avoid shorting out adjacent turns in winding.

  - Geometric restrictions. (e.g. tight-packed circles cannot cover 100% of a square area.)

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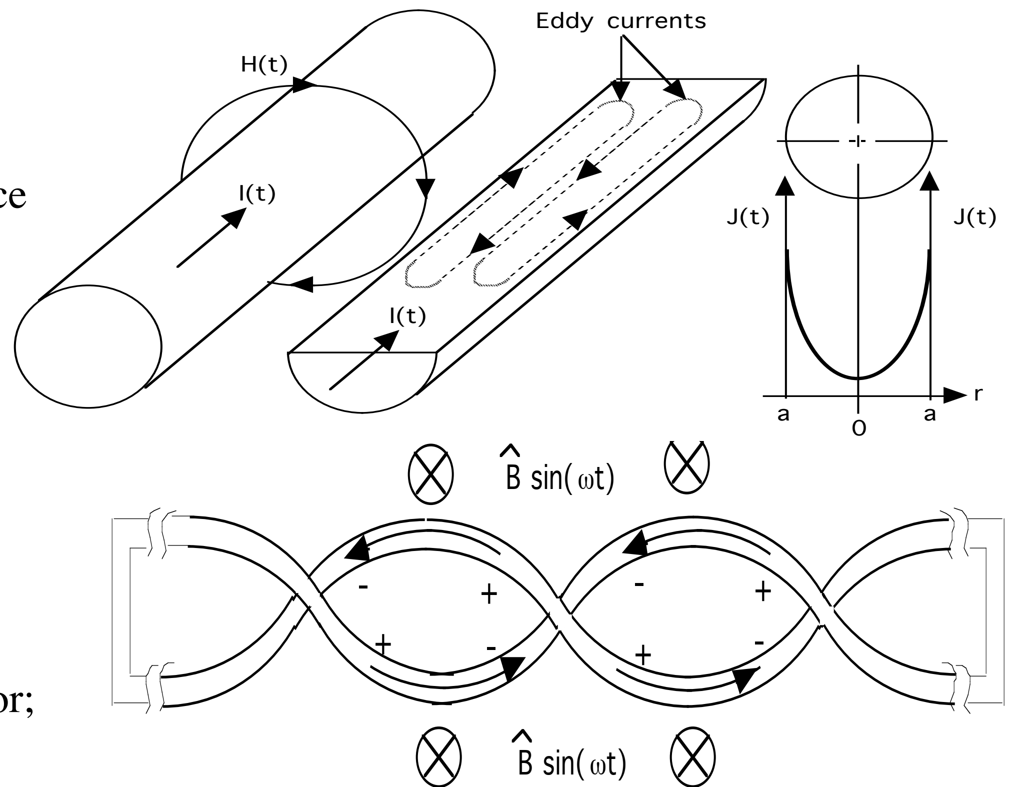
Eddy Currents Increase Winding Losses

- AC currents in conductors generate ac magnetic fields which in turn generate eddy currents that cause a nonuniform current density in the conductor . Effective resistance of conductor increased over dc value.
  - $P_{w,sp} > k_{cu} \rho_{cu} (J_{rms})^2$ if conductor dimensions greater than a skin depth.
  - $\frac{J(r)}{J_o} = \exp(\{r - a\}/\delta)$
  - δ = skin depth = $\sqrt{\frac{2}{\omega\mu\sigma}}$
    - $\omega = 2\pi f$, f = frequency of ac current
    - μ = magnetic permeability of conductor; $\mu = \mu_o$ for nonmagnetic conductors.
    - σ = conductivity of conductor material.



- Numerical example using copper at 100 C

Frequency	50 Hz	5 kHz	20 kHz	500 kHz
Skin Depth	10.6 mm	1.06 mm	0.53 mm	0.106 mm

- Mnimize eddy currents using Leitz wire bundle. Each conductor in bundle has a diameter less than a skin depth.
- Twisting of paralleled wires causes effects of intercepted flux to be canceled out between adjacent twists of the conductors. Hence little if any eddy currents.

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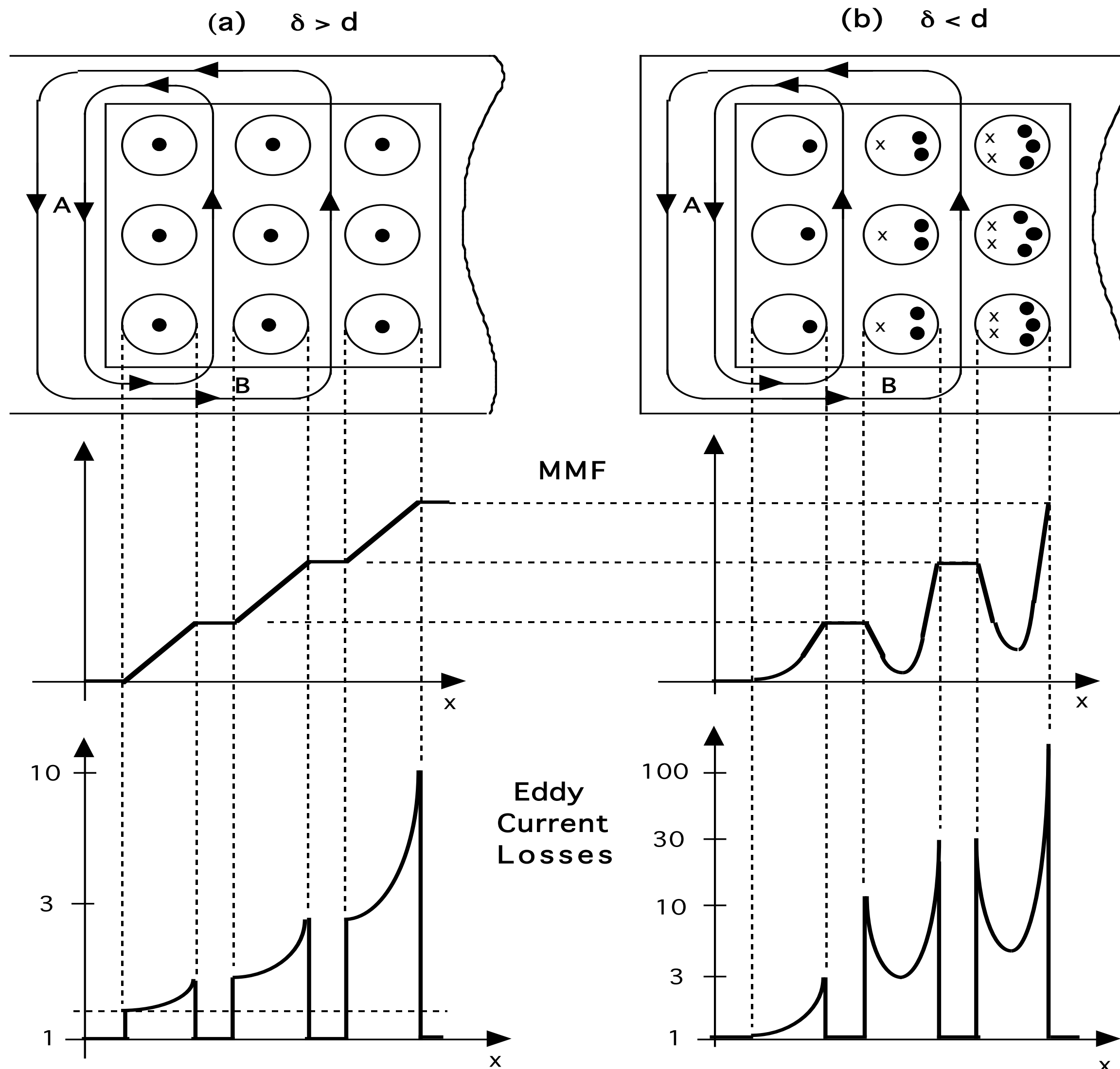
Proximity Effect Further Increases Winding Losses



- Proximity effect - losses due to eddy current generated by the magnetic field experienced by a particular conductor section but generated by the current flowing in the rest of the winding.

- Design methods for minimizing proximity effect losses discussed later.

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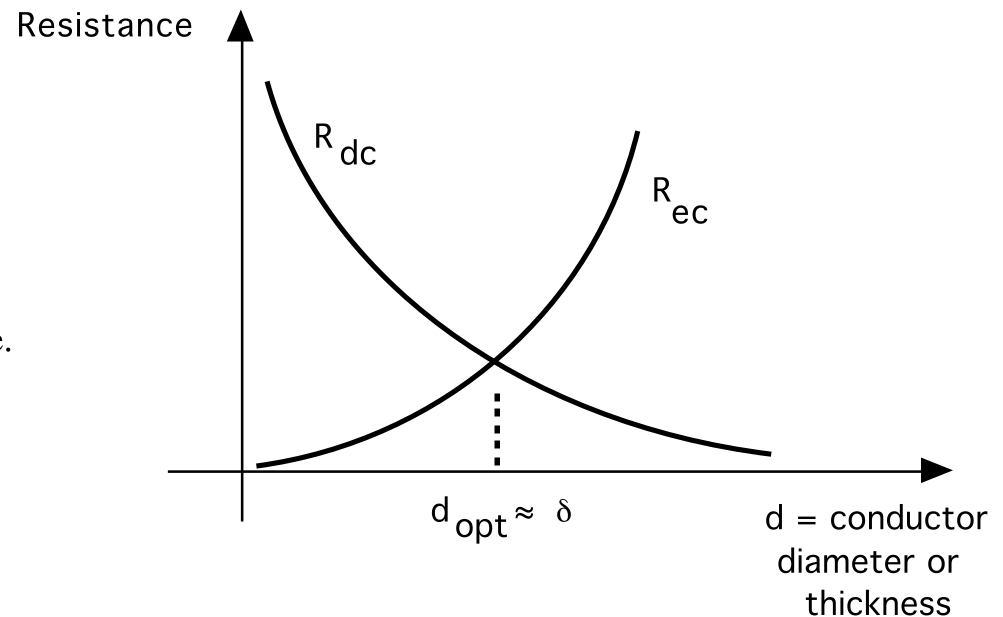
Minimum Winding Loss

- $P_w = P_{dc} + P_{ec}$; P_{ec} = eddy current loss.
- $P_w = \{ R_{dc} + R_{ec}\} [I_{rms}]^2 = R_{ac} [I_{rms}]^2$
- $R_{ac} = F_R \; R_{dc} = [1 + R_{ec}/R_{dc}] \, R_{dc}$
- Minimum winding loss at optimum conductor size.
  - $P_w = 1.5 \, P_{dc}$
  - $P_{ec} = 0.5 \, P_{dc}$
- High frequencies require small conductor sizes minimize loss.
- P_{dc} kept small by putting may small-size conductors in parallel using Litz wire or thin but wide foil conductors.



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Thermal Considerations in Magnetic Components

- Losses (winding and core) raise core temperature. Common design practice to limit maximum interior temperature to 100-125 °C.
  - Core losses (at constant flux density) increase with temperature increases above 100 °C
  - Saturation flux density B_s decreases with temp. Increases
  - Nearby components such as power semi-conductor devices, integrated circuits, capacitors have similar limits.
- Temperature limitations in copper windings
  - Copper resistivity increases with temperature increases. Thus losses, at constant current density increase with temperature.
  - Reliability of insulating materials degrade with temperature increases.
- Surface temperature of component nearly equal to interior temperature. Minimal temperature gradient between interior and exterior surface.
  - Power dissipated uniformly in component volume.
  - Large cross-sectional area and short path lengths to surface of components.
  - Core and winding materials have large thermal conductivity.
- Thermal resistance (surface to ambient) of magnetic component determines its temperature.
- $P_{sp} = \frac{T_s - T_a}{R_{\theta sa}(V_w + V_c)}$; $R_{\theta sa} = \frac{h}{A_s}$
  - h = convective heat transfer coefficient = 10 C-m^2/W
  - A_s = surface area of inductor (core + winding). Estimate using core dimensions and simple geometric considerations.
  - Uncertain accuracy in h and other heat transfer parameters do not justify more accurate thermal modeling of inductor.

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Scaling of Core Flux Density and Winding Current Density

- Power per unit volume, P_{sp}, dissipated in magnetic component is $P_{sp} = k_1/a$; k_1 = constant and a = core scaling dimension.
- $P_{w,sp} V_w + P_{m,sp} V_m = \frac{T_s - T_a}{R_{\theta sa}}$: T_a = ambient temperature and $R_{\theta sa}$ = surface-to-ambient thermal resistance of component.
- For optimal design $P_{w,sp} = P_{c,sp} = P_{sp}$: Hence $P_{sp} = \frac{T_s - T_a}{R_{\theta sa}(V_w + V_c)}$
- $R_{\theta sa}$ proportional to a^2 and $(V_w + V_c)$ proportional to a^3
- $J_{rms} = \sqrt{\frac{P_{sp}}{k_{cu} r_{cu}}} = k_2 \frac{1}{\sqrt{k_{cu} a}}$; k_2 = constant
- $P_{m,sp} = P_{sp} = k f^b [B_{ac}]^d$; Hence $B_{ac} = \sqrt[d]{\frac{P_{sp}}{k f^b}} = \frac{k_3}{\sqrt[d]{f^b a}}$ where k_3 = constant
- Plots of J_{rms}, B_{ac}, and P_{sp} versus core size (scale factor a) for a specific core material, geometry, frequency, and $T_s - T_a$ value very useful for picking appropriate core size and winding conductor size.

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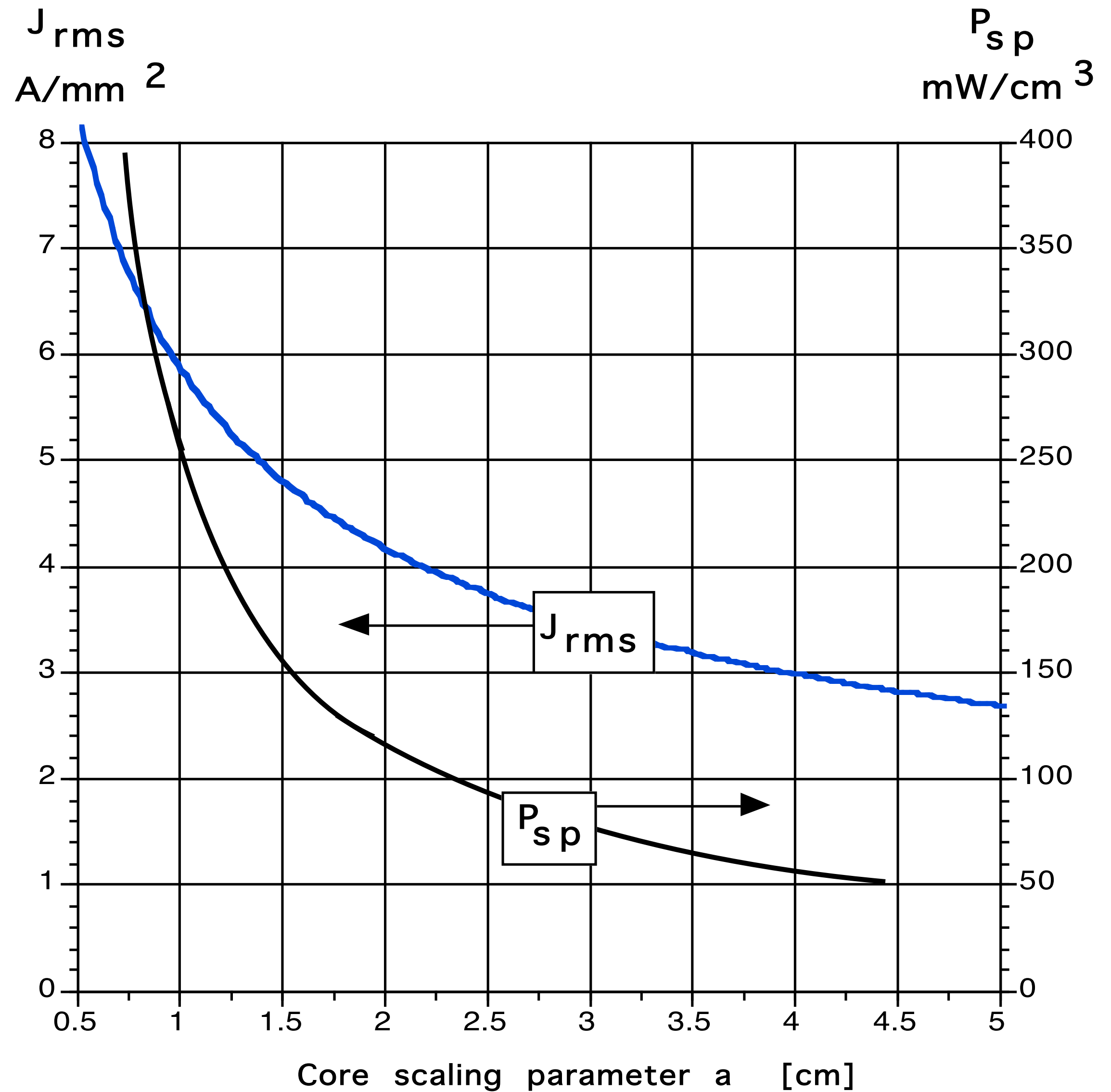
Example of Power Density and Current Density Scaling

<u>Assumptions</u>

1. Double-E core made from 3F3 ferrite
2. T_s = 100 °C and T_a = 40 °C.
3. Winding made with Leitz wire - k_{cu} = 0.3



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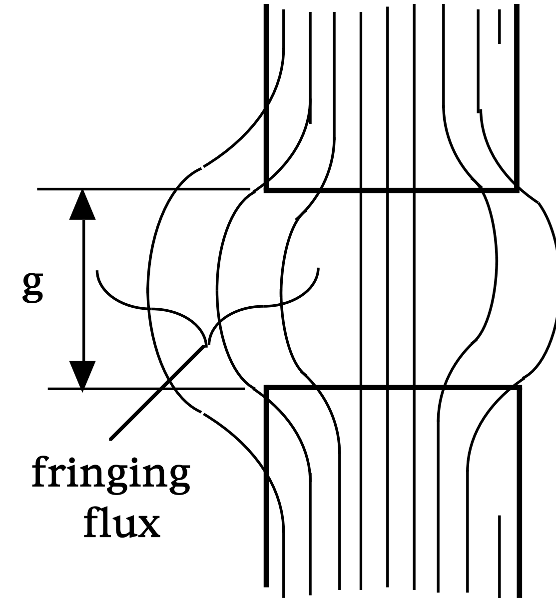
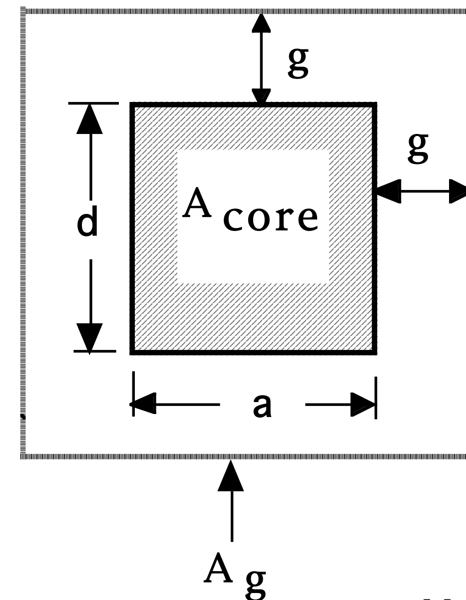
Analysis of a Specific Inductor Design



- Inductor specifications
  - Maximum current = 4 ams rms at 100 kHz
  - Double-E core with a = 1 cm using 3F3 ferrite.
  - Distributed air-gap with four gaps, two in series in each leg; total gap length Σg = 3 mm.
  - Winding - 66 turns of Leitz wire with A_{cu} = 0.64 mm^2
  - Inductor surface black with emissivity = 0.9
  - $T_{a,max}$ = 40 C
- Find; inductance L, $T_{s,max}$; effect of a 25% overcurrent on T_s
- Power dissipation in winding, $P_w = V_w\, k_{cu}\, \rho_{cu}\, (J_{rms})^2$ = 3.2 Watts
  - V_w = 12.3 cm^3 (table of core characteristics)
  - k_{cu} = 0.3 (Leitz wire)
  - ρ_{cu} at 100 C (approx. max. T_s) = 2.2x10^{-8} ohm-m
  - J_{rms} = 4/(.64) = 6.25 A/mm^2
- Power dissipation in 3F3 ferrite core, $P_{core} = V_c 1.5\text{x}10^{-6}\, f^{1.3}\, (B_{ac})^{2.5}$ = 3.3 W
  - $B_{ac} \approx \dfrac{A_g\text{"}\,\mu_o\text{"}\,N\sqrt{2}\text{"}\,I_{rms}}{A_c\text{"}\,\Sigma g}$ = 0.18 mT; assumes $H_g >> H_{core}$
    - A_g = (a + g)(d + g) = 1.71 cm^2 ; g = 3mm/4 = .075 mm
    - A_c = 1.5 cm^2 (table of core characteristics
    - V_c = 13.5 cm^3 (table of core characteristics)
    - f = 100 kHz



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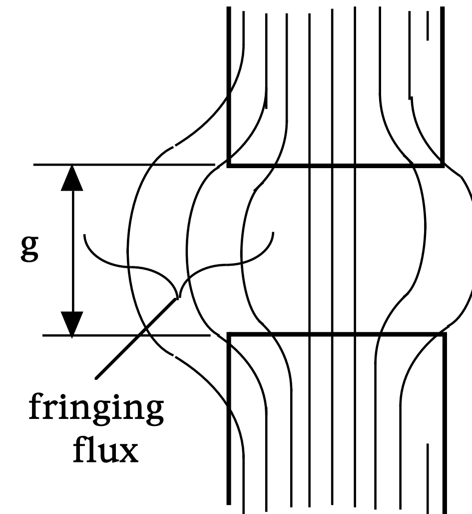
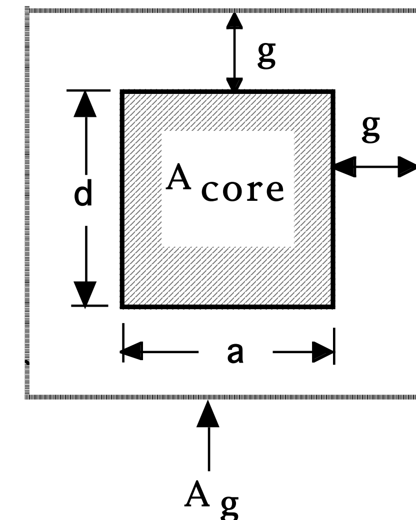
Analysis of a Specific Inductor Design (cont.)

- $L = \frac{N!\ \phi}{I} = 310\ \mu H$
  - $\phi = B_{ac}\, A_c = (0.18\ T)(1.5x10^{-4}\ m^2) = 2.6x10^{-5}\ Wb$
- Surface temperature $T_s = T_a + R_{\theta sa}\,(P_w + P_{core}) = 104\ \ C$
  - $R_{\theta sa} = R_{\theta,rad} \,||\, R_{\theta,conv} = 9.8\ \ C/W$
  - $R_{\theta,rad} = \dfrac{60}{(5.1)!\ (0.006)!\ \left(\left(\frac{373}{100}\right)^4 ! -! \left(\frac{313}{100}\right)^4 !\right)!} = 20.1\ \ [\ C/W]$
  - $R_{\theta,conv} = \dfrac{1}{(1.34)(0.006)} \sqrt[4]{\dfrac{0.035}{60}} = 19.3\ [\ C/W]$
- Overcurrent of 25% (I= 5 amp rms) makes $T_s = 146\ \ C$
  - $P_w = (3.2\ W)(1.25)^2 = 5\ W$; $P_{core} = (3.3\ W)(1.25)^{2.5} = 5.8\ W$
  - $T_s = (9.8\ \ C/W)(10.8\ W) + 40\ \ C = 146\ \ C$





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Stored Energy Relation - Basis of Inductor Design

- Input specifications for inductor design
  - Inductance value L.
  - Rated peak current I
  - Rated rms current I_{rms}.
  - Rated dc current (if any) I_{dc}.
  - Operating frequency f.
  - Maximum inductor surface temperature T_s and maximum ambient temperature T_a.
- Design consists of the following:
  - Selection of core geometric shape and size
  - Core material
  - Winding conductor geometric shape and size
  - Number of turns in winding

- Design procedure starting point - stored energy relation
  - $[L\ I]\ I_{rms} = [N\ \phi]\ I_{rms}$
  - $N = \dfrac{k_{cu} ! A_W}{A_{cu}}$
  - $\phi = B\ A_{core}$; $I_{rms} = J_{rms}\ A_{cu}$
  - $L\ I\ I_{rms} = k_{cu}\ J_{rms}\ B\ A_W\ A_{core}$
  - Equation relates input specifications (left-hand side) to needed core and winding parameters (right-hand side)
- A good design procedure will consists of a systematic, single-pass method of selecting k_{cu}, J_{rms}, B, A_W, and A_{core}.

Goal: Minimize inductor size, weight, and cost.

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Core Database - Basic Inductor Design Tool

- Interactive core database (spreadsheet-based) key to a single pass inductor design procedure.
  - User enters input specifications from converter design requirements. Type of conductor for windings (round wire, Leitz wire, or rectangular wire or foil) must be made so that copper fill factor k_{cu} is known.
  - Spreadsheet calculates capability of all cores in database and displays smallest size core of each type that meets stored energy specification.
  - Also can be designed to calculate (and display as desired) design output parameters including J_{rms}, B, A_{cu}, N, and air-gap length.
  - Multiple iterations of core material and winding conductor choices can be quickly done to aid in selection of most appropriate inductor design.

- Information on all core types, sizes, and materials must be stored on spreadsheet. Info includes dimensions, A_w, A_{core}, surface area of assembled inductor, and loss data for all materials of interest.

- Pre-stored information combined with user inputs to produce performance data for each core in spreadsheet. Sample of partial output shown below.

Core No.	Material	AP = $A_w A_{core}$	R_θ ΔT=60 C	P_{sp} @ ΔT=60 C	J_{rms} @ ΔT=60 C & P_{sp}	B_{ac} @ ΔT=60 C & 100 kHz	$k_{cu} J_{rms} \hat{B}$ •$A_w A_{core}$
•	•	•	•	•	•	•	•
8	3F3	2.1 cm^4	9.8 C/W	237 mW/cm^3	$3.3/\sqrt{k_{cu}}$	170 mT	$.0125\sqrt{k_{cu}}$
•	•	•	•	•	•	•	•

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Details of Interactive Inductor Core Database Calculations

- User inputs: L, I, I_{rms}, I_{dc}, f, T_s, T_a, and k_{cu}

- Stored information (static, independent of converter requirements)
  - Core dimensions, A_w, A_{core}, V_c, V_w, surface area, mean turn length, mean magnetic path length, etc.
  - Quantitative core loss formulas for all materials of interest including approximate temperature dependence.

- Calculation of core capabilities (stored energy value)
  1. Compute converter-required stored energy value: L I I_{rms}.
  2. Compute allowable specific power dissipation $P_{sp} = [T_s - T_a] / \{ R_{\theta sa} [V_c + V_w]\}$. $R_{\theta sa} = h/A_s$ or calculated interactively using input temperatures and formulas for convective and radiative heat transfer from Heat Sink chapter.
  3. Compute allowable flux density $P_{sp} = k f^b [B_{ac}]^d$ and current density $P_{sp} = k_{cu} \rho_{cu} \{J_{rms}\}^2$.
  4. Compute core capabilities $k_{cu} A_w A_{core} B J_{rms}$

- Calculation of inductor design parameters.
  1. Area of winding conductor $A_{cu} = I / J_{rms}$.
  2. Calculate skin depth δ in winding. If $A_{cu} > \delta^2$ at the operating frequency, then single round conductor cannot be used for winding.
     - Construct winding using Leitz wire, thin foils, or paralleled small dia. ($\leq \delta$) round wires.

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Details of Interactive Core Database Calculations (cont.)

3. Calculate number turns of N in winding: $N = k_{cu} A_w / A_{cu}$.

4. Calculate air-gap length L_g. Air-gap length determined on basis that when inductor current equals peak value I, flux density equals peak value B.
   - Formulas for air-gap length different for different core types. Example for double-E core given in next slide.

5. Calculate maximum inductance L_{max} that core can support. $L_{max} = N A_{core} B_{peak} / I_{peak}$.

   If L_{max} > required L value, reduce L_{max} by removing winding turns.
   - Save on copper costs, weight, and volume.
   - P_w can be kept constant by increasing $P_{w,sp}$
   - Keep flux density B_{peak} constant by adjusting gap length L_g.

6. Alternative L_{max} reduction procedure, increasing the value of L_g, keeping everything else constant, is a poor approach. Would not reduce copper weight and volume and thus achieve cost savings. Full capability of core would not be utilized.

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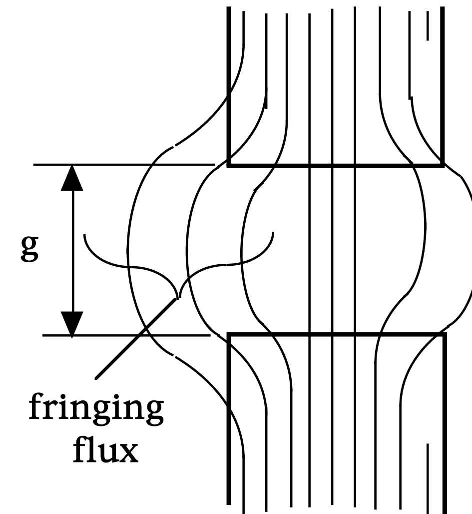
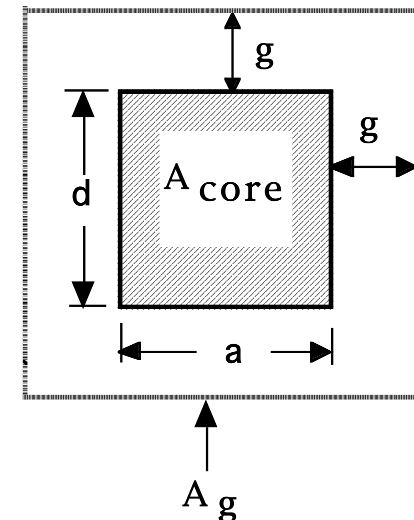
Setting Double-E Core Air-gap Length

- Set total airgap length L_g so that B_{peak} generated at the peak current I_{peak}.
- $L_g = N_g\, g$; N_g = number of distributed gaps each of length g. Distributed gaps used to minimize amount of flux fringing into winding and thus causing additional eddy current losses.
- $R_m = \dfrac{N!\, I_{peak}}{!\, A_c!\, B_{peak}} = R_{m,core} + R_{m,gap} \approx R_{m,gap} = \dfrac{L_g!}{\mu_o A_g}$
- $L_g = \dfrac{N!\, I_{peak}!\, \mu_{o!}\, A_g}{!\, A_c!\, B_{peak}}$
- For a double-E core, $A_g = \left(a + \dfrac{L_g}{N_g}\right)\left(d + \dfrac{L_g}{N_g}\right)$
  - $A_g \approx ad + (a + d)\dfrac{L_g}{N_g}$; $\dfrac{L_g}{N_g} << a$
- Insertion of expression for $A_g(L_g)$ into expression for $L_g(A_g)$ and solving for L_g yields

$$L_g = \frac{a}{!\, \dfrac{B_{peak!}\, A_c}{d!\, \mu_{o!}\, N_!\, I_{peak}} !\, -!\, \dfrac{a! +! d}{d!\, N_g}}$$

- Above expression for L_g only valid for double-E core, but similar expressions can be developed for other core shapes.





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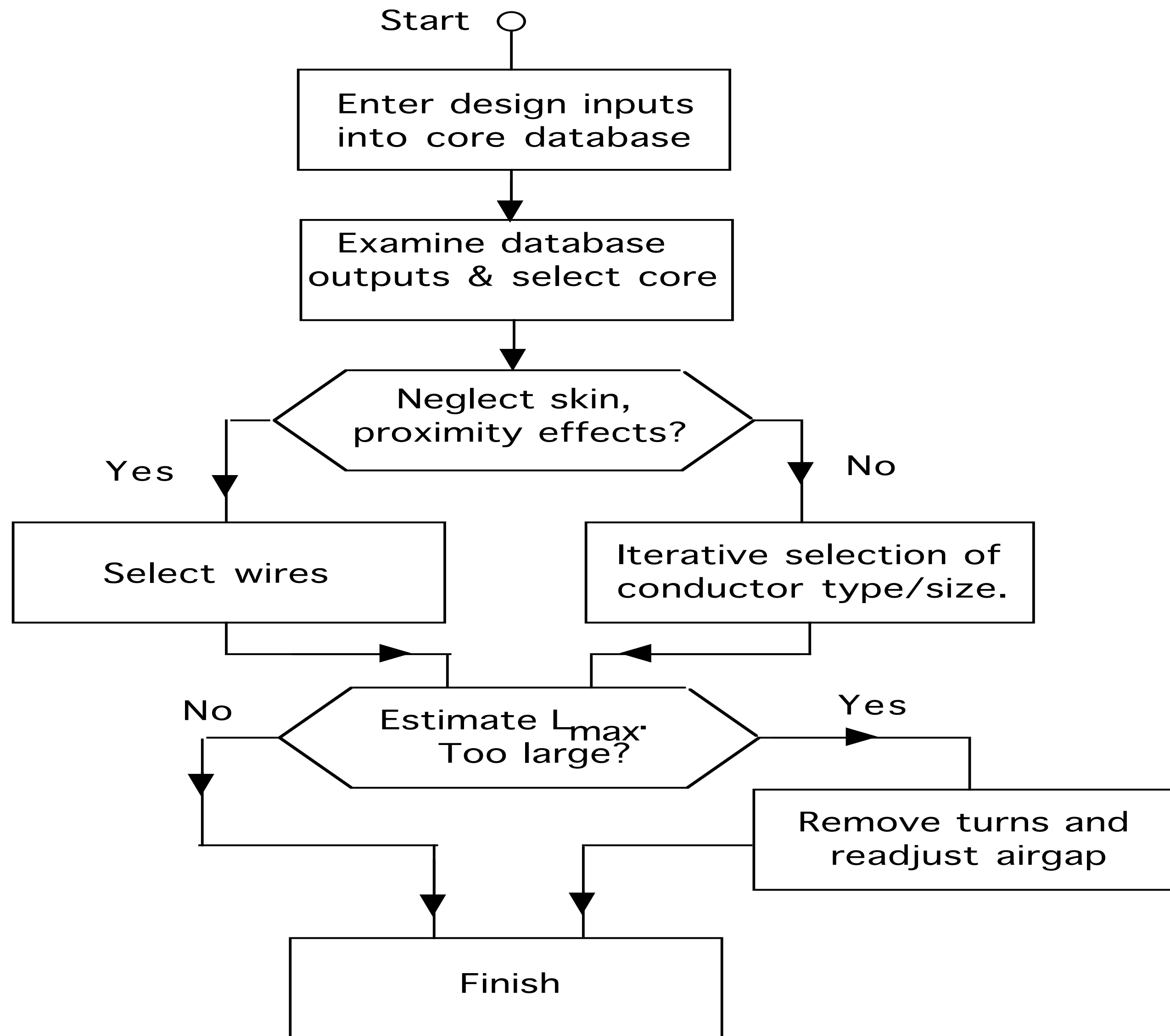
Single Pass Inductor Design Procedure



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Inductor Design Example

- Assemble design inputs
  - L = 300 microhenries
  - Peak current = 5.6 A, sinewave current, I_{rms} = 4 A
  - Frequency = 100 kHz
  - T_s = 100 C ; T_a = 40 C
- Stored energy $L\ I\ I_{rms} = (3\text{x}10^{-4})(5.6)(4)$
  $= 0.00068$ J-m^{-3}
- Core material and geometric shape
  - High frequency operation dictates ferrite material. 3F3 material has highest performance factor PF at 100 kHz.
  - Double-E core chosen for core shape.
- Double-E core with a = 1 cm meets requirements.
  $k_{cu}\ J_{rms}\ \hat{B}\ \ A_w\ A_{core} \geq 0.0125\ \sqrt{k_{cu}}\ 0.0068$
  for $k_{cu} > 0.3$
- Database output: R_θ = 9.8 C/W and
  P_{sp} = 237 mW/cm^3
- Core flux density B =170 mT from database. No I_{dc}, B_{peak} = 170 mT.
- Winding parameters.
  - Litz wire used, so k_{cu} = 0.3. J_{rms} = 6 A/mm^2
  - A_{cu} = (4 A)/(6 A/mm^2) = 0.67 mm^2
  - N = (140 mm^2)((0.3)/(0.67 mm^2) = 63 turns.
- $L_{max} = \dfrac{(63)(170\ \text{mT})(1.5\text{x}10^{-4}\ \text{m}^2)}{5.6\ \text{A}}$
  ≈ 290 microhenries
- $$L_g = \frac{10^{-2}}{\dfrac{(0.17)\,(1.5\text{x}10^{-4})}{(1.5\text{x}10^{-2})(4\pi\text{x}10^{-7})(63)(5.6)} - \dfrac{2.5\text{x}10^{-2}}{(4)(1.5\text{x}10^{-2})}}$$
  $L_g \approx$ 3 mm
- $L_{max} \approx L$ so no adjustment of inductance value is needed.

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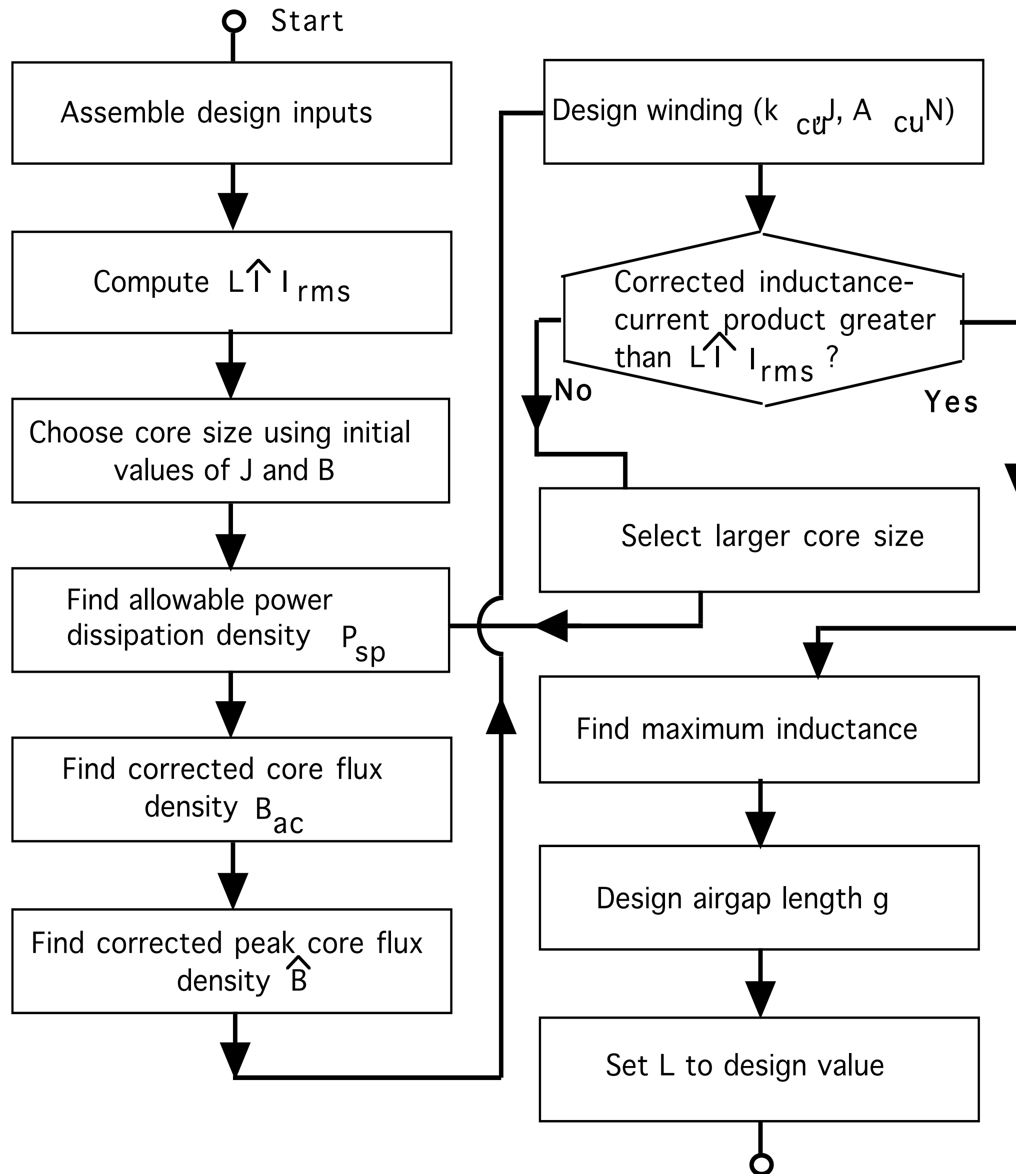
Iterative Inductor Design Procedure



- Iterative design procedure essentially consists of constructing the core database until a suitable core is found.
- Choose core material and shape and conductor type as usual.
- Use stored energy relation to find an initial area product $A_w A_c$ and thus an initial core size.
  - Use initial values of J_{rms} = 2-4 A/mm^2 and B_{ac} = 50-100 mT.
- Use initial core size estimate (value of a in double-E core example) to find corrected values of J_{rms} and B_{ac} and thus corrected value of $k_{cu}\, J_{rms}\, \hat{B}\, A_w\, A_{core}$.
- Compare $k_{cu}\, J_{rms}\, \hat{B}\, A_w\, A_{core}$ with $L\, \hat{I}\, I_{rms}$ and iterate as needed into proper size is found.

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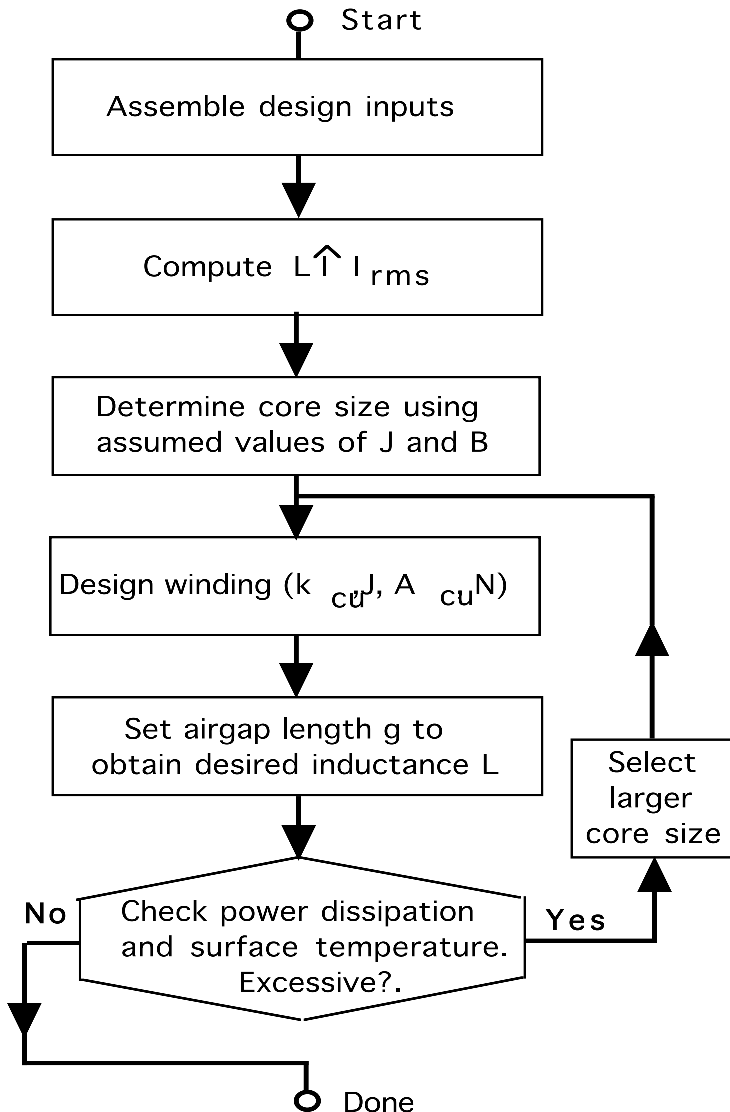
Simple, Non-optimal Inductor Design Method



- Assemble design inputs and compute required LI I_{rms}
- Choose core geometry and core material based on considerations discussed previously.
- Assume J_{rms}= 2-4 A/mm^2 and B_{ac} = 50-100 mT and use LI I_{rms} = k_{cu} J_{rms} B_{ac} A_w A_{core} to find the required area product A_w A_{core} and thus the core size.
  - Assumed values of J_{rms} and B_{ac} based on experience.
- Complete design of inductor as indicated.
- Check power dissipation and surface temperature using assumed values of J_{rms} and B_{ac}. If dissipation or temperature are excessive, select a larger core size and repeat design steps until dissipation/temperature are acceptable.
- Procedure is so-called area product method. Useful in situations where only one ore two inductors are to be built and size/weight considerations are secondary to rapid construction and testing..

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Analysis of Specific Transformer Design

- Transformer specifications
  - Wound on double-E core with a = 1 cm using 3F3 ferrite.
  - I_{pri} = 4 A rms, sinusoidal waveform; V_{pri} = 300 V rms.
  - Frequency = 100 kHz
  - Turns ratio $N_{pri}/N_{sec} = 4$ and $N_{pri} = 32$.
  - Winding window split evenly between primary and secondary and wound with Litz wire.
  - Transformer surface black (E = 0.9) and $T_a \leq 40$ C.
- Find: core flux density, leakage inductance, and maximum surface temperature T_s, and effect of 25% overcurrent on T_s.

- Areas of primary and secondary conductors, $A_{cu,pri}$ and $A_{cu,sec}$.
  - $A_{w,pri} = \dfrac{N_{pri}!A_{cu,pri}}{!k_{cu,pri}}$; $A_{w,sec} = \dfrac{N_{sec}!A_{cu,sec}}{!k_{cu,sec}}$
  - $A_{w,pri} + A_{w,sec} = A_w = \dfrac{N_{pri}!A_{cu,pri}}{!k_{cu}} + \dfrac{N_{sec}!A_{cu,sec}}{!k_{cu}}$

    where $k_{cu,pri} = k_{cu,sec} = k_{cu}$ since we assume primary and secondary are wound with same type of conductor.
- Equal power dissipation density in primary and secondary gives

  $$\frac{I_{pri}}{I_{sec}} = \frac{A_{cu,pri}}{!A_{cu,sec}} = \frac{N_{sec}}{N_{pri}}$$

  - Using above equations yields $A_{cu,pri} = \dfrac{k_{cu}!A_w}{2!N_{pri}}$ and

    $A_{cu,sec} = \dfrac{k_{cu}!A_w}{2!N_{sec}}$
  - Numerical values: $A_{cu,pri} = \dfrac{(0.3)(140!mm^2)}{(2)(32)} = 0.64\ mm^2$

    and $A_{cu,sec} = \dfrac{(0.3)(140!mm^2)}{(2)(8)} = 2.6\ mm^2$

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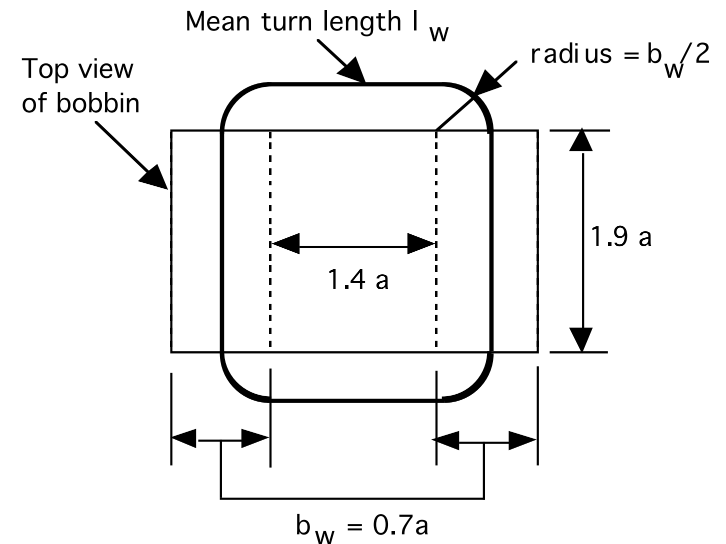
Analysis of Specific Transformer Design (cont.)

- Power dissipation in winding $P_w = k_{cu}\,\rho_{cu}(J_{rms})^2\,V_w$
  - $J_{rms} = (4\text{ A})/(0.64\text{ mm}^2) = (16\text{ A})/(2.6\text{ mm}^2) = 6.2\text{ A/mm}^2$
  - $P_w = (0.3)(2.2\text{x}10^{-8}\text{ ohm-m})\,(6.2\text{x}10^{6}\text{ A/m}^2)^2(1.23\text{x}10^{-5}\text{ m}^3)$
    $P_w = 3.1\text{ watts}$

- Flux density and core loss
  - $V_{pri,max} = N_{pri}\,A_c\,\omega\,B_{ac} = (1.414)(300) = 425\text{ V}$
  - $B_{ac} = \dfrac{425}{(32)(1.5\text{x}10^{-4}\text{ m}^2)(2\pi)(10^5\text{ Hz})} = 0.140\text{ T}$
  - $P_{core} = (13.5\text{ cm}^3)(1.5\text{x}10^{-6})(100\text{ kHz})^{1.3}(140\text{ mT})^{2.5} = 1.9\text{ W}$

- Leakage inductance $L_{leak} = \dfrac{\mu_o (N_{pri})^2\,b_w\,l_w}{3\,h_w}$
  - $l_w = 8\text{ a} = 8\text{ cm}$
  - $L_{leak} = \dfrac{(4\pi\text{x}10^{-7})(32)^2(0.7)(10^{-2})(8\text{x}10^{-2})}{(3)(2\text{x}10^{-2})} \approx 12\text{ microhenries}$



$l_w = (2)(1.4a) + (2)(1.9a) + 2\pi\,(0.35b_w) = 8\text{ a}$

- Surface temperature T_s.
  - Assume $R_{\theta,sa} \approx 9.8\ \text{C/W}$. Same geometry as inductor.
  - $T_s = (9.8)(3.1 + 1.9) + 40 = 89\ \text{C}$

- Effect of 25% overcurrent.
  - No change in core flux density. Constant voltage applied to primary keeps flux density constant.
  - $P_w = (3.1)(1.25)^2 = 4.8\text{ watts}$
  - $T_s = (9.8)(4.8 + 1.9) + 40 = 106\ \text{C}$

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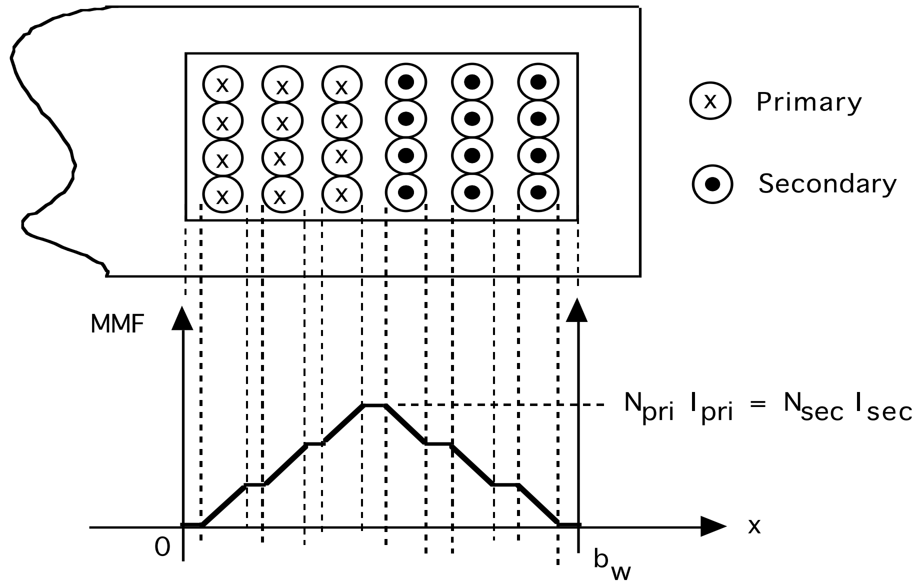
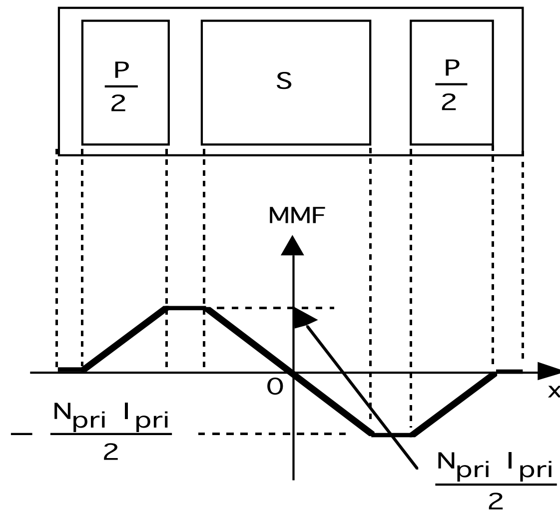
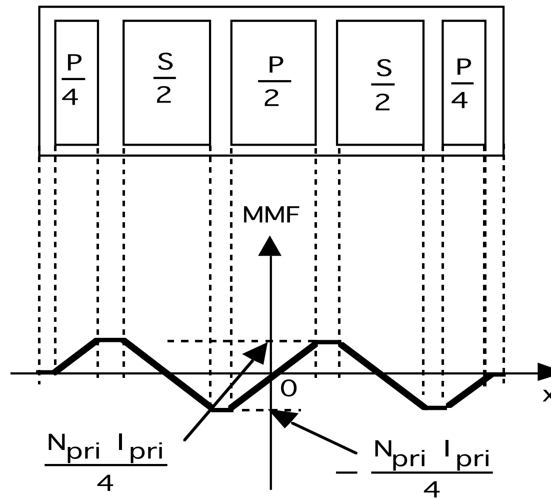
Sectioning of Transformer Windings to Reduce Winding Losses



- Reduce winding losses by reducing magnetic field (or equivently the mmf) seen by conductors in winding. Not possible in an inductor.
- Simple two-section transformer winding situation.





- Division into multiple sections reduces MMF and hence eddy current losses.

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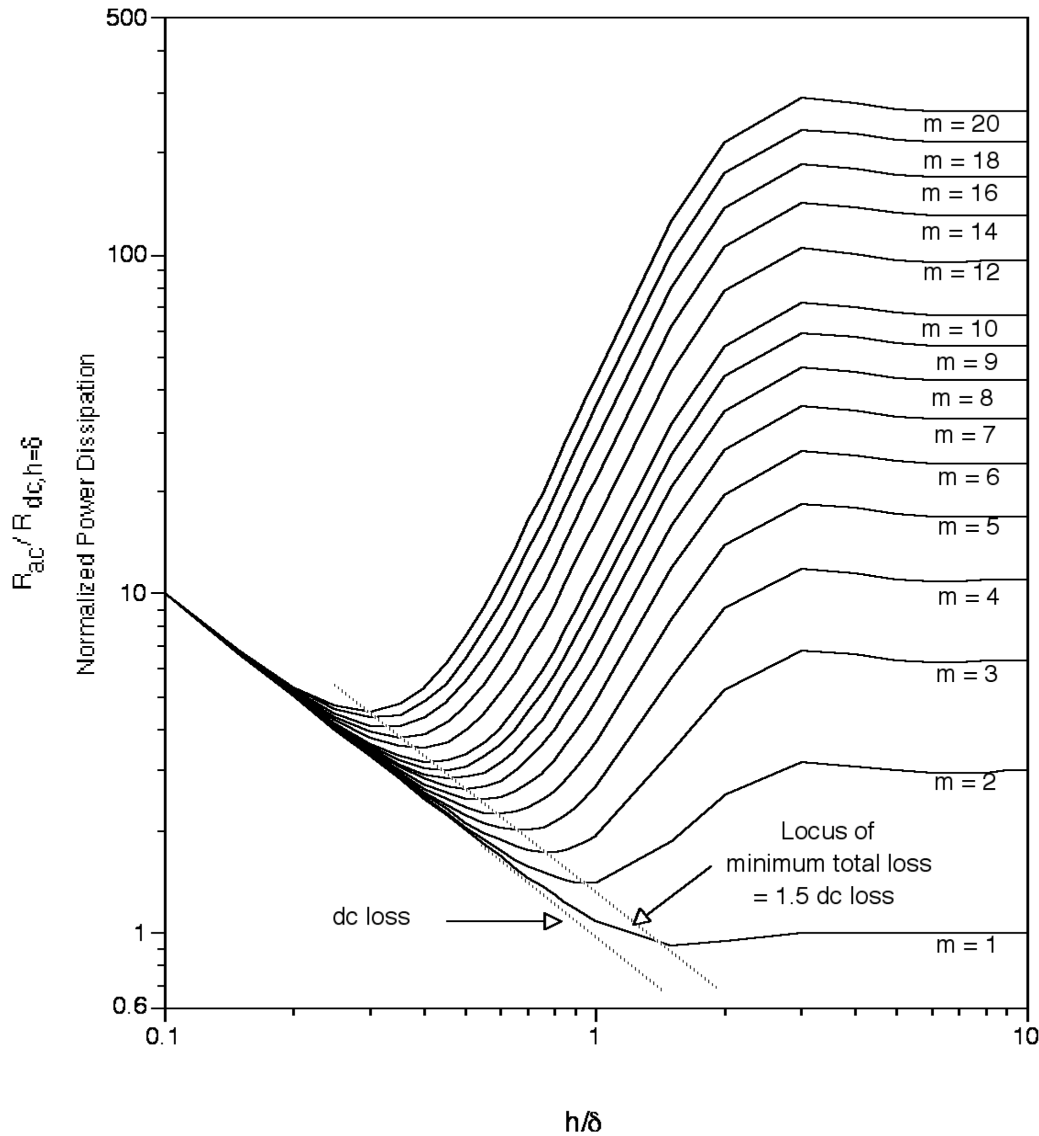
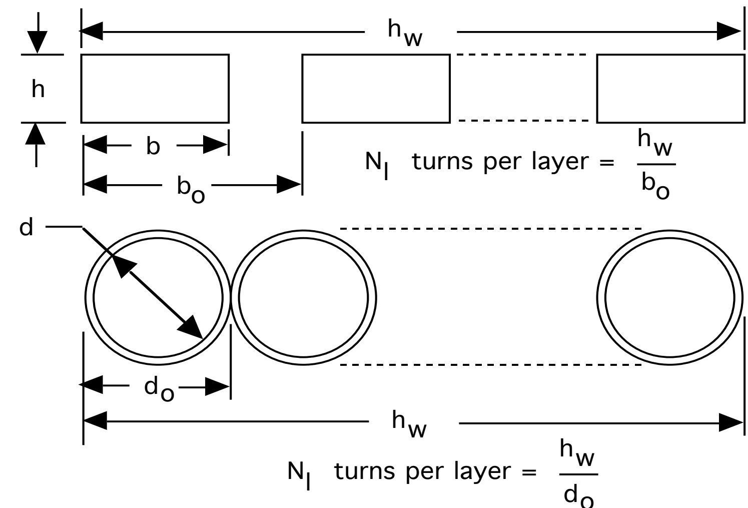
Optimization of Solid Conductor Windings



- Nomalized power dissipation = $$\frac{P_w}{R_{dc,h=\delta}(I_{rms})^2} = \frac{F_R R_{dc}}{R_{dc,h=\delta}}$$
- Conductor height/diameter $\frac{\sqrt{F_l!}\ h}{\delta}$
- F_l = copper layer factor
  - $F_l = b/b_o$ for rectangular conductors
  - $F_l = d/d_o$ for round conductors
- h = effective conductor height
  - $h = \sqrt{\frac{\pi}{4}}\, d$ for round conductors
- m = number of layers



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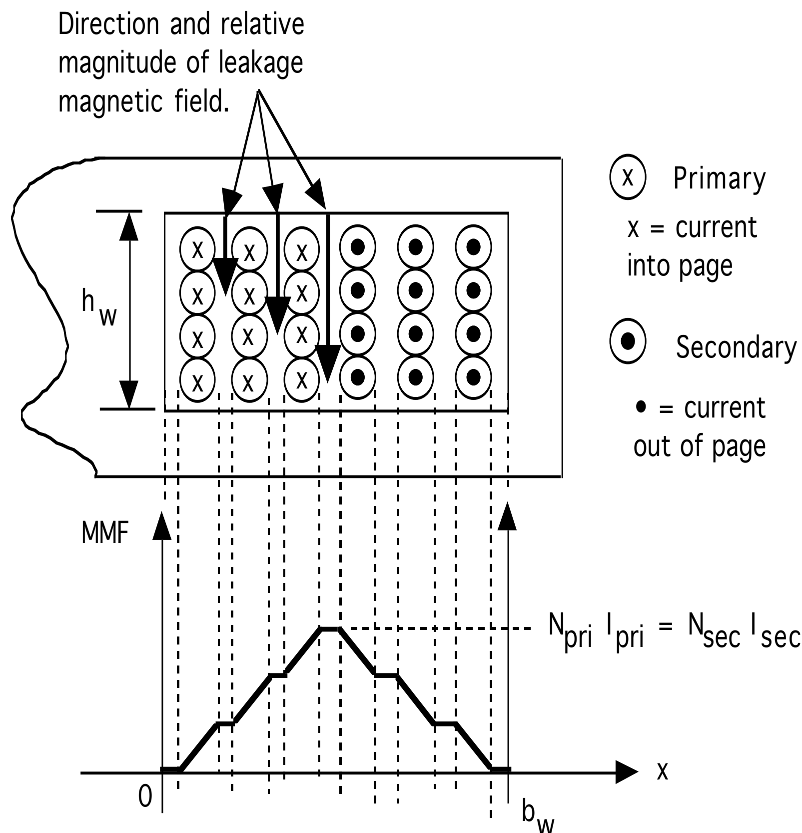
Transformer Leakage Inductance

- Transformer leakage inductance causes overvoltages across power switches at turn-off.
- Leakage inductance caused by magnetic flux which does not completely link primary and secondary windings.



- Linear variation of mmf in winding window indicates spatial variation of magnetic flux in the window and thus incomplete flux linkage of primary and secondary windings.

- $$H_{window} = H_{leak} = \frac{2!\ N_{pri}!\ I_{pri}!\ x}{h_w!\ b_w} \quad ;\ 0 < x < b_w/2$$

  $$H_{leak} = \frac{2!\ N_{pri}!\ I_{pri}}{h_w}\,(1 - x/b_w)\ ;\ \ b_w/2 < x < b_w$$

- $$\frac{L_{leak}!\ (I_{pri})^2}{2} = \frac{1}{2}\int_{V_w} \mu_o (H_{leak})^2 dV$$

- Volume element $dV = h_w\ l_w(x)dx$; $l_w(x)$ equals the length of the conductor turn located at position x.
  - Assume a mean turn length $l_w \approx 8a$ for double-E core independent of x.

- $$\frac{L_{leak}!\ (I_{pri})^2}{2} = (2)\ \frac{1}{2}\int_0^{b_w/2} \mu_o \left[\frac{2!\ N_{pri}!\ I_{pri}!\ x}{h_w!\ b_w}\right]^2 !\ h_w!\ l_w dx$$

- $$L_{leak} = \frac{\mu_o!\ (N_{pri})^2!\ l_w!\ b_w}{3!\ p^2!\ !\ h_w}$$

- If winding is split into p+1 sections, with p > 1, leakage inductance is greatly reduced.

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Volt-Amp (Power) Rating - Basis of Transformer Design

- Input design specifications
  - Rated rms primary voltage V_{pri}
  - Rated rms primary current I_{pri}
  - Turns ratio N_{pri}/N_{sec}
  - Operating frequency f
  - Maximum temperatures T_s and T_a
- Design consists of the following:
  - Selection of core geometric shape and size
  - Core material
  - Winding conductor geometric shape and size
  - Number of turns in primary and secondary windings.

- Design proceedure starting point - transformer V-A rating S
  - $S = V_{pri} I_{pri} + V_{sec} I_{sec} = 2 V_{pri} I_{pri}$
  - $V_{pri} = N_{pri} \frac{d\phi}{dt} = \frac{N_{pri} A_{core} \omega B_{ac}}{\sqrt{2}}$; $I_{pri} = J_{rms} A_{cu,pri}$
  - $S = 2 V_{pri} I_{pri} = 2 \frac{N_{pri} A_{core} \omega B_{ac}}{\sqrt{2}} J_{rms} A_{cu,pri}$
  - $A_{cu,pri} = \frac{k_{cu} A_w}{2 N_{pri}}$
  - $S = 2 V_{pri} I_{pri} = 2 \frac{N_{pri} A_{core} \omega B_{ac}}{\sqrt{2}} J_{rms} \frac{k_{cu} A_w}{2 N_{pri}}$
  - $S = V_{pri} I_{pri} = 4.4\, k_{cu}\, f\, A_{core} A_w J_{rms} B_{ac}$
- Equation relates input specifications (left-hand side) to core and winding parameters (right-hand side).
- Desired design procedure will consist of a systematic, single-pass method of selecting k_{cu}, A_{core}, A_w, J_{rms}, and B_{ac}.

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Core Database - Basic Transformer Design Tool

- Interactive core database (spreadsheet-based) key to a single pass tramsformer design procedure.
  - User enters input specifications from converter design requirements. Type of conductor for windings (round wire, Leitz wire, or rectangular wire or foil) must be made so that copper fill factor k_{cu} is known.
  - Spreadsheet calculates capability of all cores in database and displays smallest size core of each type that meets V- I specification.
  - Also can be designed to calculate (and display as desired) design output parameters including J_{rms}, B, $A_{cu,pri}$, $A_{cu,sec}$, N_{pri}, N_{sec}, and leakage inductance..
  - Multiple iterations of core material and winding conductor choices can be quickly done to aid in selection of most appropriate tranformer design.
- Information on all core types, sizes, and materials must be stored on spreadsheet. Info includes dimensions, A_w, A_{core}, surface area of assembled transformer , and loss data for all materials of interest.
- Pre-stored information combined with user inputs to produce performance data for each core in spreadsheet. Sample of partial output shown below.

Core No.	Material	AP = A_wA_c	R_θ ΔT=60 C	P_{sp} @ T_s=100 C	J_{rms} @ T_s=100 C & P_{sp}	$\hat{B}_{rated}$ @ T_s=100 C & 100 kHz	2.22 k_{cu} f J_{rms} $\hat{B}$ AP (f = 100kHz)
•	•	•	•	•	•	•	•
8	3F3	2.1 cm^4	9.8 C/W	237 mW/cm^3	$(3.3/\sqrt{k_{cu}}) \cdot \sqrt{\frac{R_{dc}}{R_{ac}}}$ A/mm^2	170 mT	$2.6\times10^3 \cdot \sqrt{\frac{k_{cu}R_{dc}}{R_{ac}}}$ [V-A]
•	•	•	•	•	•	•	•

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Details of Interactive Transformer Core Database Calculations

- User inputs: V_{pri}, I_{pri}, turns ratio N_{dc}/ N_{sec}, f, T_s, T_a, and k_{cu}

- Stored information (static, independent of converter requirements)
  - Core dimensions, A_w, A_{core}, V_c, V_w, surface area, mean turn length, mean magnetic path length, etc.
  - Quantitative core loss formulas for all materials of interest including approximate temperature dependence.

- Calculation of core capabilities
  1. Compute converter-required stored energy value: $S = 2\ V_{pri}\ I_{pri}$
  2. Compute allowable specific power dissipation $P_{sp} = [T_s - T_a] /\{ R_{\theta sa} [V_c + V_w]\}$. $R_{\theta sa} = h/A_s$ or calculated interactively using input temperatures and formulas for convective and radiative heat transfer from Heat Sink chapter.
  3. Compute allowable flux density $P_{sp} = k\ f^b\ [B_{ac}]^d$ and current density $P_{sp} = k_{cu}\ \rho_{cu}\ \{J_{rms}\}^2$.
  4. Compute core capabilities $4.4\ f\ k_{cu}\ A_w\ A_{core}\ B_{ac}\ J_{rms}$

- Calculation transformer parameters.
  1. Calculate number of primary turns $N_{pri} = V_{pri} /\{2\pi\ f\ A_{cpre} B_{ac}\}$ and secondary turns $N_{sec} = V_{sec} /\{2\pi\ f\ A_{cpre} B_{ac}\}$
  2. Calculate winding conductor areas assuming low frequencies or use of Leitz wire
     - $A_{cu,pri} = [k_{cu} A_w]/[2\ N_{pri}]$ and $A_{cu,sec} = [k_{cu} A_w]/[2\ N_{sec}]$

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Details of Interactive Transformer Core Database Calculations (cont.)

3. Calculate winding areas assuming eddy current/proximity effect is important

- Only solid conductors, round wires or rectangular wires (foils), used. $J_{rms} = [\{P_{sp} R_{dc}\}/\{R_{ac} k_{cu} r_{cu}\}]^{1/2}$
- Conductor dimensions must simultaneously satisfy area requirements and requirements of normalized power dissipation versus normalized conductor dimensions.
- May require change in choice of conductor shape. Most likely will require choice of foils (rectangular shapes).
- Several iterations may be needed to find proper combinations of dimensions, number of turns per layer, and number of layers and sections.
- Best illustrated by a specific design example.

4. Estimate leakage inductance $L_{leak} = \{\mu_o \{N_{pri}\}^2 l_w b_w\} / \{3 p^2 h_w\}$

5. Estimate $S_{max} = 4.4\ k_{cu}\ f\ A_{core}\ A_w\ J_{rms}\ B_{ac}$

6. If $S_{max} > S = 2\ V_{pri}\ I_{pri}$ reduce S_{max} and save on copper cost, weight, and volume.
   - If $N_{pri}\ w\ A_c\ B_{ac} > V_{pri}$, reduce S_{max} by reducing N_{pri} and N_{sec}.
   - If $J_{rms}\ A_{cu,\ pri} > I_{rms}$, reduce $A_{cu,pri}$ and $A_{cu,\ sec}$.
   - If $S > S_{max}$ by only a moderate amount (10-20%) and smaller than S_{max} of next core size, increase S_{max} of present core size.
   - Increase I_{rms} (and thus winding power dissipation) as needed. Temperature T_s will increase a modest amount above design limit, but may be preferable to going to larger core size.

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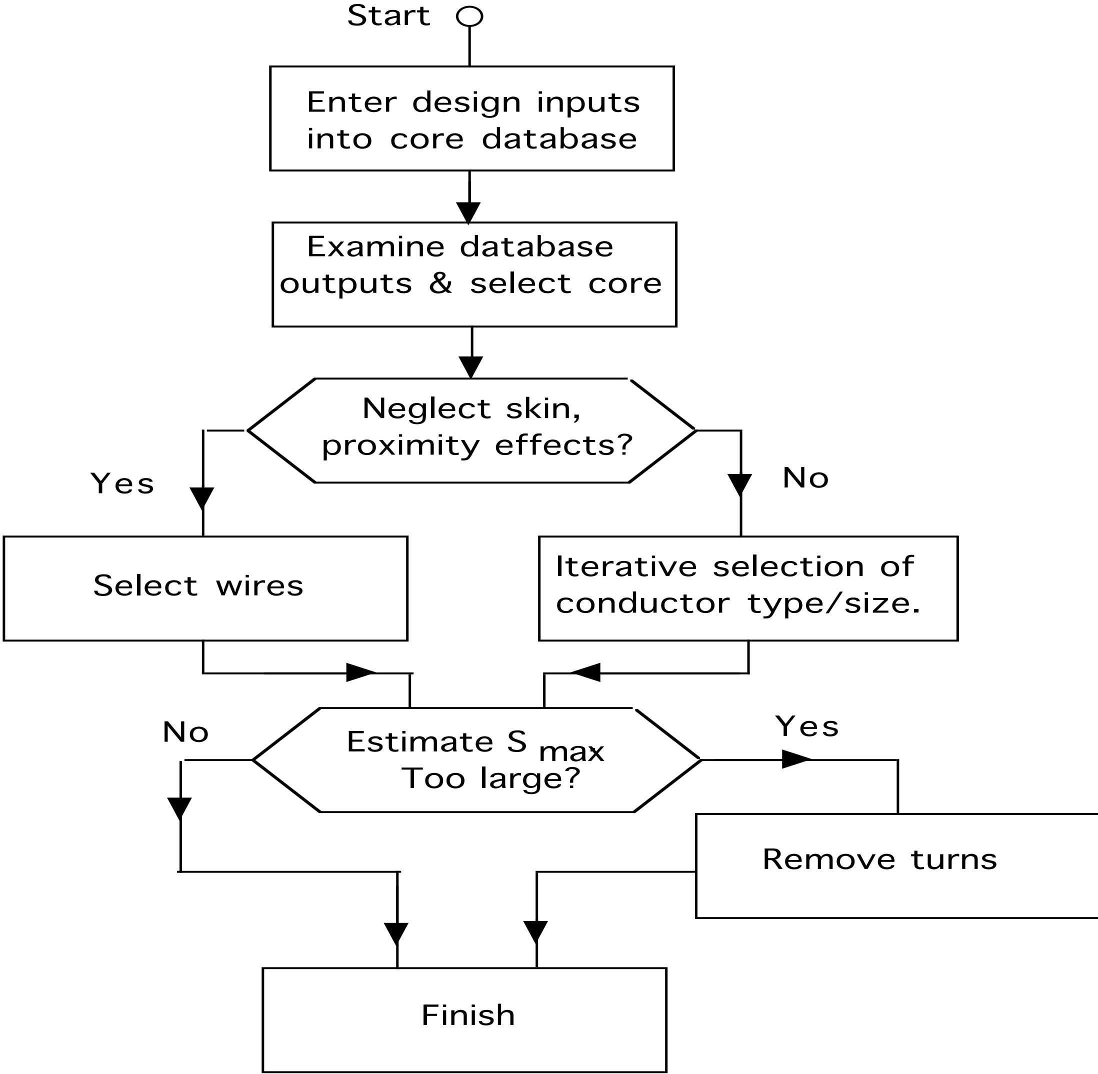
Single Pass Transformer Design Procedure



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Transformer Design Example

- Design inputs
  - V_{pri} = 300 V rms ; I_{rms} = 4 A rms
  - Turns ratio n = 4
  - Operating frequency f = 100 kHz
  - T_s = 100 C and T_a = 40 C
- V - I rating S = (300 V rms)(4 A rms) = 1200 watts
- Core material, shape, and size.
  - Use 3F3 ferrite because it has largest performance factor at 100 kHz.
  - Use double-E core. Relatively easy to fabricate winding.
- Core volt-amp rating = $2{,}600 \sqrt{k_{cu}} \sqrt{\frac{R_{dc}}{R_{ac}}}$
  - Use solid rectangular conductor for windings because of high frequency. Thus k_{cu} = 0.6 and R_{ac}/R_{dc} = 1.5.
  - Core volt-amp capability = $2{,}600 \sqrt{\frac{0.6}{1.5}}$ = 1644 watts. > 1200 watt transformer rating. Size is adequate.
- Using core database, R_θ = 9.8 C/W and P_{sp} = 240 mW/cm^3.
- Flux density and number of primary and secondary turns.
  - From core database, B_{ac} = 170 mT.
  - $N_{pri} = \frac{300\sqrt{2}}{(1.5\text{x}10^{-4}\text{m}^2)(2\pi)(10^5\text{Hz})(0.17\text{ T})}$ = 26.5 ≈ 24. Rounded down to 24 to increase flexibility in designing sectionalized transformer winding.
  - $N_{sec} = \frac{24}{6}$ = 6.
- From core database $J_{rms} = \frac{3.3}{\sqrt{(0.6)(1.5)}}$ = 3.5 A/mm^2.
  - $A_{cu,pri} = \frac{4\text{ A rms}}{3.5\text{ A rms/mm}^2}$ = 1.15 mm^2
  - $A_{cu,sec}$ = (4)(1.15 mm^2) = 4.6 mm^2

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Transformer Design Example (cont.)

- Primary and secondary conductor areas - proximity effect/eddy currents included. Assume rectangular (foil) conductors with $k_{cu} = 0.6$ and layer factor $F_l = 0.9$.

  - Iterate to find compatible foil thicknesses and number of winding sections.
  - 1st iteration - assume a single primary section and a single secondary section and each section having single turn per layer. Primary has 24 layers and secondary has 6 layers.

- Primary layer height $h_{pri} = \dfrac{A_{cu,pri}}{F_l\,h_w}$

$$= \frac{1.15\,\text{mm}^2}{(0.9)(20\,\text{mm})} = 0.064\ \text{mm}$$

  - Normalized primary conductor height

$$\phi = \frac{\sqrt{F_l}\,h_{pri}}{d} = \frac{\sqrt{0.9}\,(0.064\,\text{mm})}{(0.24\,\text{mm})} = 0.25\ ;$$

    $\delta = 0.24$ mm in copper at100 kHz and 100 C.

  - Optimum normalized primary conductor height $\phi = 0.3$ so primary winding design is satisfactory.

- Secondary layer height $h_{sec} = \dfrac{A_{cu,sec}}{F_l\,h_w}$

$$= \frac{4.6\,\text{mm}^2}{(0.9)(20\,\text{mm})} \approx 0.26\ \text{mm.}$$

  - Normalized secondary conductor height

$$\phi = \frac{\sqrt{F_l}\,h_{sec}}{d} = \frac{\sqrt{0.9}\,(0.26\,\text{mm})}{(0.24\,\text{mm})} = 1$$

  - However a six layer section has an optimum $\phi = 0.6$. A two layer section has an optimum $\phi = 1$. 2nd iteration needed.

- 2nd iteration - sectionalize the windings.

  - Use a secondary of 3 sections, each having two layers, of height $h_{sec} = 0.26$ mm.

  - Secondary must have single turn per layer. Two turns per layer would require $h_{sec} = 0.52$ mm and thus $\phi = 2$. Examination of normalized power dissipation curves shows no optimum $\phi = 2$.

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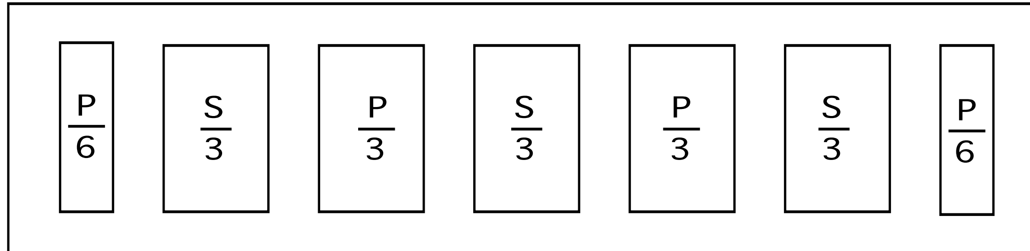
Transformer Design Example (cont.)



- Three secondary sections requires four primary sections.
  - Two outer primary sections would have 24/6 = 4 turns each and the inner two sections would have 24/3 = 8 turns each.
  - Need to determine number of turns per layer and hence number of layers per section.

Turns/ layer	h_{pri}	No. of Layers	ϕ	Optimum ϕ
1	0.064 mm	8	0.25	0.45
2	0.128 mm	4	0.5	0.6
4	0.26 mm	2	1	1

  - Use four turns per layer. Two interior primary sections have two layers and optimum value of ϕ. Two outer sections have one layer each and ϕ not optimum, but only results in slight increase in loss above the minimum.

- Leakage inductance L_{leak}

$$= \frac{(4\pi x10^{-9})(24)^2(8)(0.7)(1)}{(3)(6)^2(2)} = 0.2\ \mu H$$

  - Sectionalizing increases capacitance between windings and thus lowers the transformer self-resonant frequency.

- S_{max} = 1644 watts
  - Rated value of S = 1200 watts only marginally smaller than S_{max}. Little to be gained in reducing S_{max} to S unless a large number of transformer of this design are to be fabricated.

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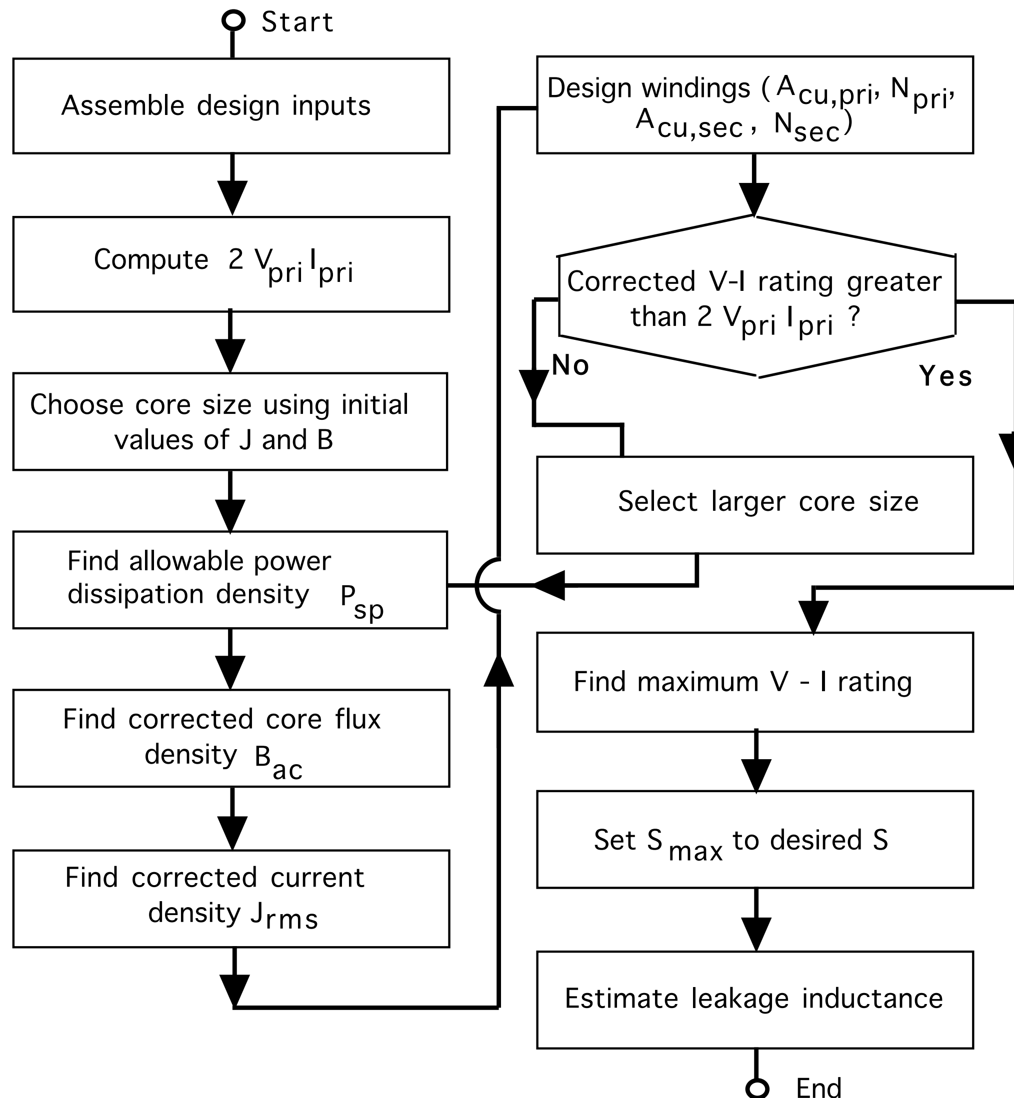
Iterative Transformer Design Procedure



- Iterative design procedure essentially consists of constructing the core database until a suitable core is found.
- Choose core material and shape and conductor type as usual.
- Use V - I rating to find an initial area product $A_w A_c$ and thus an initial core size.
  - Use initial values of J_{rms} = 2-4 A/mm^2 and B_{ac} = 50-100 mT.
- Use initial core size estimate (value of a in double-E core example) to find corrected values of J_{rms} and B_{ac} and thus corrected value of $4.4\, f\, k_{cu}\, J_{rms}\, \hat{B}\; A_w\, A_{core}$.
- Compare $4.4\, f\, k_{cu}\, J_{rms}\, \hat{B}\; A_w\, A_{core}$ with $2\, V_{pri}\, I_{pri}$ and iterate as needed into proper size is found.

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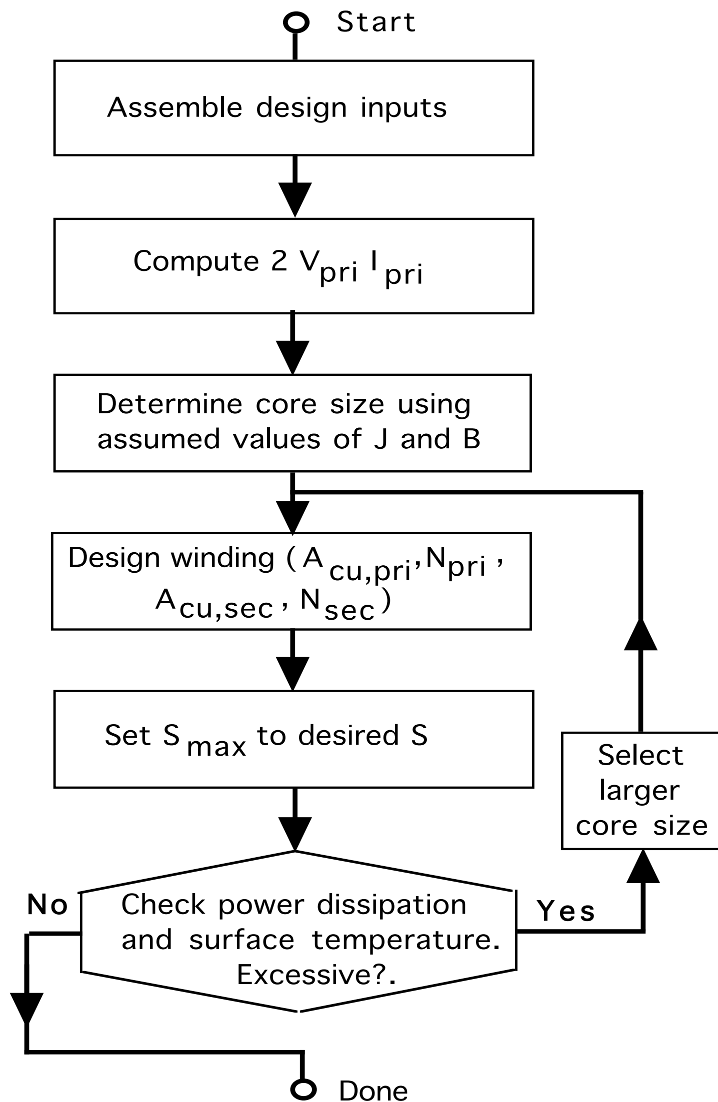
Simple, Non-optimal Transformer Design Method



- Assemble design inputs and compute required 2 V_{pri} I_{pri}
- Choose core geometry and core material based on considerations discussed previously.
- Assume J_{rms}= 2-4 A/mm^2 and B_{ac} = 50-100 mT and use 2 V_{pri} I_{pri} = 4.4 f k_{cu} J_{rms} B_{ac} A_w A_{core} to find the required area product A_w A_{core} and thus the core size.
  - Assumed values of J_{rms} and B_{ac} based on experience.
- Complete design of transformer as indicated.
- Check power dissipation and surface temperature using assumed values of J_{rms} and B_{ac}. If dissipation or temperature are excessive, select a larger core size and repeat design steps until dissipation/temperature are acceptable.
- Procedure is so-called area product method. Useful in situations where only one ore two transformers are to be built and size/weight considerations are secondary to rapid construction and testing..

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